KEYSIGHT

3 Ways to Optimize Signal Integrity in Your Design Flow

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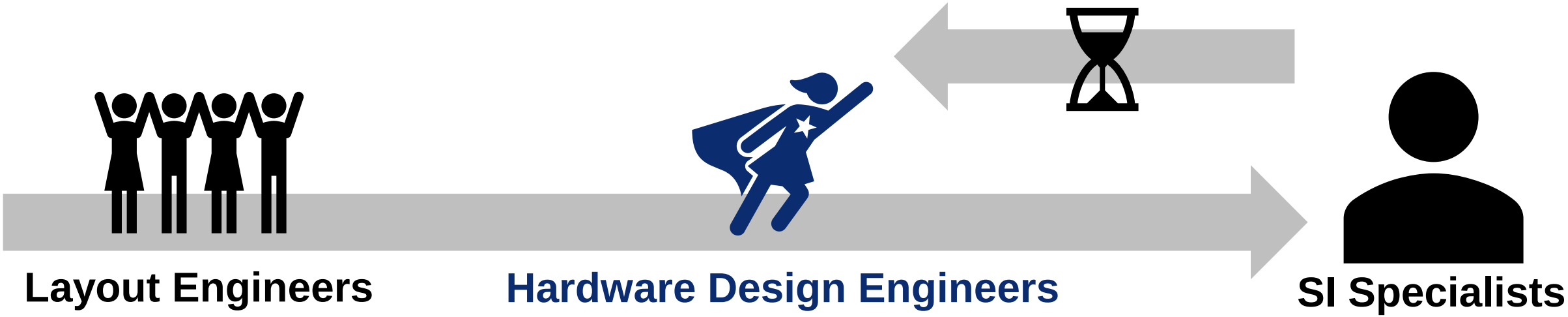
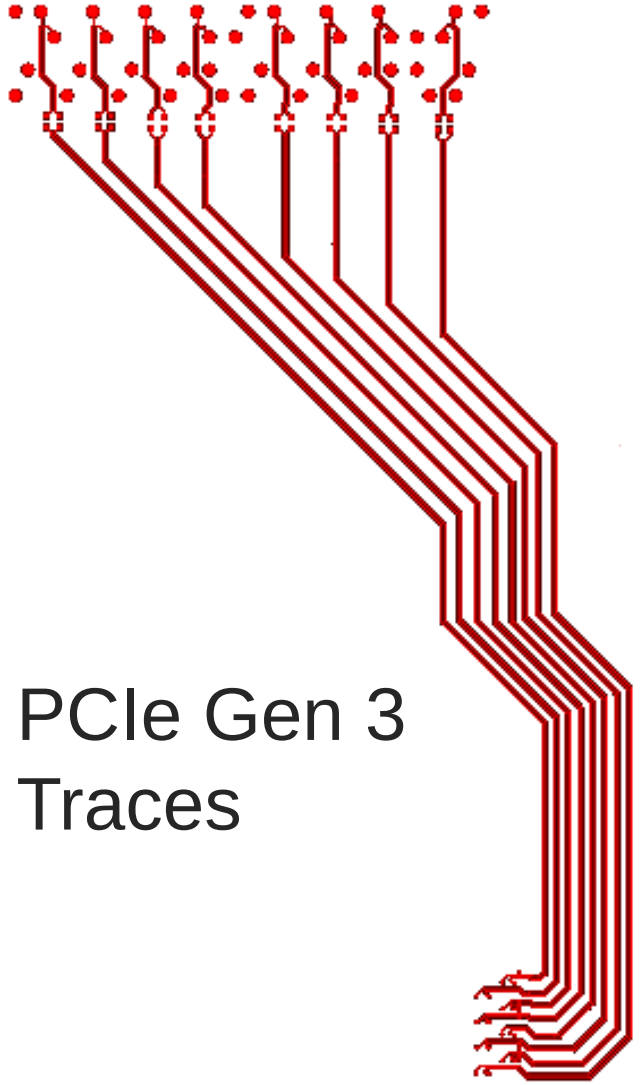
Signal Integrity Application Scientist

There Exists a Verification Bottleneck

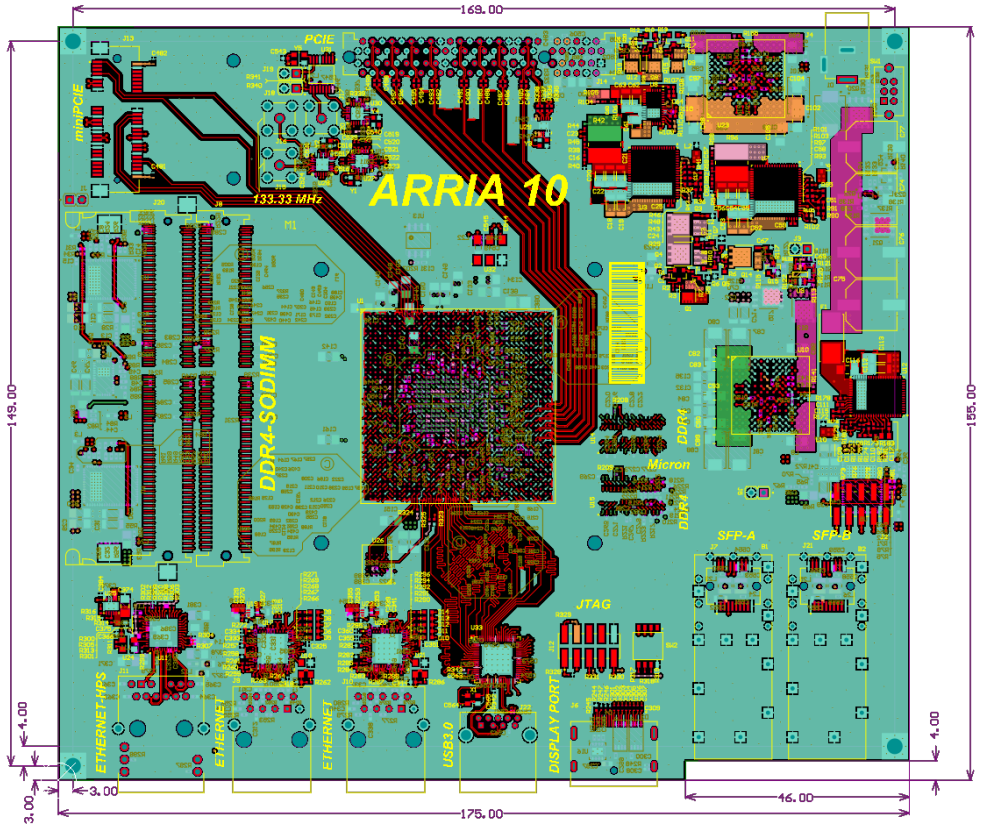


Challenge : The verification bottleneck in the design cycle.

Key Learnings to Remove the Verification Bottleneck



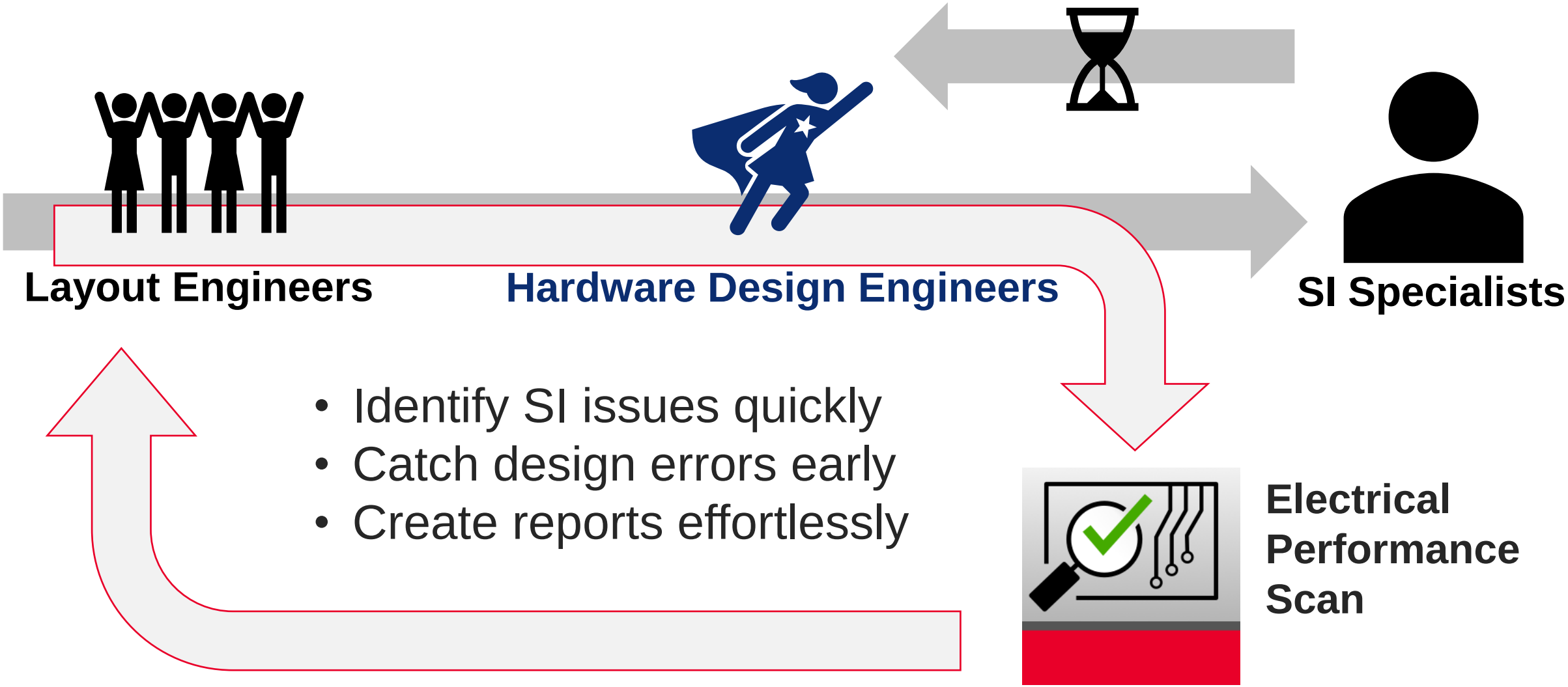
PCIe Gen 3
Traces



Root causes and fixes for

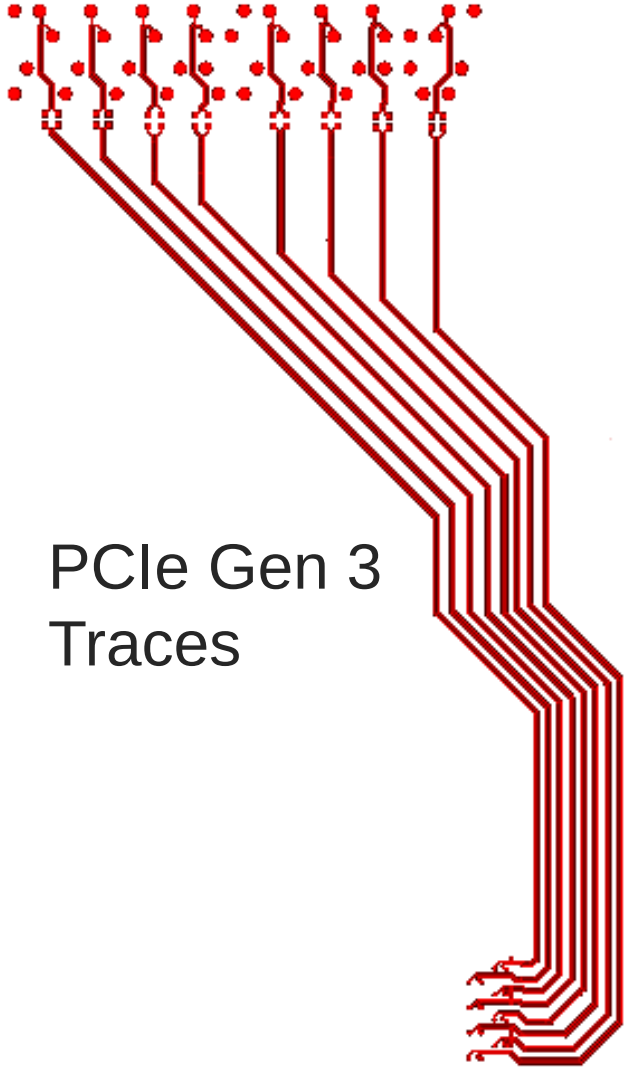
- Impedance discontinuities
- Unexpected Return loss (S_{DD11})
- Unexpected Insertion Loss (S_{DD21})

EP-Scan to Remove Verification Bottleneck



Learning #1: How to Fix Unexpected Differential Impedance

Quiz: What Differential Impedance Would Pass the Spec?

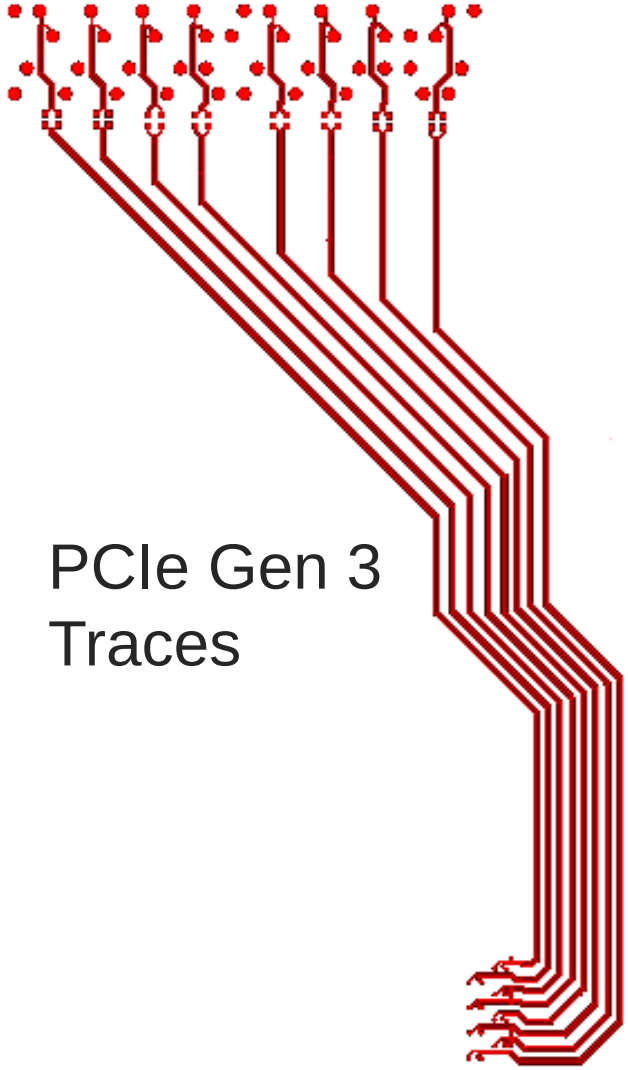


PCIe Gen 3
Traces

PCIe Gen 3

71.2 Ω 85.0 Ω 91.5 Ω

Quiz: What Differential Impedance Would Pass the Spec?



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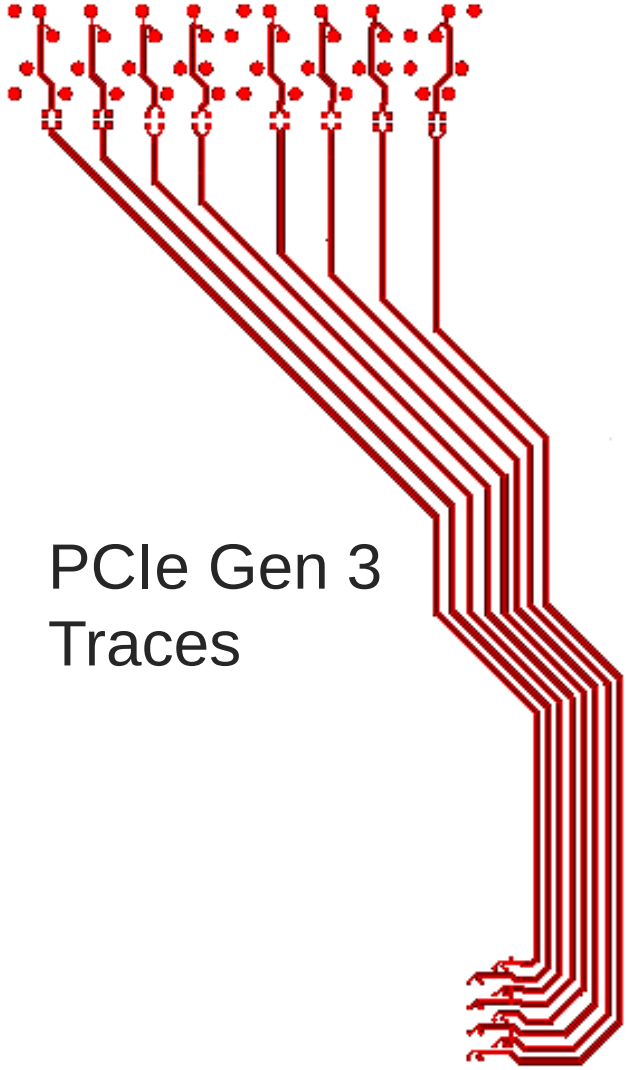
Everybody is right!

Quiz: What Differential Impedance Would Pass the Spec?



PCIe Gen 3 Traces

PCIe Gen 3

71.2 Ω 85.0 Ω 91.5 Ω

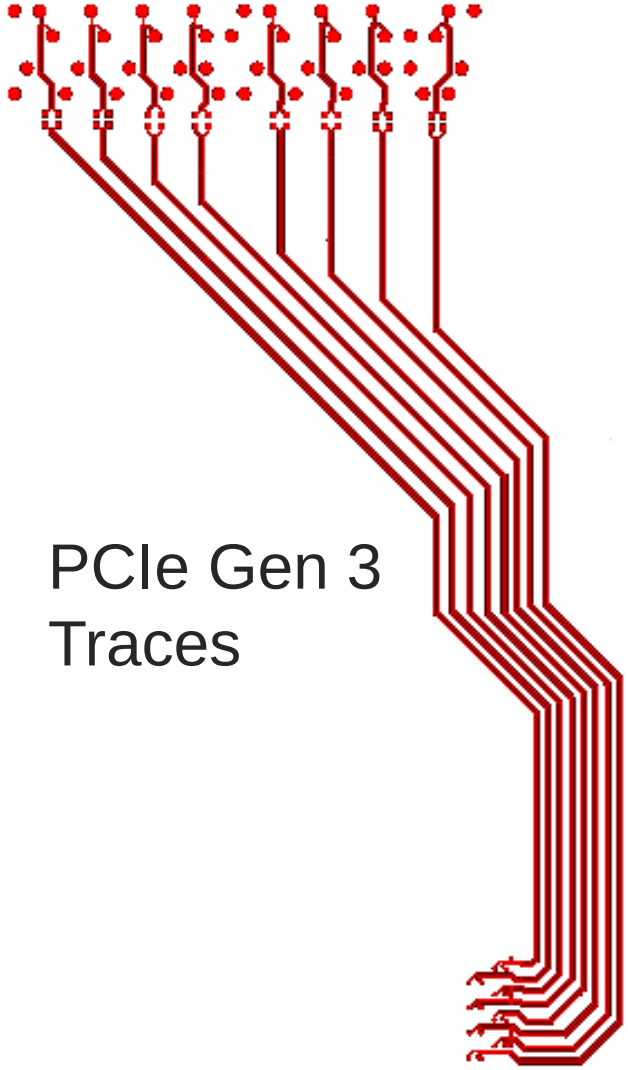
Everybody is right!

4.7.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the **range of 68 Ω to 105 Ω.** The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the **range of 70 Ω to 100 Ω.** These limits apply to both the add-in card and the system board.

Source: PCI Express® Card Electromechanical Specification Revision 3.0

One Impedance To Rule Them All



PCIe Gen 3
Traces

PCIE_TX0_P
PCIE_TX0_N

PCIE_TX1_P
PCIE_TX1_N

PCIE_TX2_P
PCIE_TX2_N

PCIE_TX3_P
PCIE_TX3_N

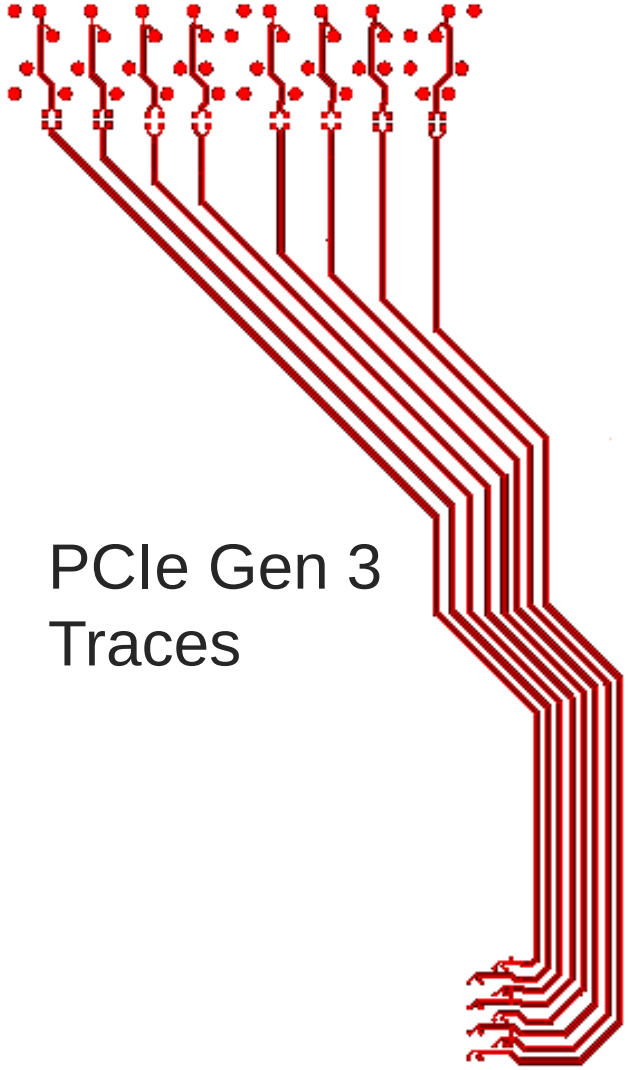
PCIE_TX4_P
PCIE_TX4_N

PCIE_TX5_P
PCIE_TX5_N

PCIE_TX6_P
PCIE_TX6_N

PCIE_TX7_P
PCIE_TX7_N

One Impedance To Rule Them All



PCIe Gen 3
Traces

PCIE_TX0_P
PCIE_TX0_N

PCIE_TX1_P
PCIE_TX1_N

PCIE_TX2_P
PCIE_TX2_N

PCIE_TX3_P
PCIE_TX3_N

PCIE_TX4_P
PCIE_TX4_N

PCIE_TX5_P
PCIE_TX5_N

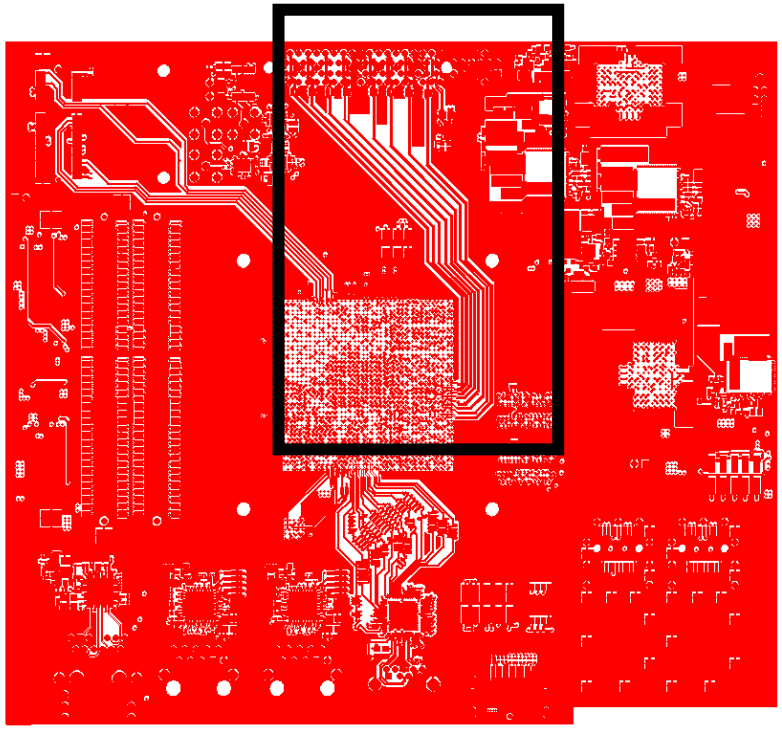
PCIE_TX6_P
PCIE_TX6_N

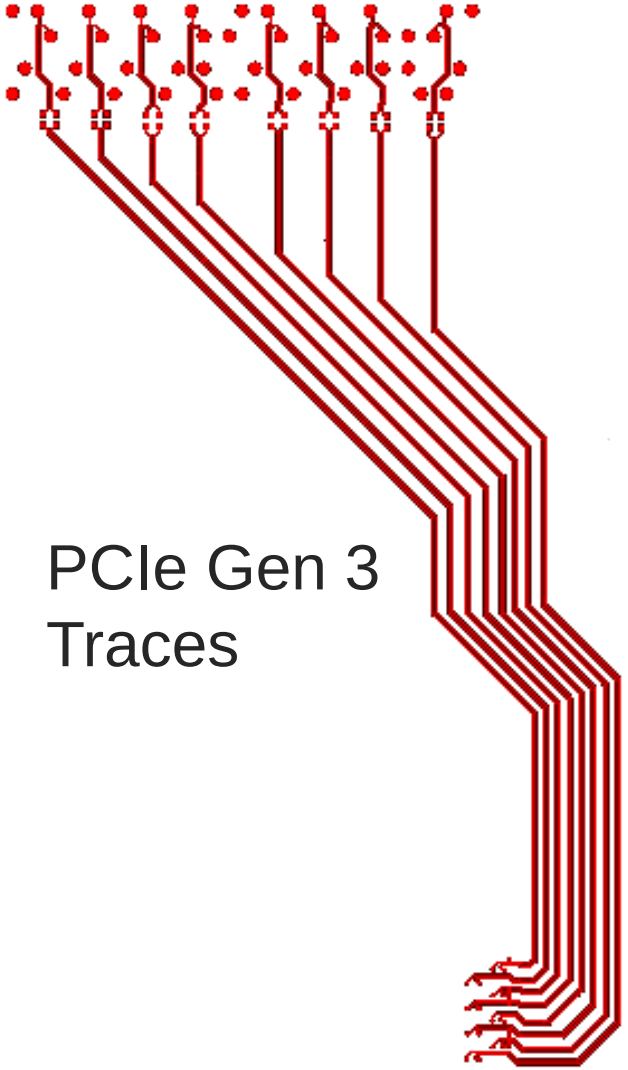
PCIE_TX7_P
PCIE_TX7_N

91.5 Ω

2 min Demo: Z_{diff} is different

We Found a Differential Pair with Different Impedance

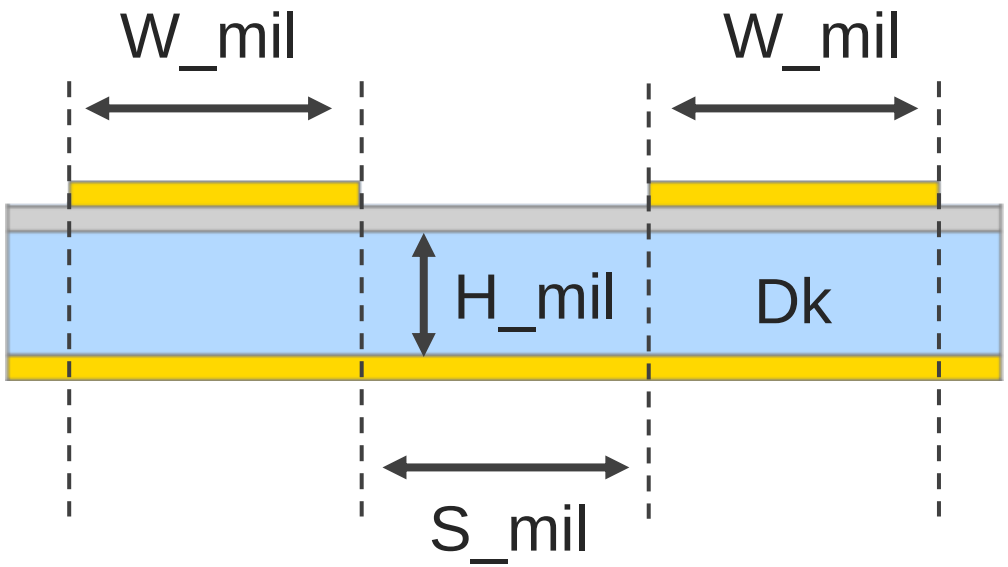




PCIe Gen 3 Traces

	Net Name	Z0 [Ohm]
1	PCIE_TX0_P PCIE_TX0_N	91.5
2	PCIE_TX1_P PCIE_TX1_N	91.5
3	PCIE_TX2_P PCIE_TX2_N	91.5
4	PCIE_TX3_P PCIE_TX3_N	91.5
5	PCIE_TX4_P PCIE_TX4_N	104.9
6	PCIE_TX5_P PCIE_TX5_N	91.5
7	PCIE_TX6_P PCIE_TX6_N	91.5
8	PCIE_TX7_P PCIE_TX7_N	91.4

Parameters that Impact the Differential Impedance

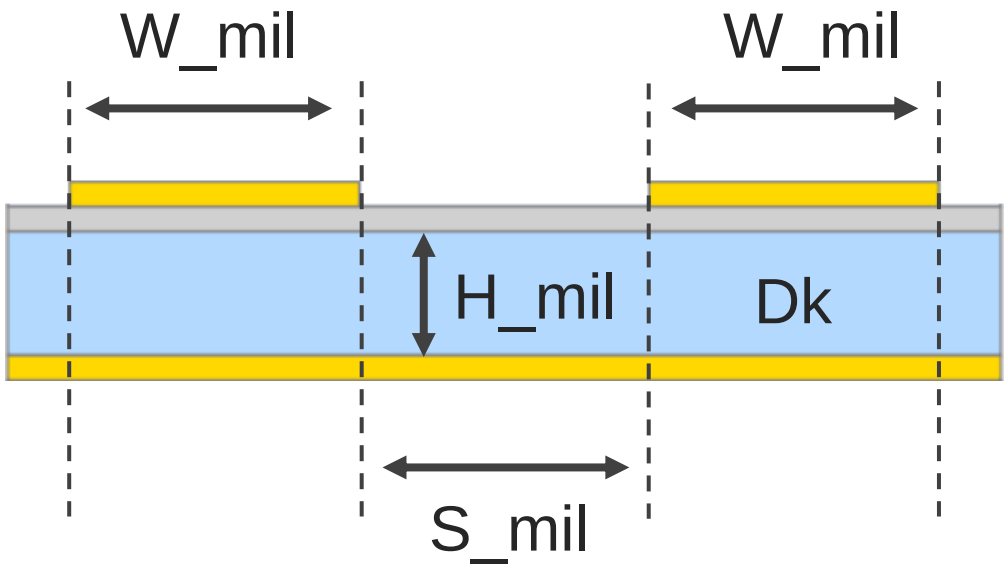


- Trace width (W_mil)
- Trace spacing (S_mil)
- Substrate height (H_mil)
- Dielectric constant (Dk)

$$Z_{diff} \propto \frac{H\_mil}{Dk \cdot W\_mil}$$

$$Z_{diff} \propto S\_mil$$

Parameters that Impact the Differential Impedance



- Trace width (W_mil)
- Trace spacing (S_mil)
- Substrate height (H_mil)
- Dielectric constant (Dk)

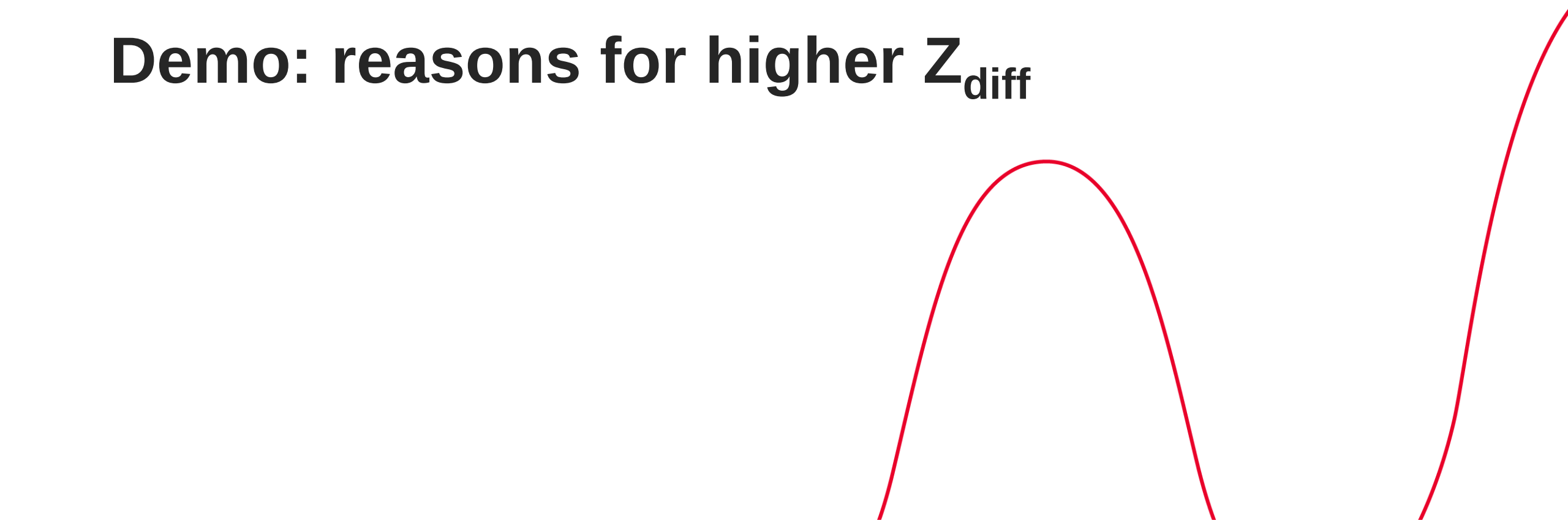
$$Z_{diff} \propto \frac{H\_mil}{Dk \cdot W\_mil}$$

Let spacing be constant, Z_{diff} increases if
- trace widths are narrower (W_mil)
- substrate height is higher
- Dk is lower

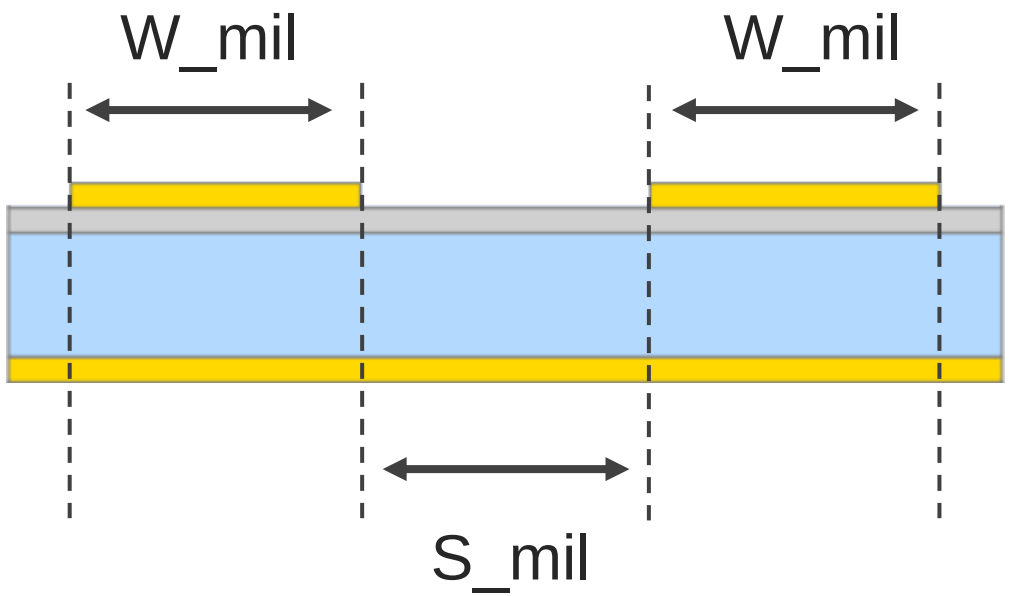
$$Z_{diff} \propto S\_mil$$

Let trace widths be constant, Z_{diff} increases if
- trace spacing is wider (S_mil)

Demo: reasons for higher Z_{diff}



Increase Trace Width and Decrease Spacing to Lower Z_{diff}



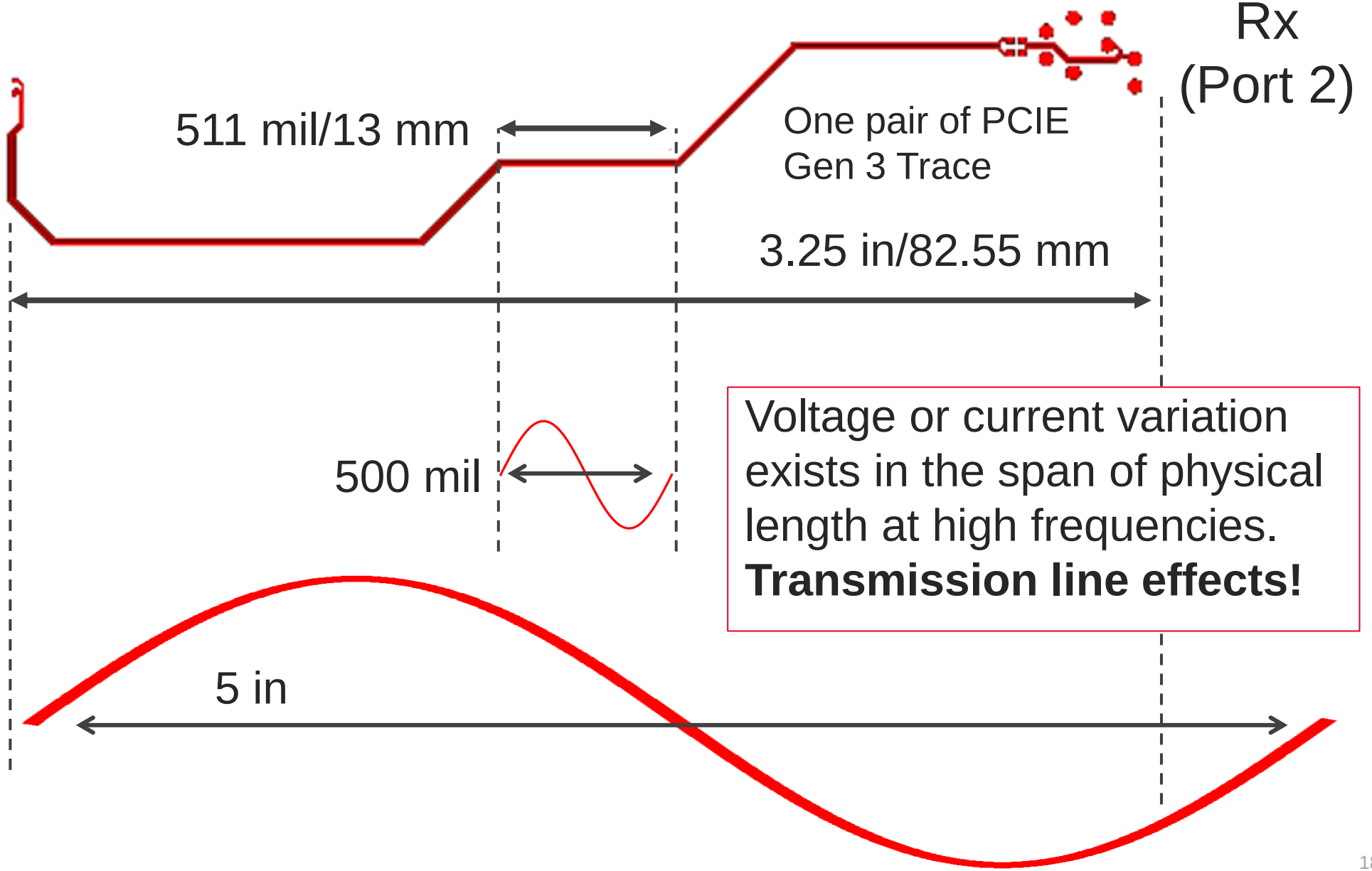
Decrease Z_{diff} , make

- trace widths wider (W_mil ⬆)
- trace spacing narrower (S_mil ⬇)

Z0 [Ohm]	Width [mil]	Spacing [mil]
104.9	4.7	5.9
91.5	5.9	4.7

Learning #2: How to Fix Unexpected S_{DD11}

Transmission Line Effects Are Present at Higher Frequencies

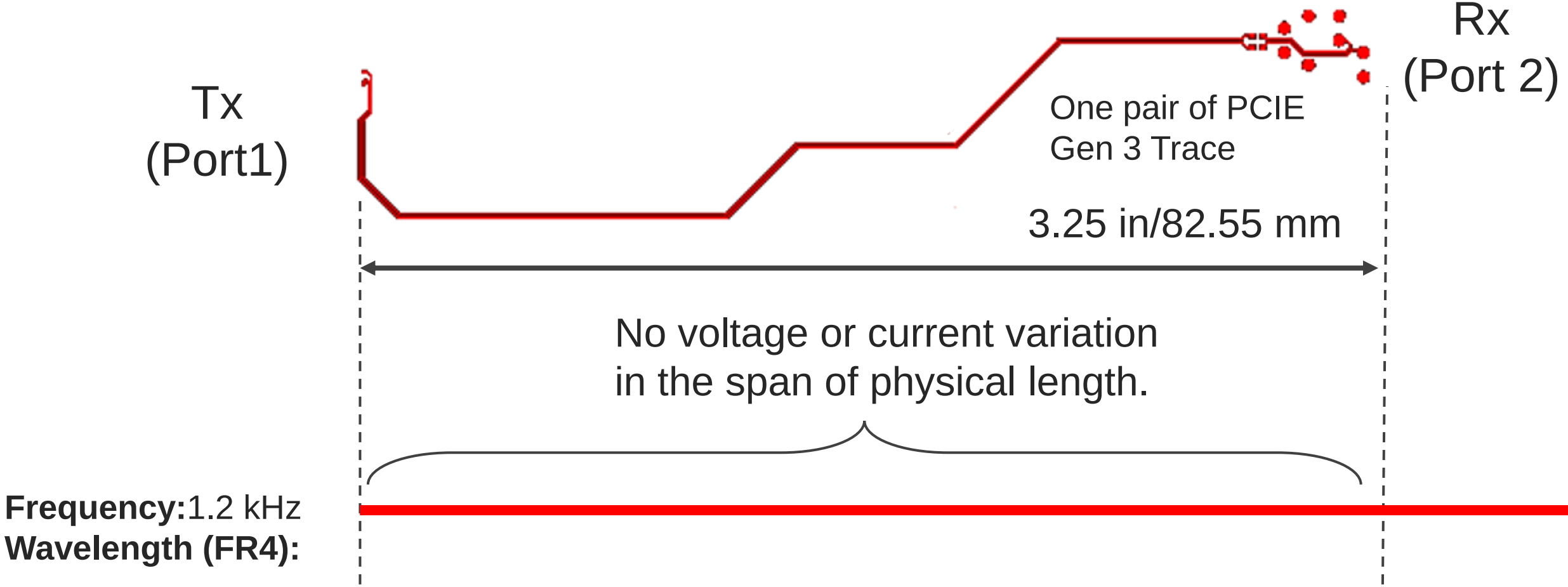


Frequency:
12 GHz
Wavelength (FR4):
6 in/nsec/12 ~ 500 mil

Frequency:
1.2 GHz
Wavelength (FR4):
6 in/nsec/1.2 ~ 5 in

Voltage or current variation exists in the span of physical length at high frequencies. **Transmission line effects!**

Interconnects Are Transparent at the Low Frequency

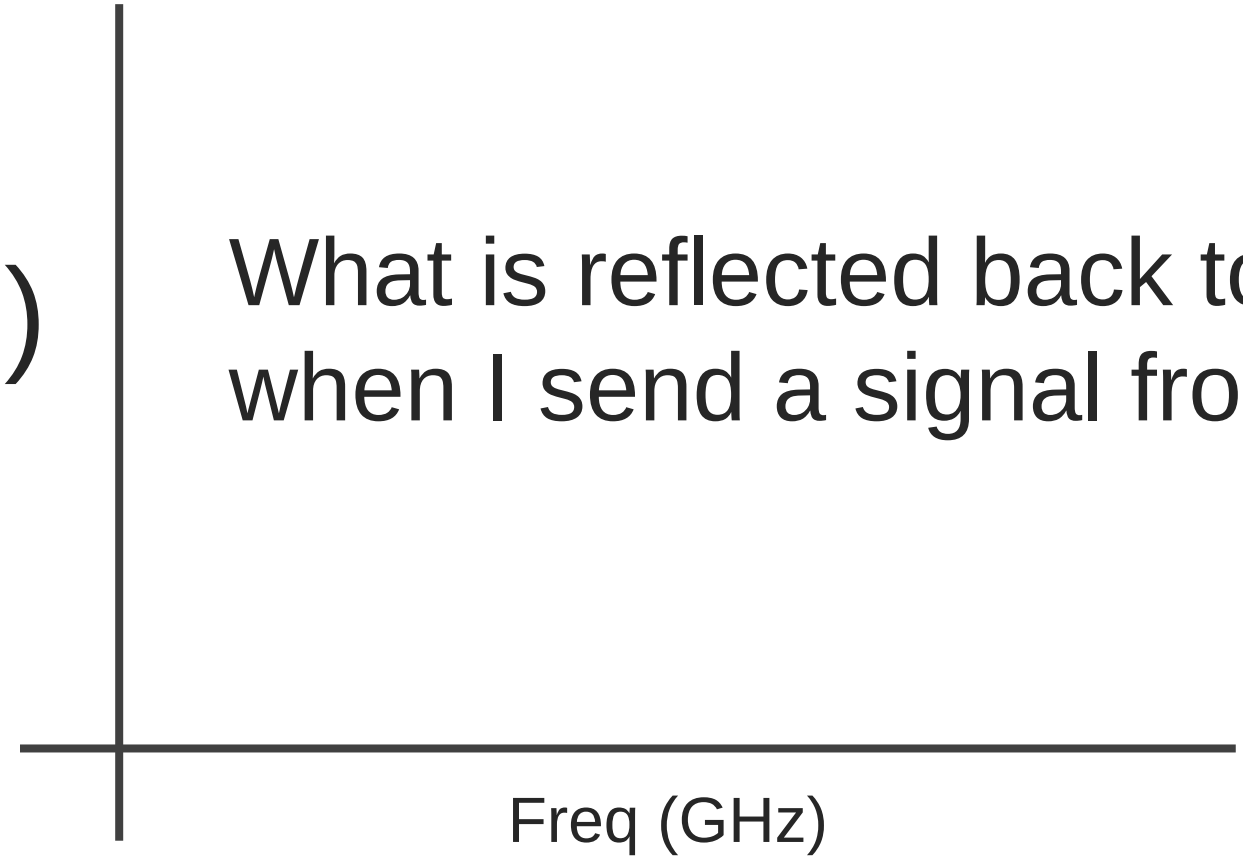


7.8 miles

Quick Definition of S_{DD11}

At the low frequency, interconnects are **transparent**.

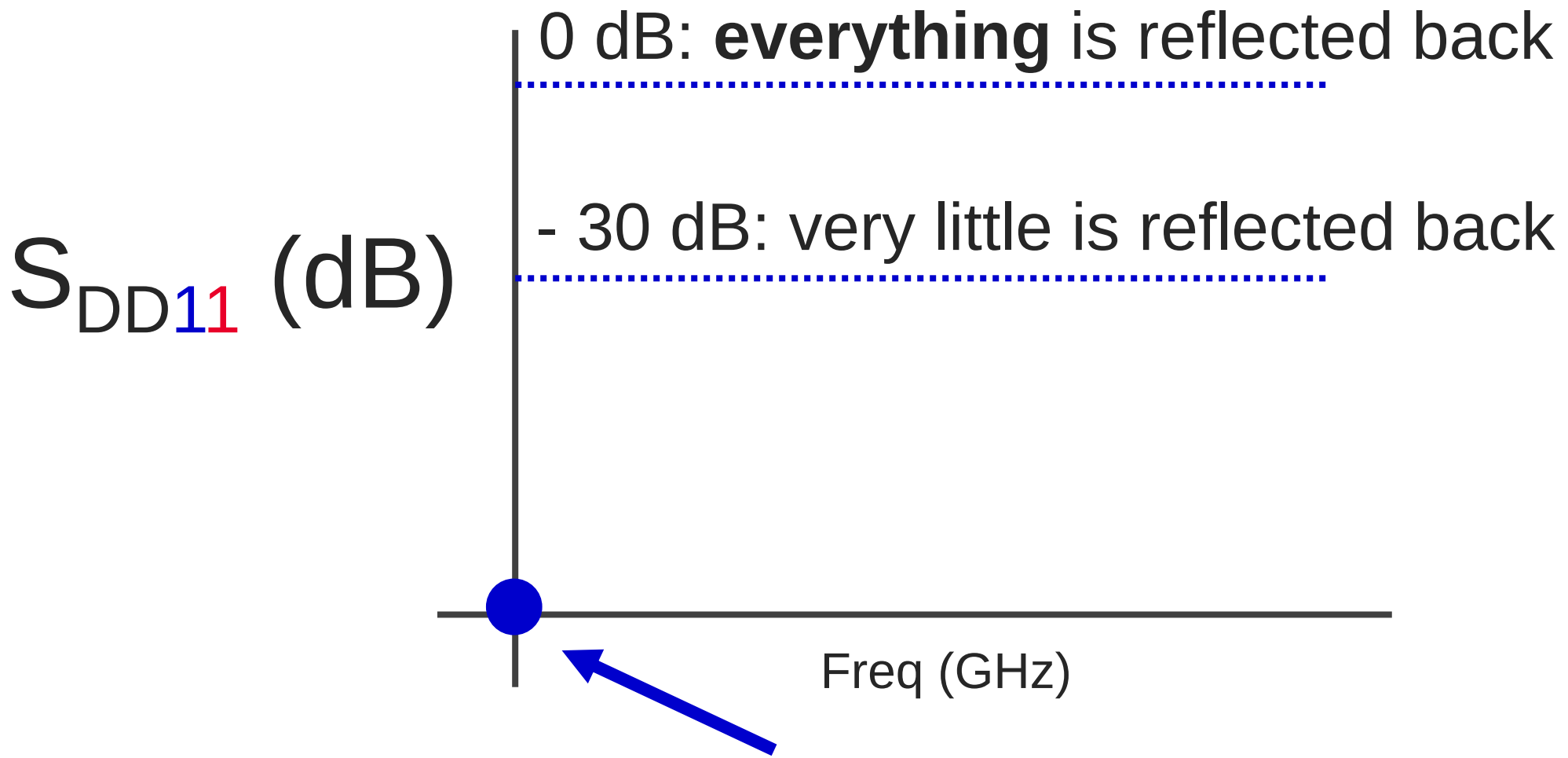
S_{DD11} (dB)



What is reflected back to **port 1**
when I send a signal from **port 1**

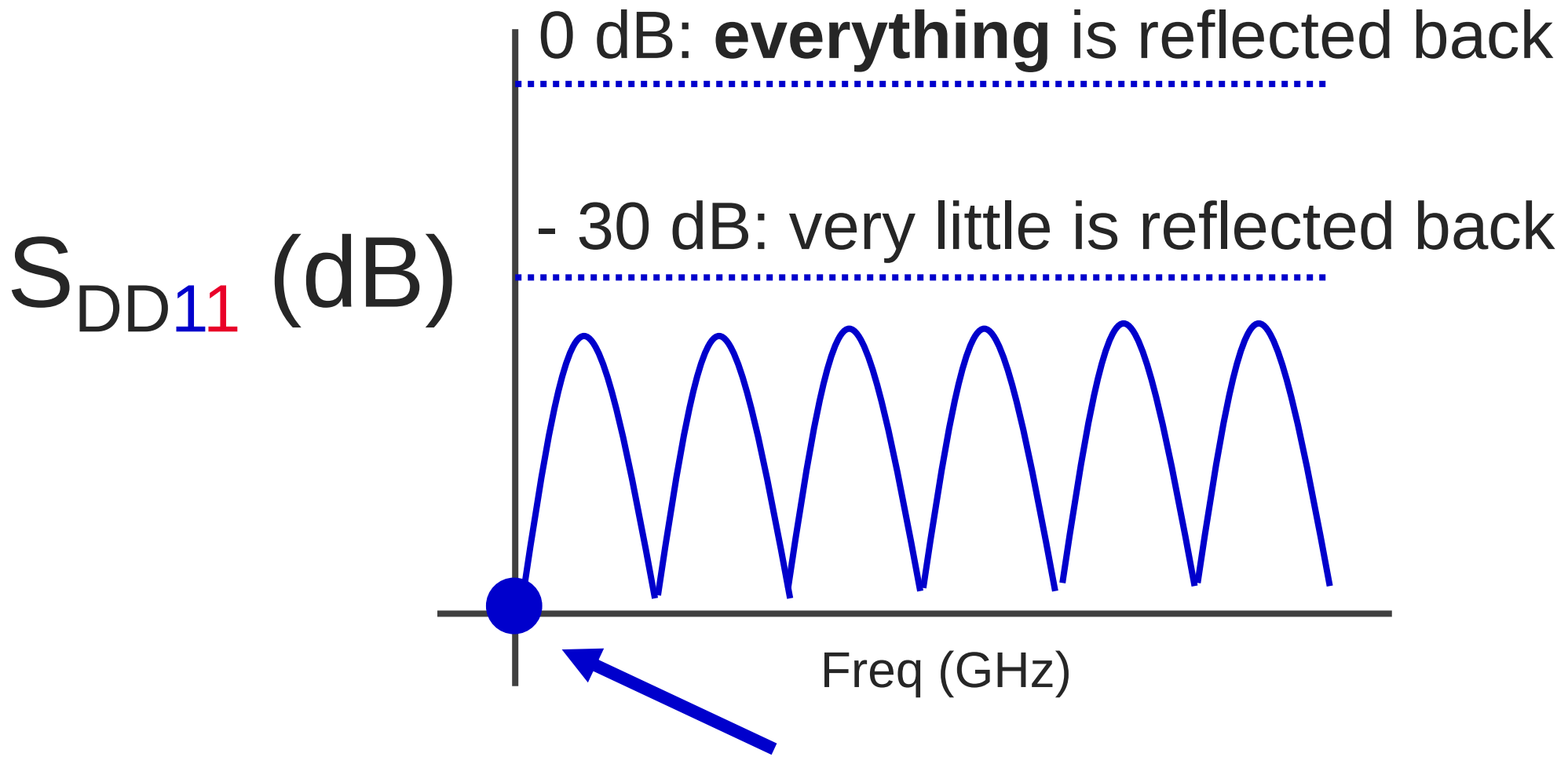
Expect S_{DD11} to Have Large Negative dB at Low Frequency

At the low frequency, interconnects are **transparent**.



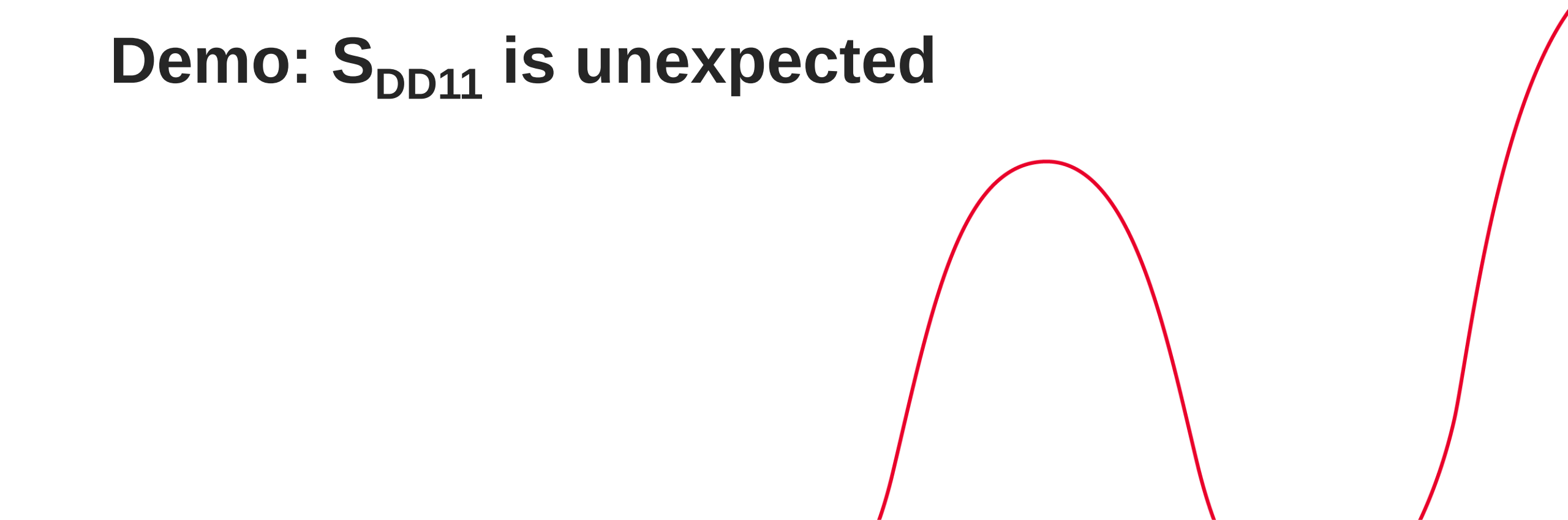
Expect S_{DD11} to Have Ripples at Higher Frequencies

At the low frequency, interconnects are **transparent**.

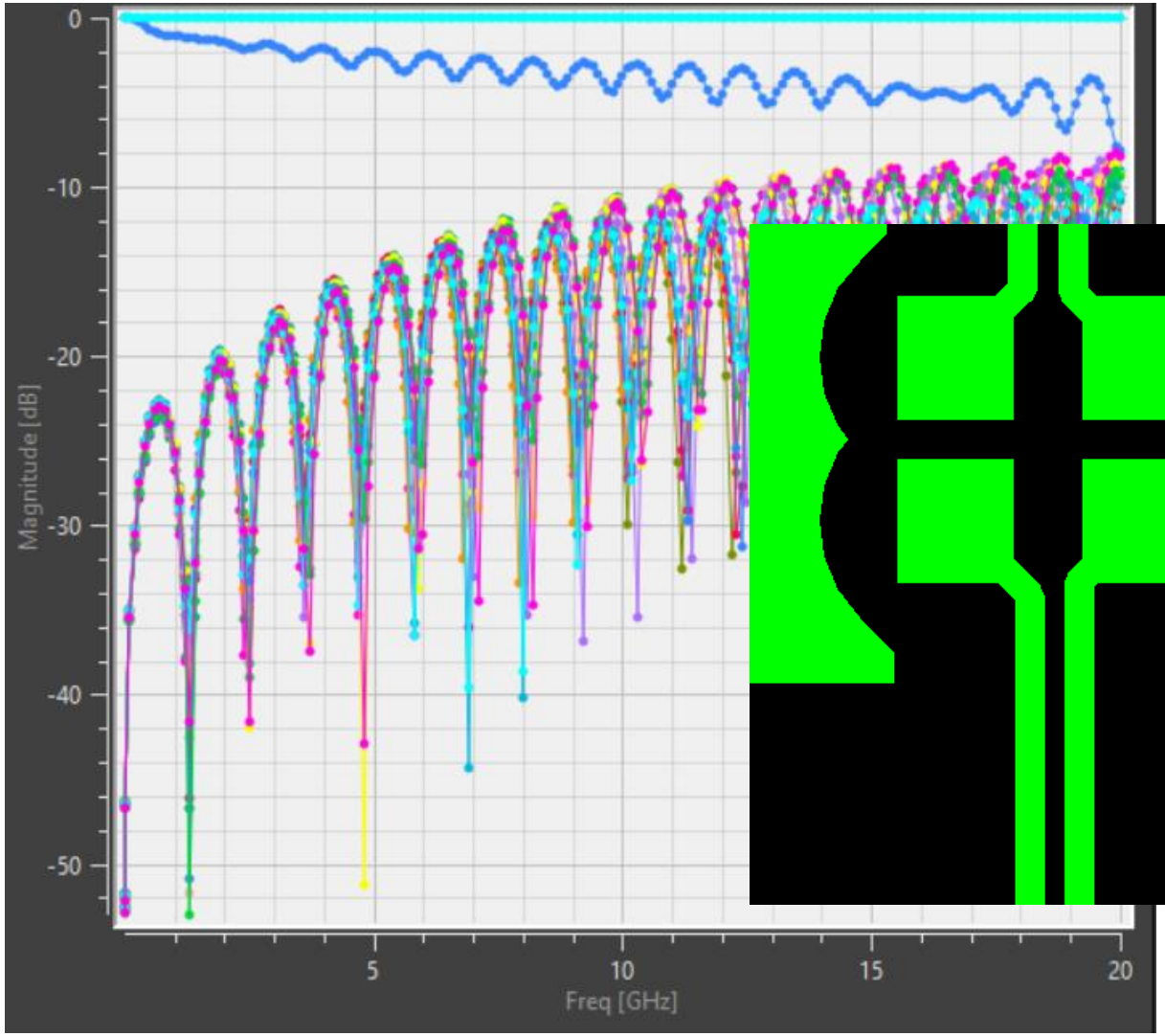


Large negative dB: **nothing** is reflected back

Demo: S_{DD11} is unexpected



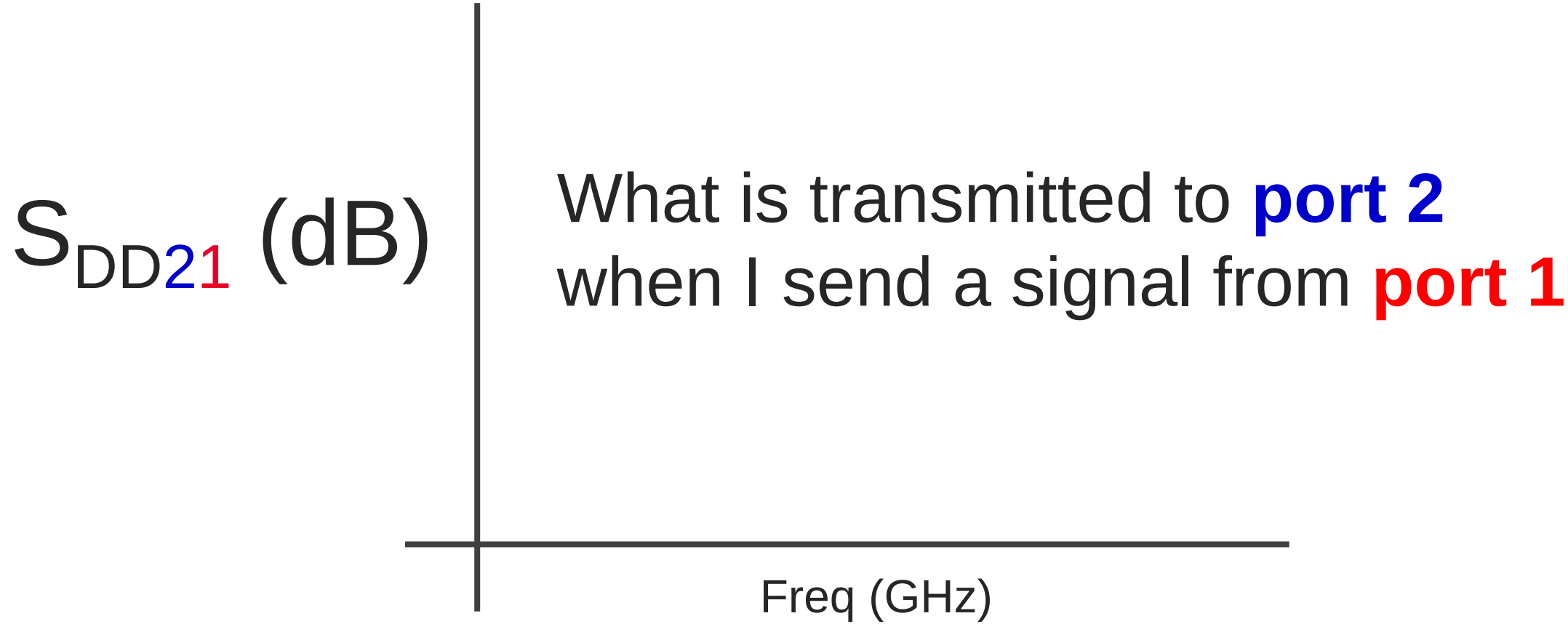
Fix Connection to Resolve Unexpected S_{DD11}



Learning #3: How to Fix Unexpected S_{DD21}

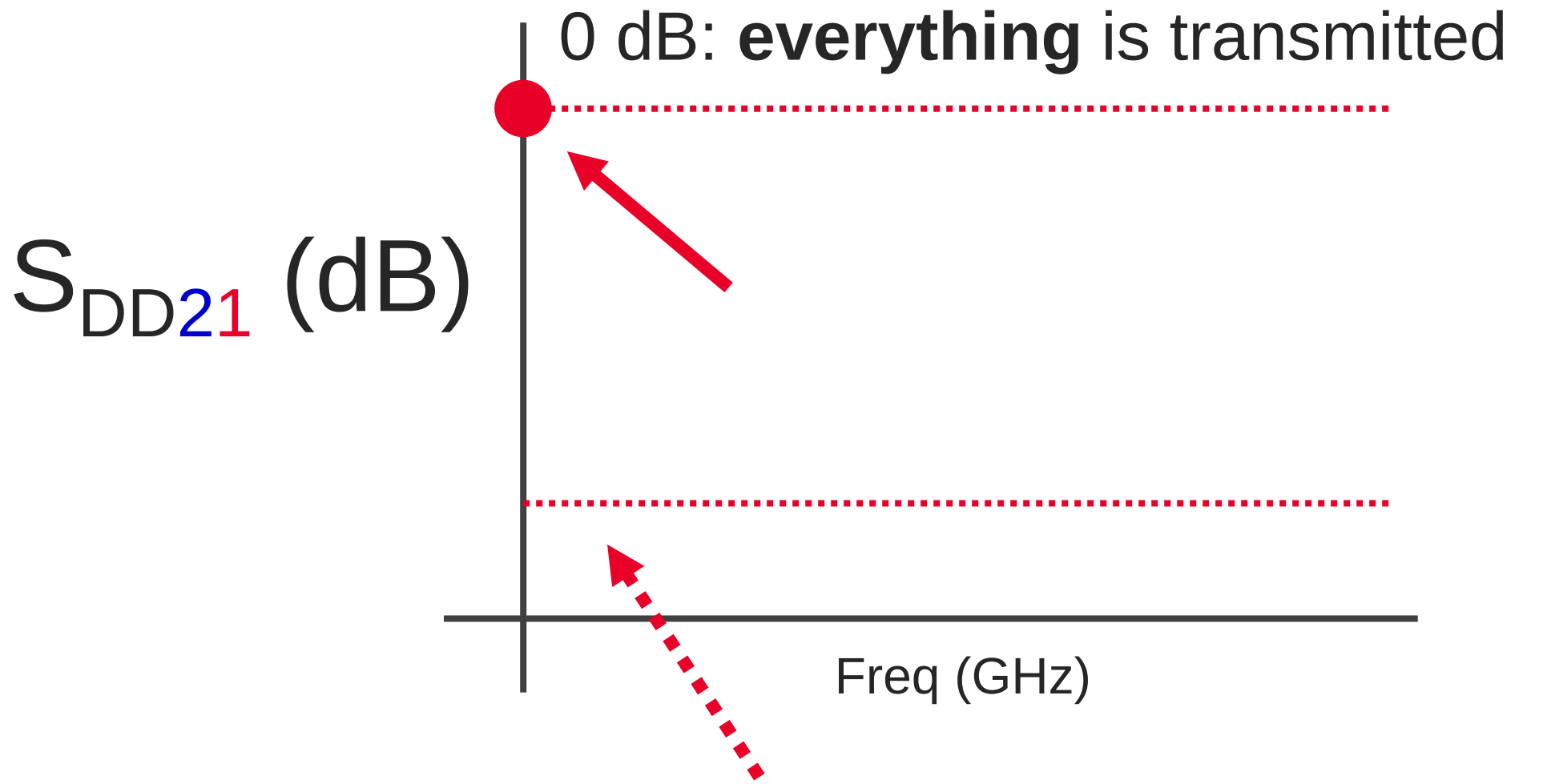
Quick Definition of S_{DD21}

At the low frequency, interconnects are **transparent**.

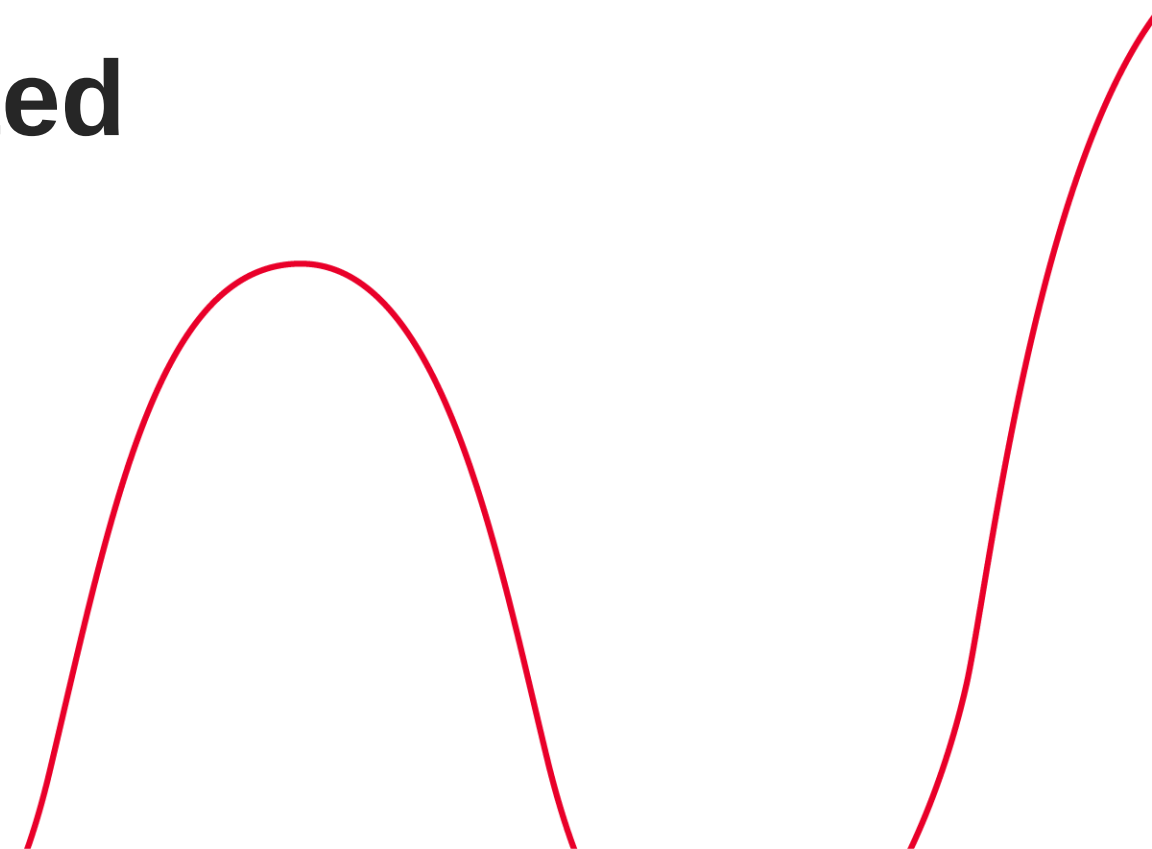


Expect S_{DD21} to be at 0 dB at Low Frequency

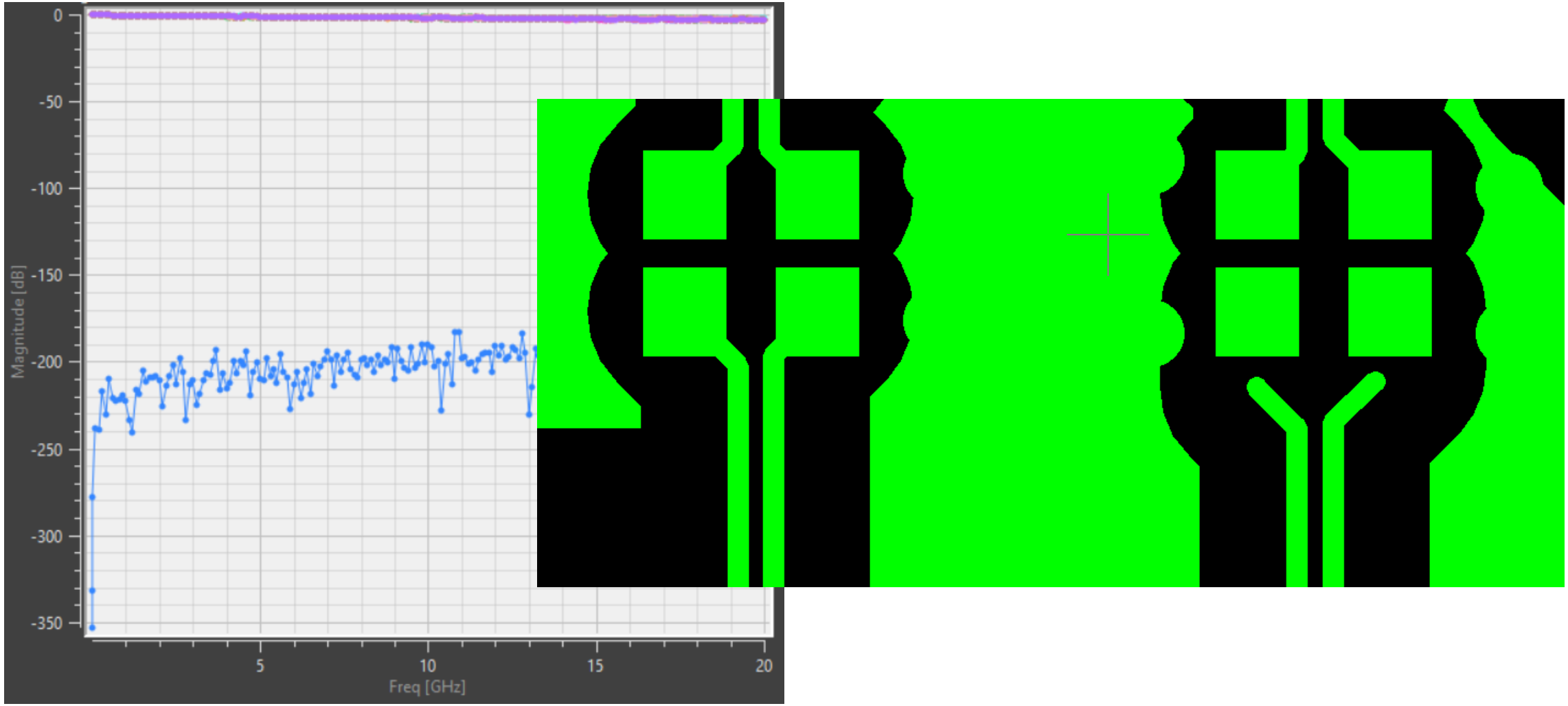
At the low frequency, interconnects are **transparent**.



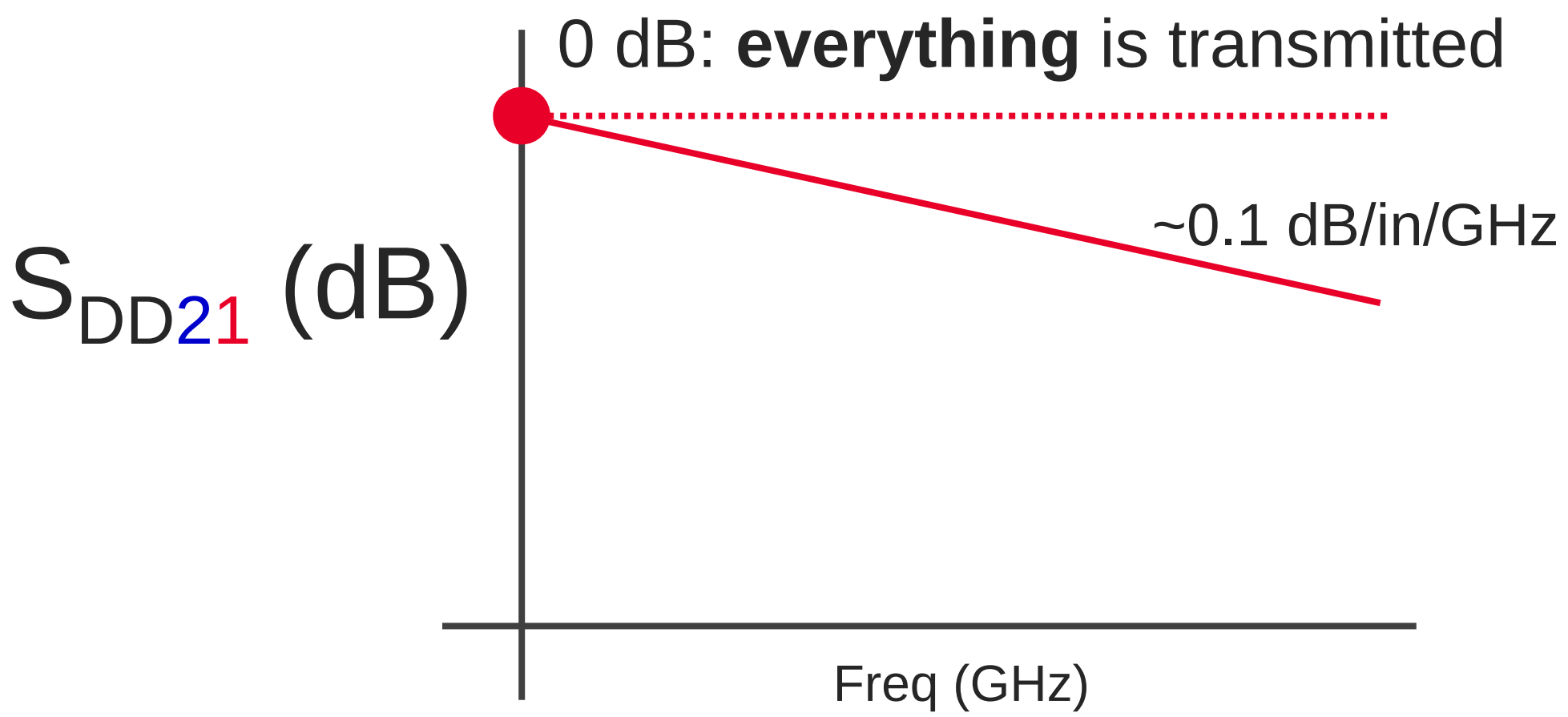
Demo: S_{DD21} is unexpected



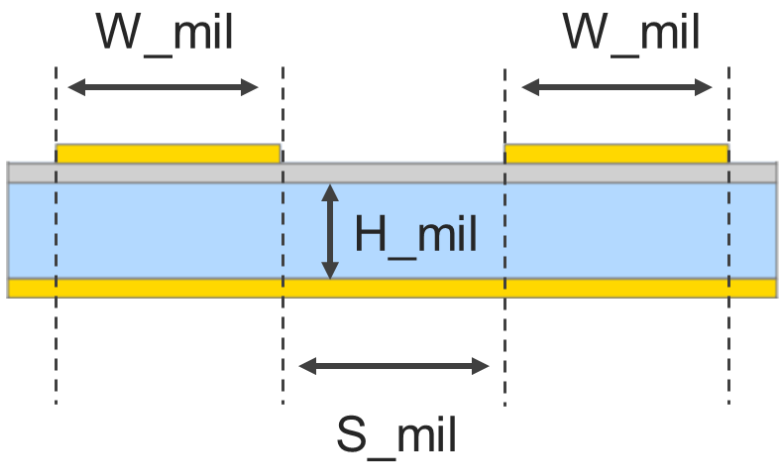
Fix Connection to Resolve Unexpected S_{DD21}



Expect S_{DD21} to Scale with ~0.1dB/in/GHz at Higher Frequencies



Summary



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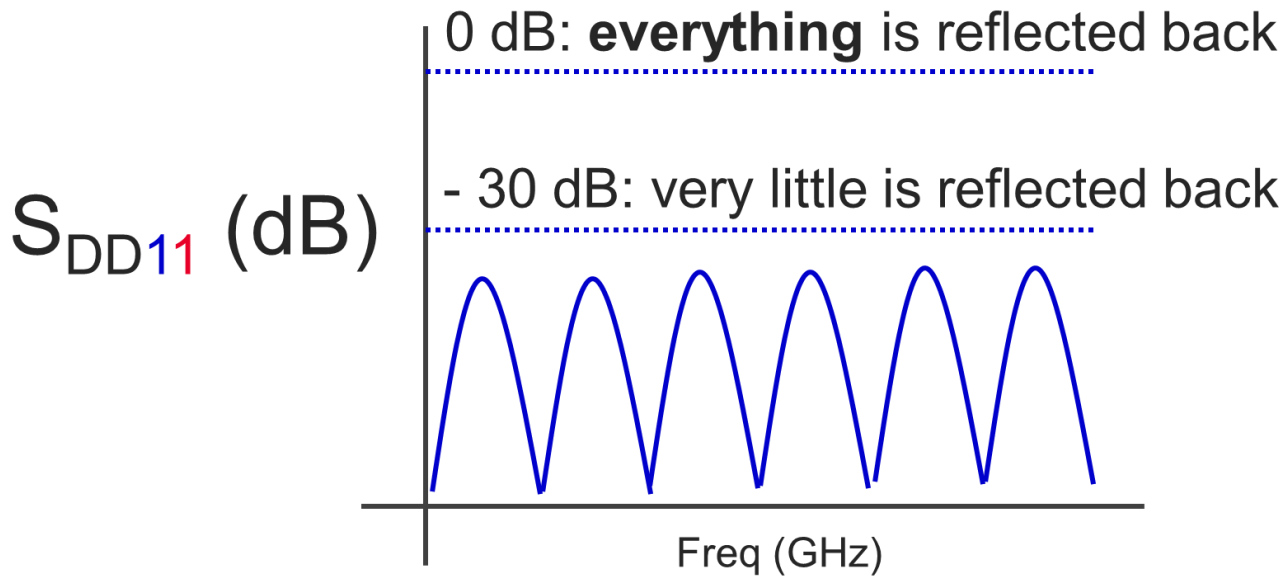
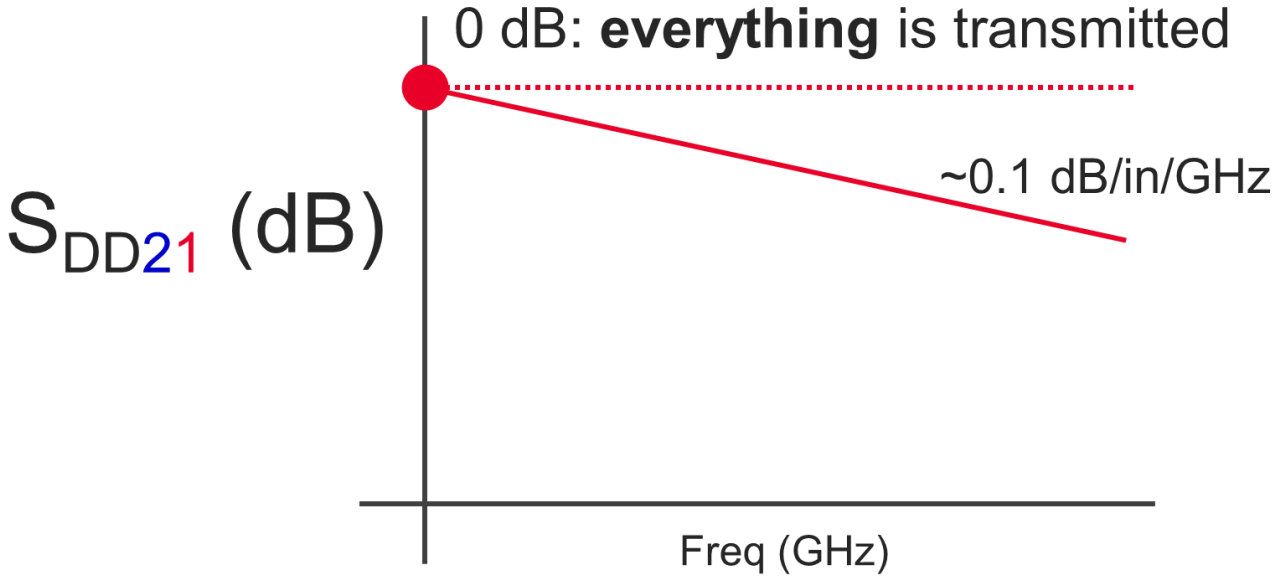
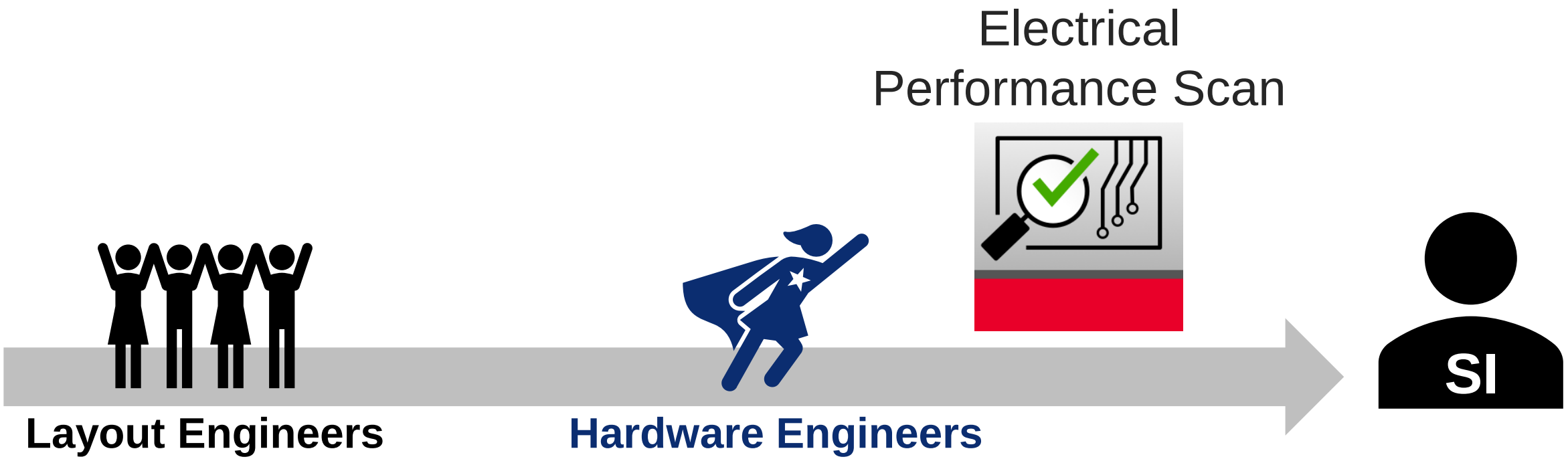




Electrical Performance Scan Empowers Hardware Engineers



- Gain more insights
- Increase productivity
- Reduce time to market

KEYSIGHT

Thank you