

Keysight Talks Standards: USB4 Version 2.0

Ben Miller, Product Marketing Manager
Jit Lim, USB Solutions Program Manager

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Thunderbolt[™] is a trademark of Intel Corporation

Jit Lim

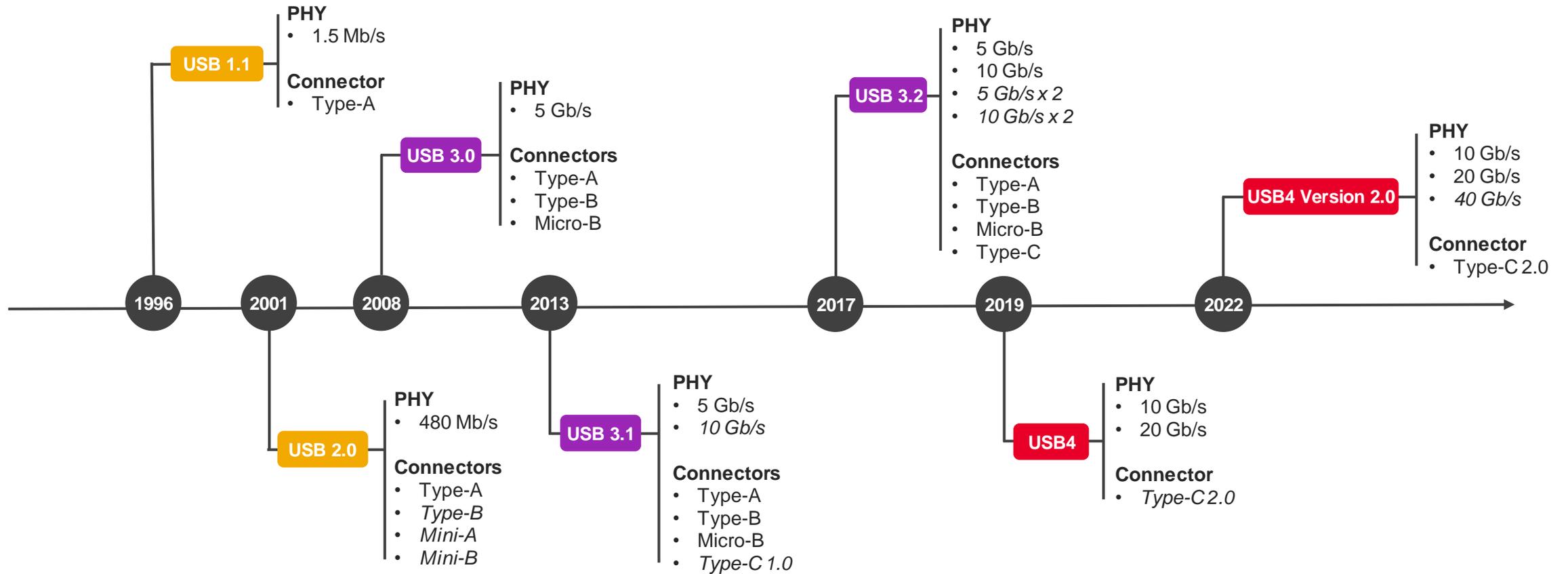
USB Solutions Program Manager
Keysight Network & Data Centers Solutions

BSEE, Massachusetts Institute of Technology
Executive MBA, University of Texas at Dallas



History of Universal Serial Bus

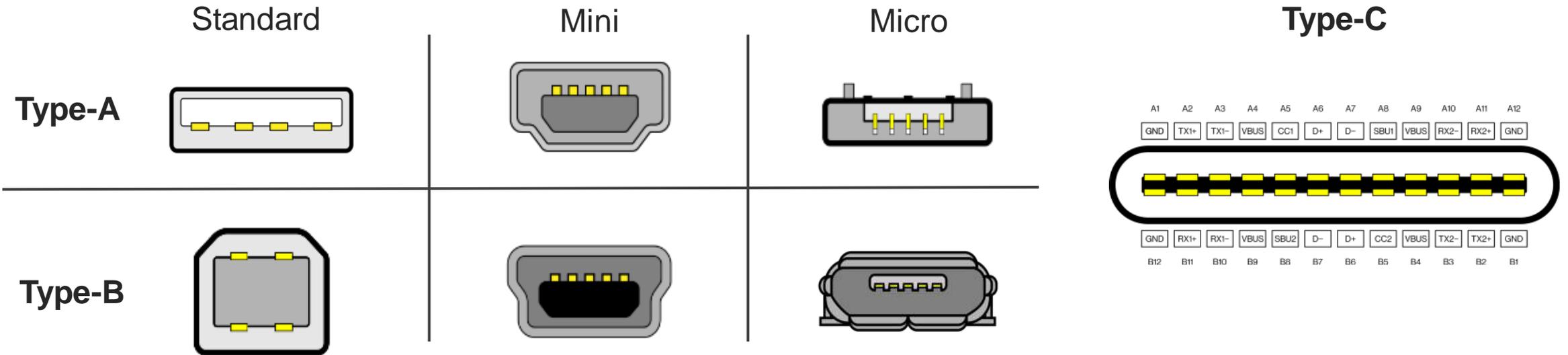
Signaling and Connectors



• *New additions*

USB Type-C Connector

Signaling protocol vs connector types



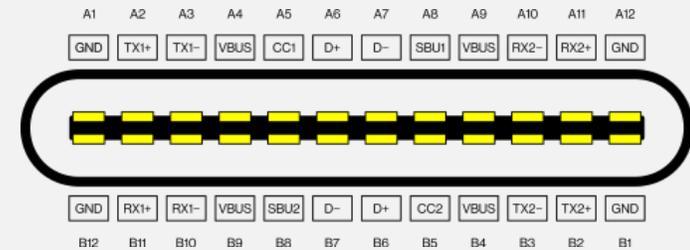
USB Type-C Connector

A more universal connector

Benefits of the Type-C connector:

- Smaller
- Reversible
- Supports higher speeds
- Supports USB power delivery
- Supports alternate mode protocols
 - DisplayPort
 - Thunderbolt
 - HDMI

Type-C



USB Implementers Forum

- Member companies determine how to make USB faster
- Releases specifications and compliance test specification (CTS)
- USB products need certification per CTS
- Companies producing USB products are part of the USB-IF

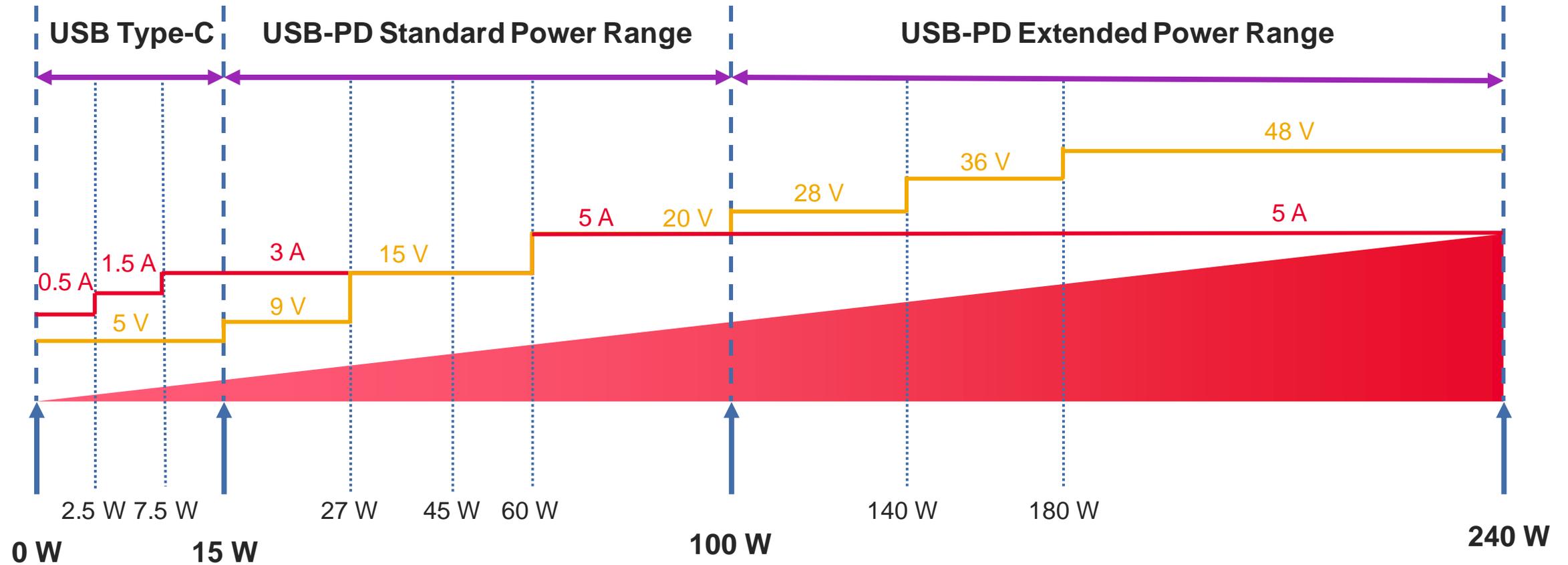


What's New in USB4 Version 2.0?

| Specification | USB4 | USB4 Version 2.0 |
|----------------------|------------|------------------|
| Aggregated Data Rate | 40 Gbps | 80 Gbps |
| # of Lanes | 2 Tx, 2 Rx | 2 Tx, 2 Rx |
| Lane Data Rate | 20 Gbps | 40 Gbps |
| Branding | USB 40Gbps | USB 80 Gbps |
| Baud Rate | 20 GBd | 25.6 GBd |
| Signaling | NRZ | PAM3 |
| Connector | Type-C | Type-C |

USB Power Delivery

Levels of Power over Type-C



Why PAM3?

Trade-off between bandwidth and noise

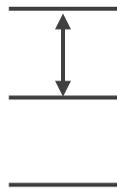
- Why did USB-IF decide to use PAM3?
 - Vertical noise margin issues with PAM4
 - Low-cost consumer cables are lossy and noisy
 - PAM3 allows for trade-off between higher bandwidth and noise margin
 - Technologies using PAM4 use more expensive hardware, less concern about noise margin

NRZ / PAM2



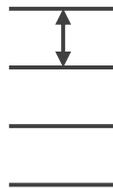
Bits/symbol = 1
Noise margin = 1

PAM3

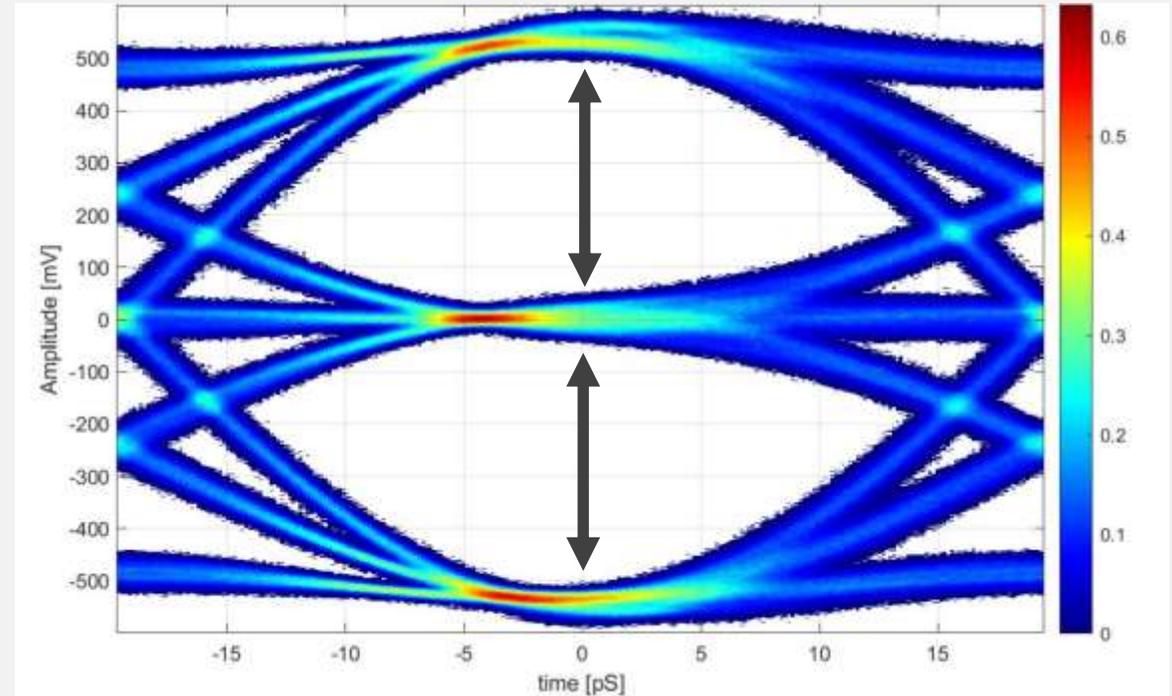


Bits/symbol = 1.57
Noise margin = 0.5

PAM4



Bits/symbol = 2
Noise margin = 0.33



PAM3

Let's do the math

PAM4

$$20 \text{ Gbaud PAM4} = 40 \frac{\text{Gigabits}}{\text{second}}$$

PAM3

$$25.6 \text{ Gbaud PAM3} = 25.6 \frac{\text{Gigatrits}}{\text{second}}$$

$$1 \text{ trit} = \log_2(3) \text{ bits} = \sim \frac{11}{7} \text{ bits}$$

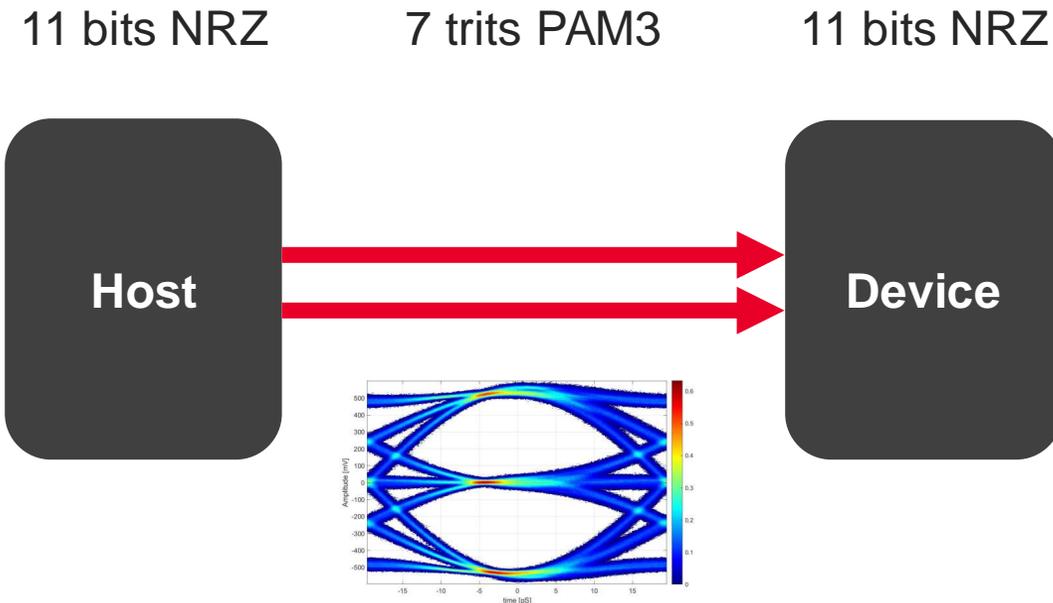
$$\left(25.6 \frac{\text{Gigatrits}}{\text{second}} \right) * \left(\frac{11}{7} \frac{\text{bits}}{\text{trit}} \right) = 40 \text{ Gbps}$$

$$2 \text{ lanes} * 40 \text{ Gbps} = 80 \text{ Gbps}$$

PAM3

Let's do the math

PAM3 Encoding



PAM3

$$25.6 \text{ Gbaud PAM3} = 25.6 \frac{\text{Gigatrits}}{\text{second}}$$

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PAM3

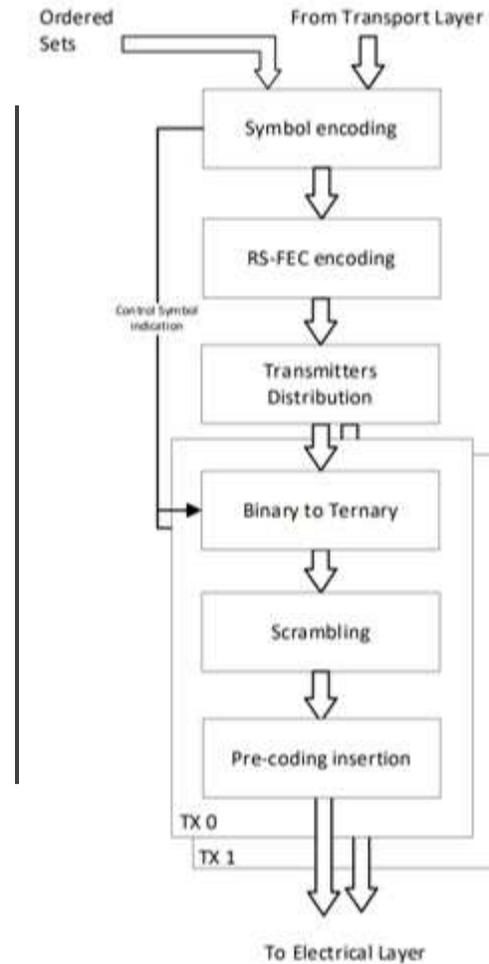
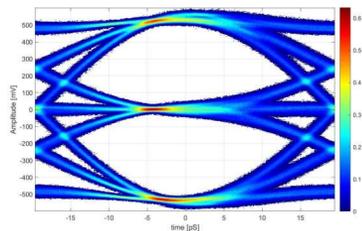
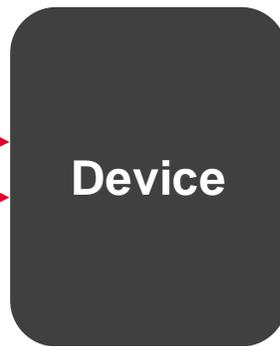
Let's do the math

PAM3 Encoding

11 bits NRZ

7 trits PAM3

11 bits NRZ



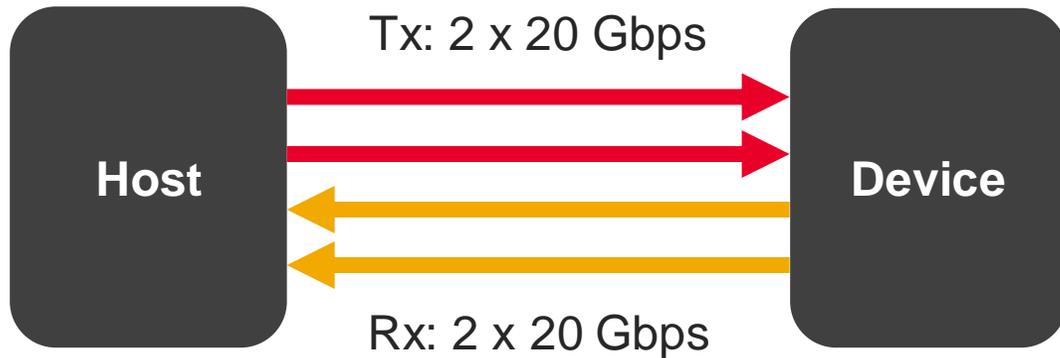
Encoding Efficiency

$$\frac{2^{11}}{3^7} = \sim 97\%$$

Asymmetric Channels

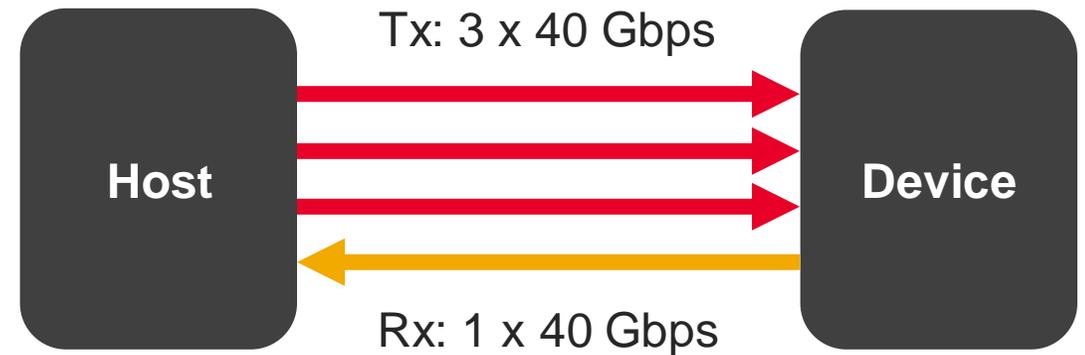
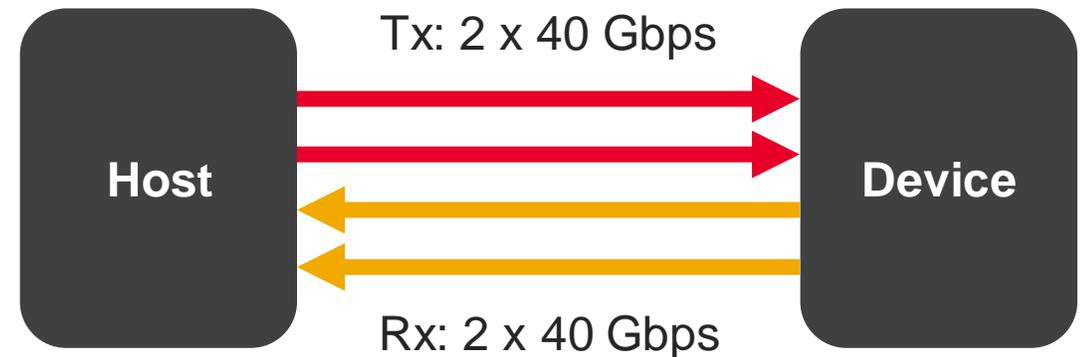
How USB4 Version 2.0 supports up to 120 Gb/s

USB4



Symmetric

USB4 Version 2.0



Asymmetric

Test Challenges

What's going to be harder about USB4 Version 2.0

Higher speeds

- 20 GBd to 25.6 GBd not much faster, but speeds can make testing difficult
- Oscilloscopes need a higher sampling rate (>80 Gs/s), higher bandwidth (>25 GHz), and intrinsic noise removal
- Cable and connector testing will not change; current designs should work

Multi-level signaling

- Noise margin for PAM3 is half of NRZ
- BERTs need to generate PAM3 signals
- Oscilloscopes need software to analyze PAM signals

Increasing Complexity of the Link

Design simulation is more important than ever



Transmitter

USB 3.2

- 1 Feed-forward Tx EQ

USB4

- 16 EQ presets

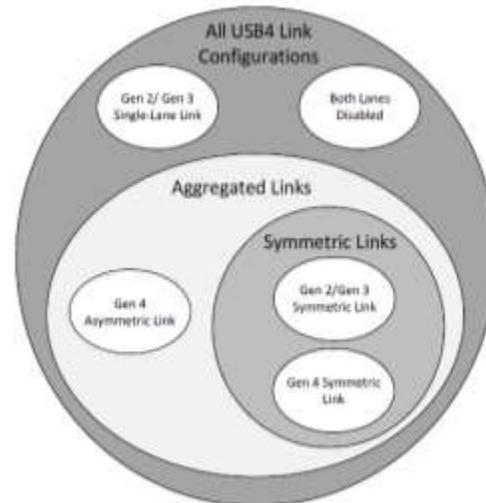
USB4 Version 2.0

- 42 EQ presets to characterize and optimize

Channel

Multiple Type-C Cable Types

- Passive cables
- Active cables
- Retimer/redriver (LRD) cables



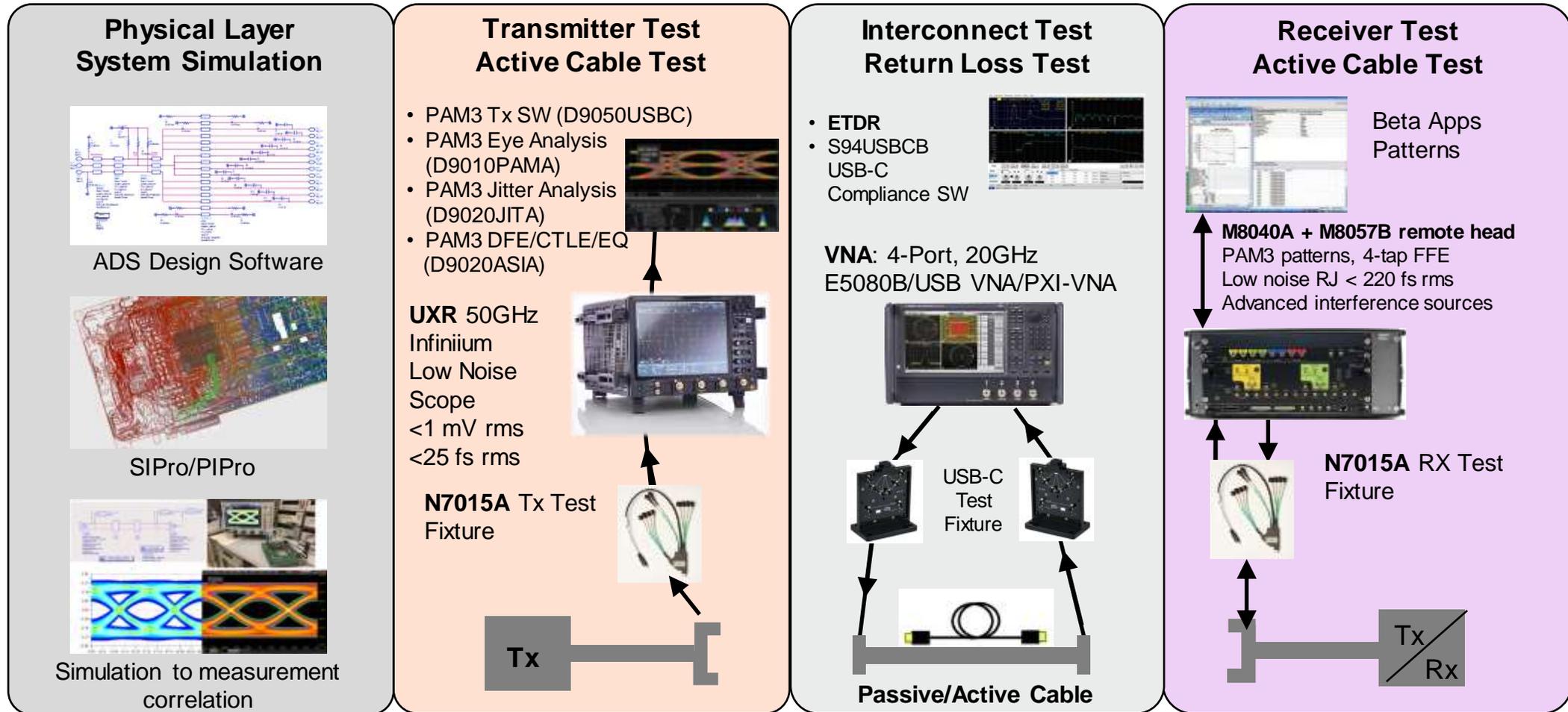
Receiver

New Receiver Considerations

- Gain
- Clock recovery
- Filtering
- DFE, CTLE
- Forward error correction

Keysight USB4v2 Test Solutions at Spec Release

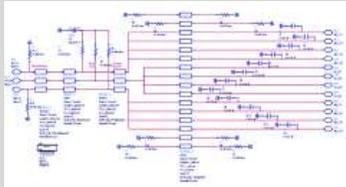
Design simulation, protocol decode, live link debug, USB-PD, RF, channel characterization



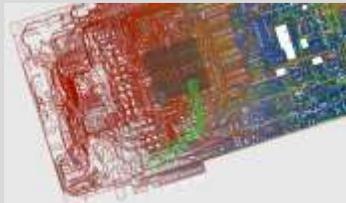
Design Simulation Solutions

Keysight Design Solutions for the Whole Product Development Cycle

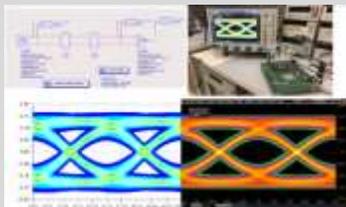
Physical Layer System Simulation



ADS Design Software

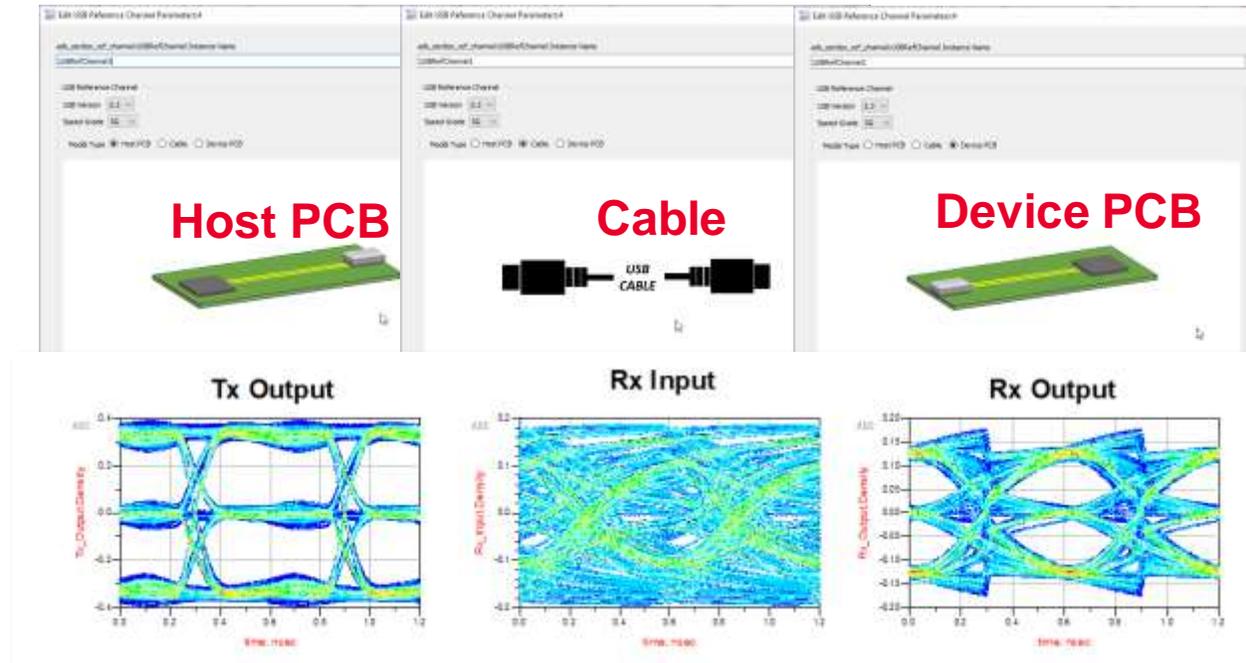


SIPro/PIPro



Simulation to measurement correlation

- W3081E PathWave USB AMI Model Builder
- USB4v2 Reference Channels and Simulation in PathWave ADS



Transmitter, Receiver, and Cable Test Solutions

Keysight Test Solutions for the Whole Product Development Cycle



Transmitter

UXR-Series Oscilloscope

- ≥ 25 GHz, 2 channel scope

Test Software

- D9050USBC USB4v2 automated compliance test SW with SigTest
- D9010PAMA PAM3 analysis SW
- D9120JITA jitter analysis SW
- D9120ASIA advanced signal integrity SW



Channel

Connector and Cable Test

- 4-port, 20 GHz E5080B Vector Network Analyzer
- S94USBCB USB-C cable compliance software
- N7015A USB-C test fixture

Active Link Solutions

- N7019A active link fixture
- D9010USBP USB protocol decode/trigger software



Receiver

M8040A PAM3 BERT

- Pattern generator and error detector
- TX FFE preset table
- Symbol error injection

N5991U42A Rx calibration and automated test software

M8195A AWG

- CM and DM interference
- Advanced SSC modulations

Transmitter, Receiver, and Cable Test Solutions

Other considerations



- Simulation and measurement correlation
- USB power delivery and Alt Mode testing and compliance
- Backwards compatibility (USB 2.0, USB 3.2)
- Automated test software saves time, ensures repeatability

Keysight Value

Partner with test and measurement experts on your
USB development journey

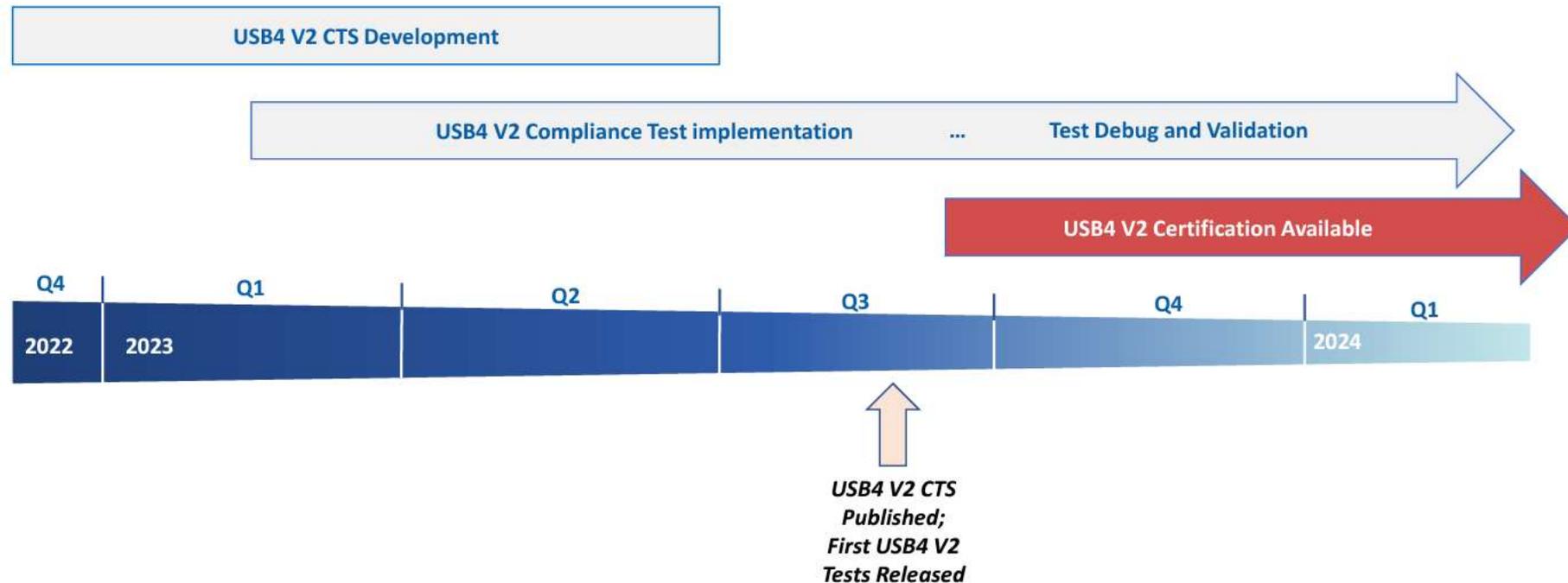
Keysight experts:

- Guide customers through test challenges
- Understand tools and solutions
- Help interpret results and debugging
- Understand new standards and measurement science

USB4 Version 2.0 Timeline

When can USB 80 Gbps products get certified?

- Pathfinding for USB4 Version 2.0 began in 2017
- Specification released in October 2022



Survey

Please take a moment for this survey

We appreciate your feedback on today's event...

How would you rate the overall technical content of this webinar?



Challenge: Test Run Time Optimization

Case Study: DisplayPort



Full Characterization

Four data rates, four lanes
SSC enabled/disabled

Signal Acquisition

DUT configuration
Signal conditioning

Measurements

Equalization
Jitter decomposition
Eye diagram

What is it costing you?

- Extensive test plan requires long test time
- 75% of test time is spent processing data

What is an ideal solution?

- Significant test time improvement
- Re-use of your invested solution
 - Saves \$\$\$
 - Builds on your present equipment and knowledge

Solutions

1) Sequential

- Traditional use model
- What you use today



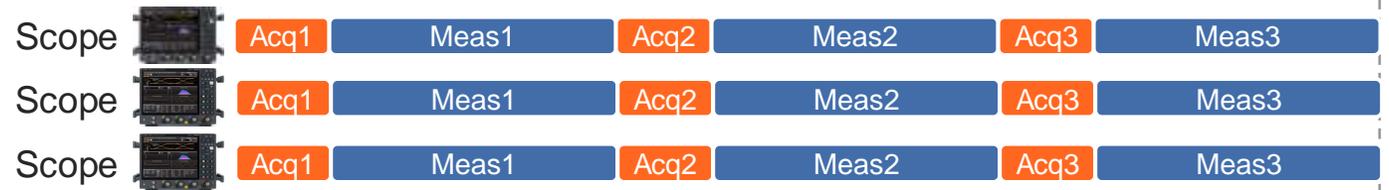
2) Offline processing

- Better instrument usage
- No test time reduction



3) Parallel stations

- Parallel operations
- Takes \$\$\$ and space
- Cannot test same DUT



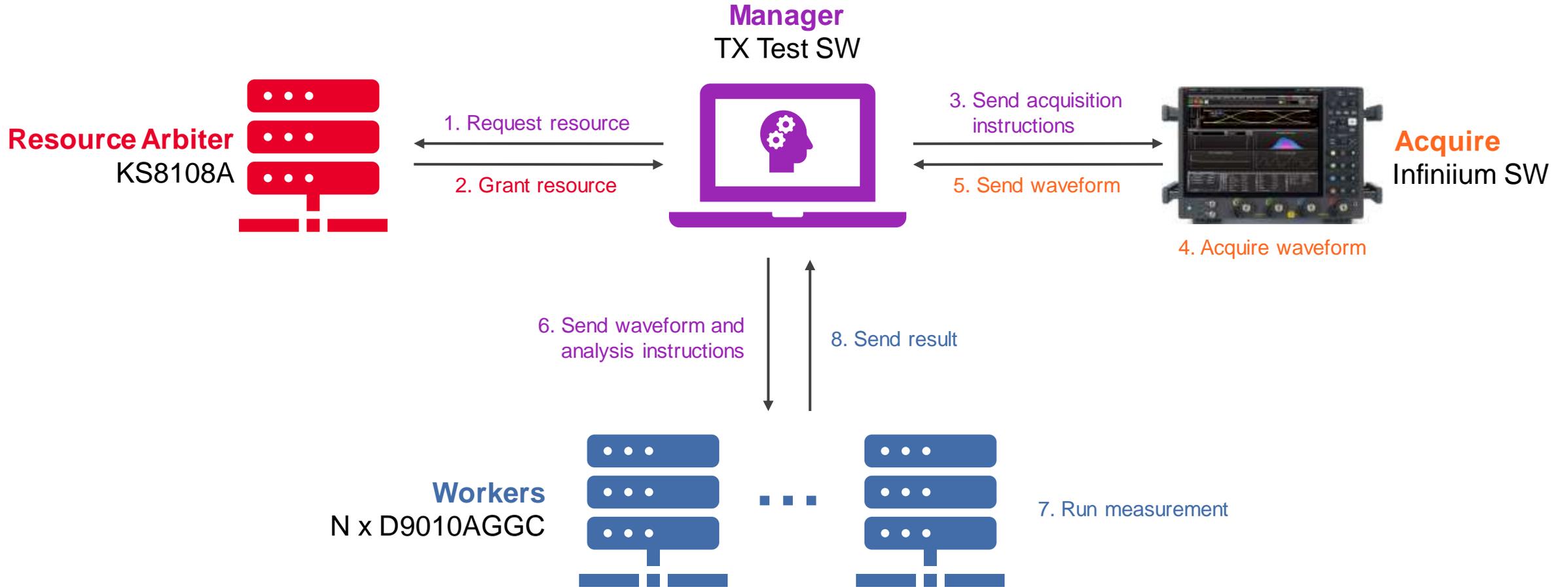
4) Measurement disaggregation

- Parallel operations
- Better instrument usage
- Test time reduction
- Very cost effective

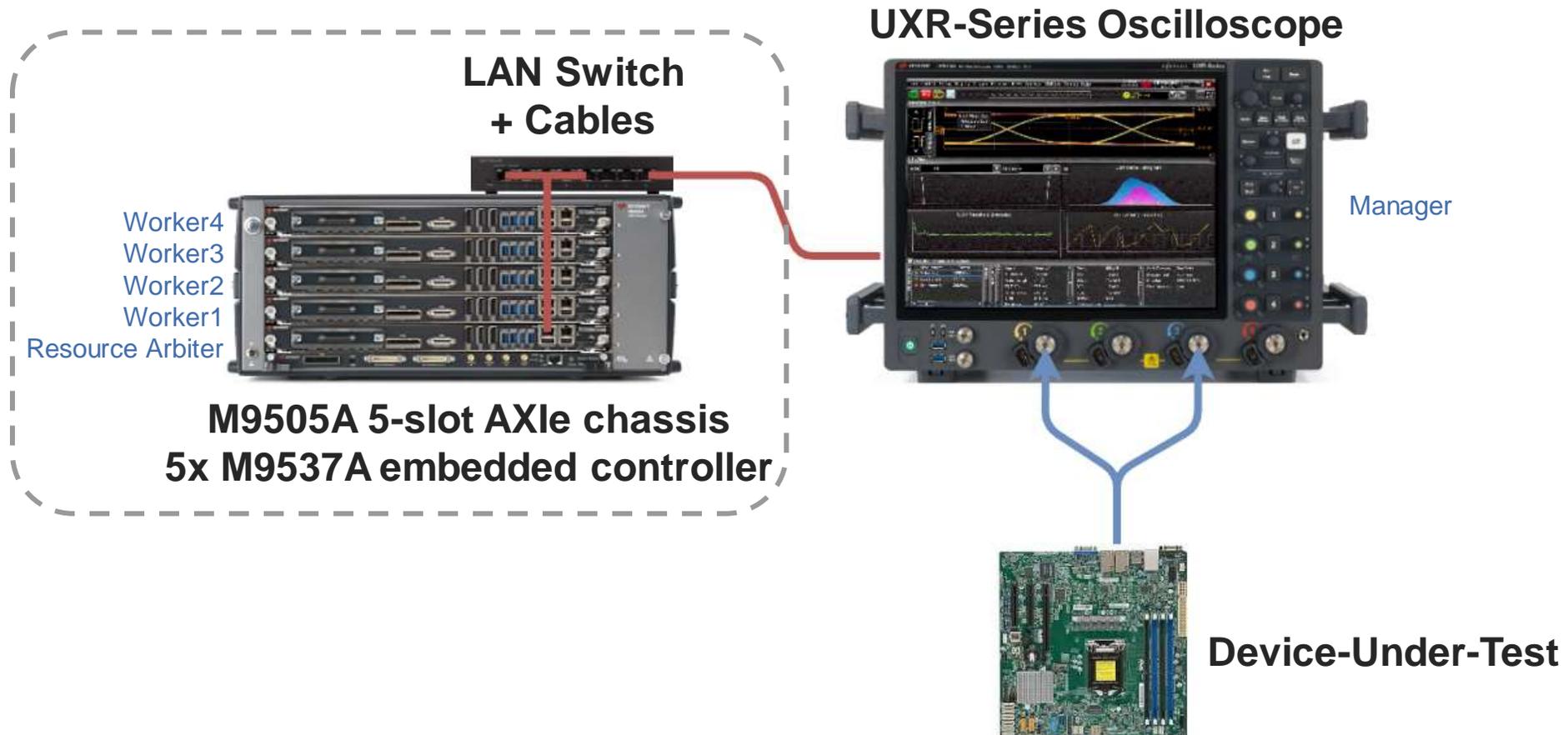


Measurement Disaggregation

Overview

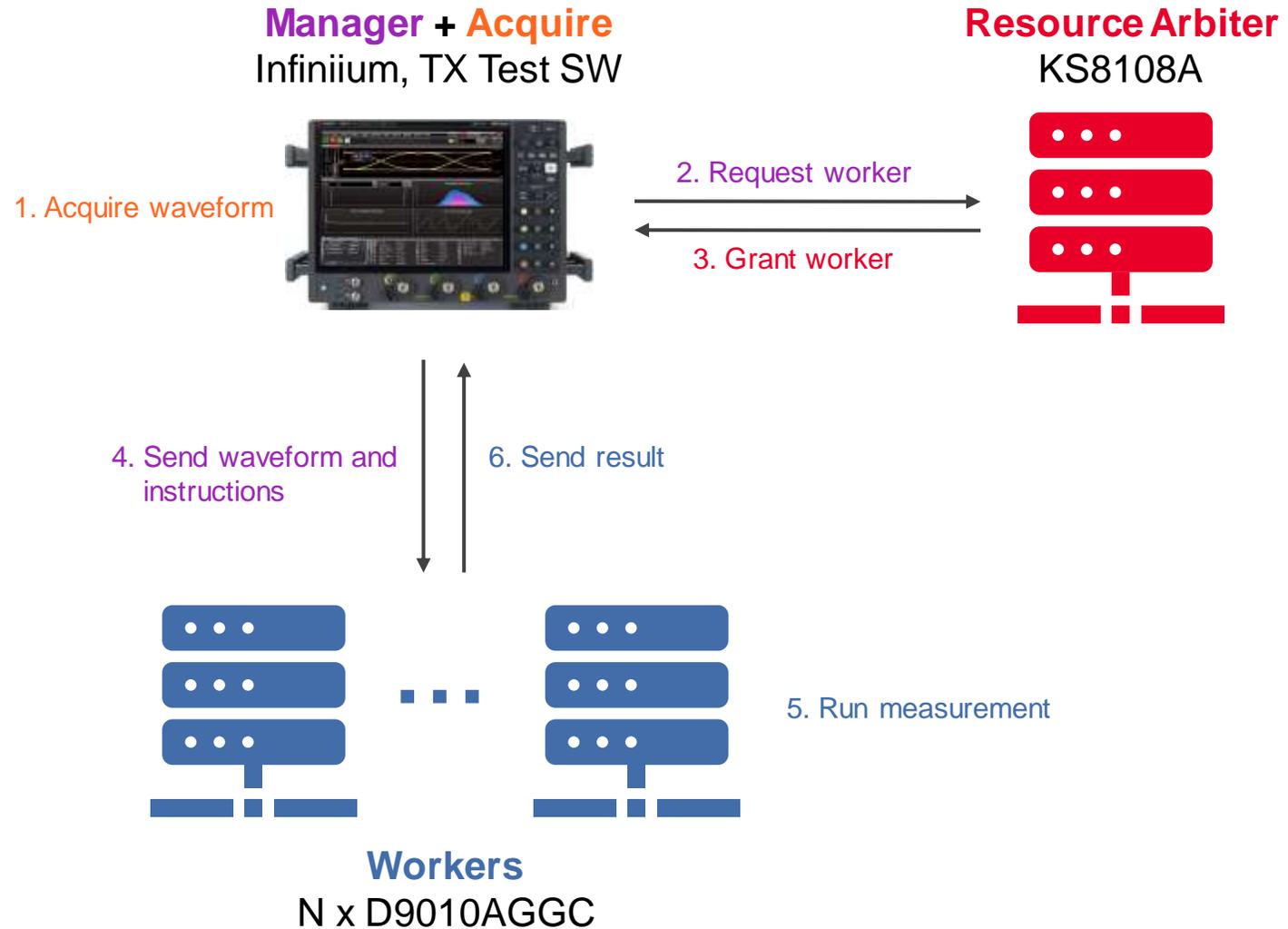


Disaggregation Compute Unit



Measurement Disaggregation

Common Setup



Price & Test Time vs Number of Workers

Case study: DisplayPort



| # Workers | Additional SW Price | Test Time | Price Factor | Speed Factor |
|-----------|---------------------|-----------|--------------|--------------|
| 0 | \$0 | 5h 56min | 1 | 1 |
| 1 | \$24k | > 6h | 1.52 | <1 |
| 2 | \$44k | 3h 10min | 1.96 | 1.87 |
| 3 | \$64k | 2h 14min | 2.39 | 2.66 |
| 4 | \$84k | 2h 01min | 2.82 | 2.94 |

Notes

Test duration based on internal benchmarks.
Setup with one worker has never been tested (not relevant).

SW Price

KS8108A + N * D9010AGGC, node-locked with 12-month Keysight Care
Assuming customer already owns D9040DPPC.

Thank you