

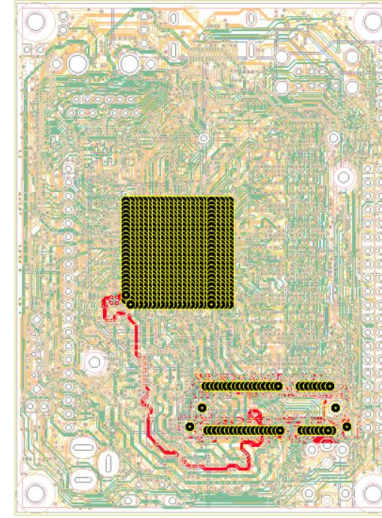
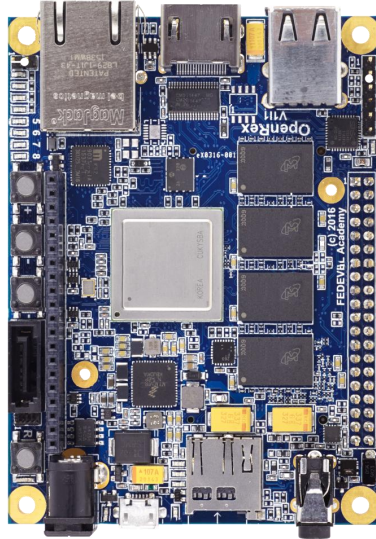
# From Fixing Today's PCIe Channels to Preparing for Tomorrow's Designs

[Your Name | Title]

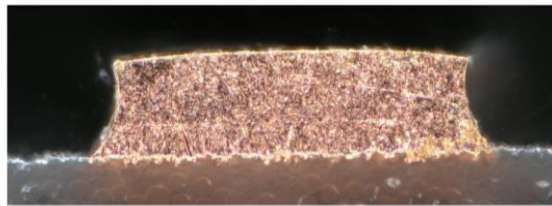
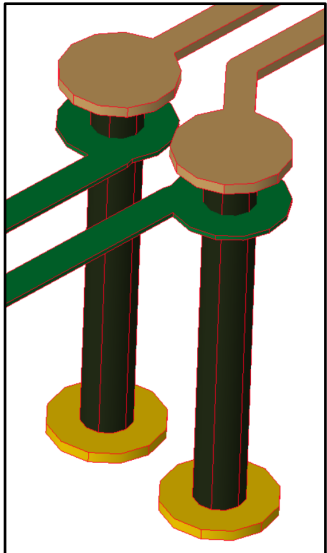
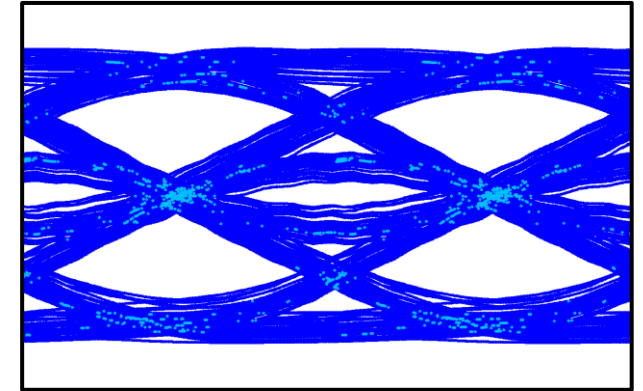
# Agenda



## PCIe Standard Overview

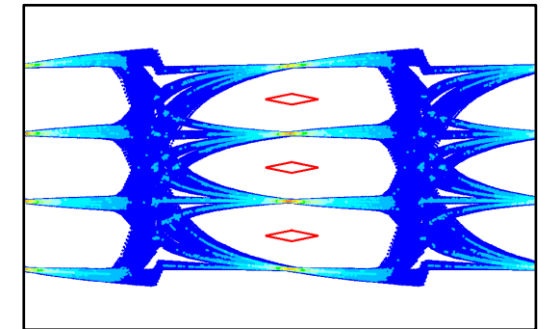
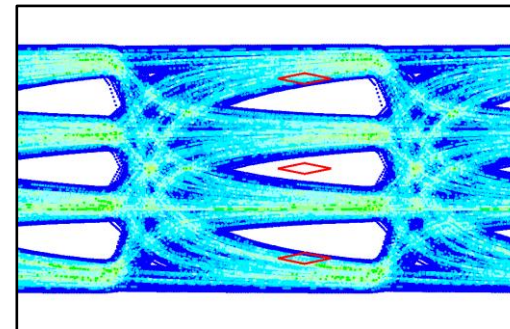


## Signal Integrity (SI) in Action A Broken PCIe Channel



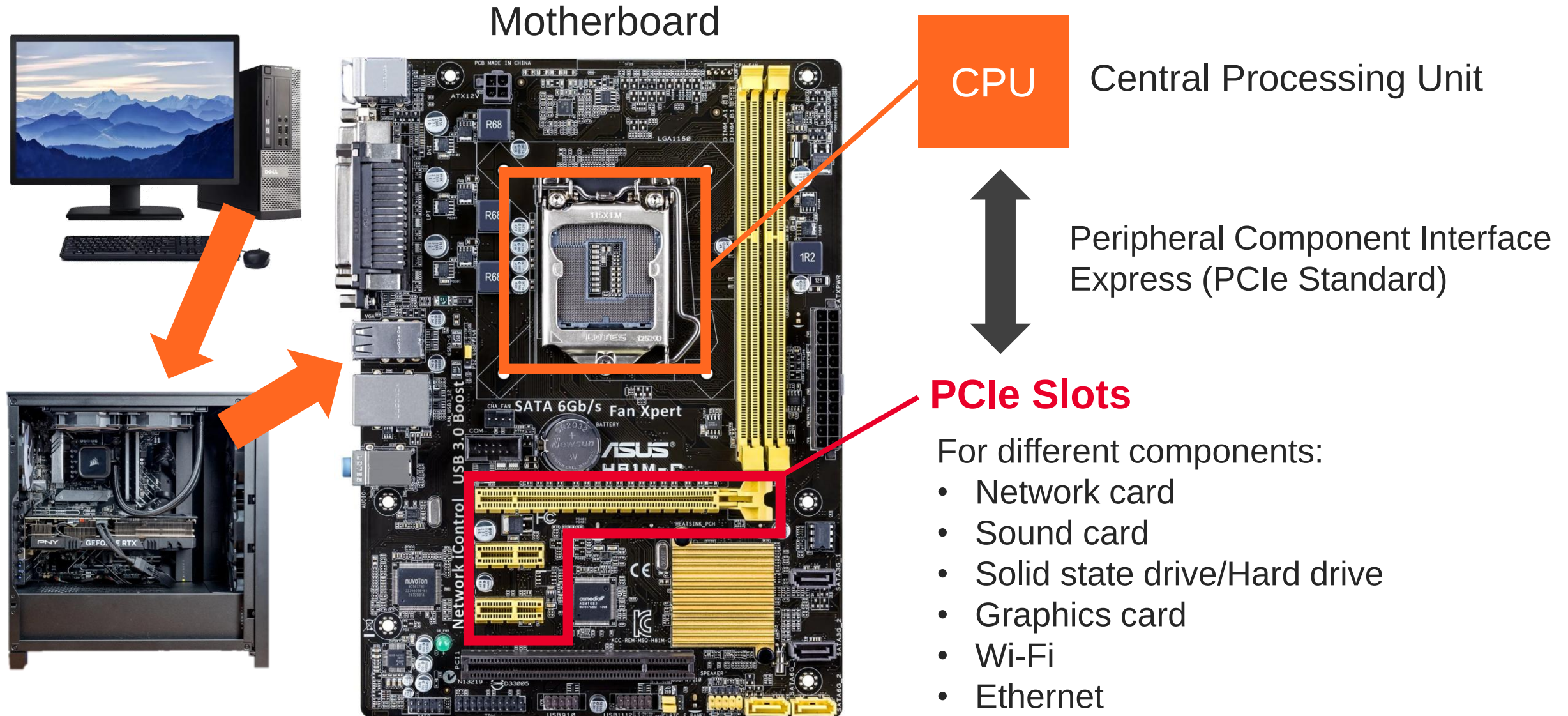
Causes of SI  
problems

## Design and Test PCIe 7 with Keysight



# PCIe Standard Overview

# PCIe Communicates between Components and the Motherboard



# Different Components for PCIe Expansions



A PCI Express 2.0 **x1** expansion card that provides USB 3.0 connectivity



Intel 82574L Gigabit Ethernet NIC, a PCI Express **x1** card



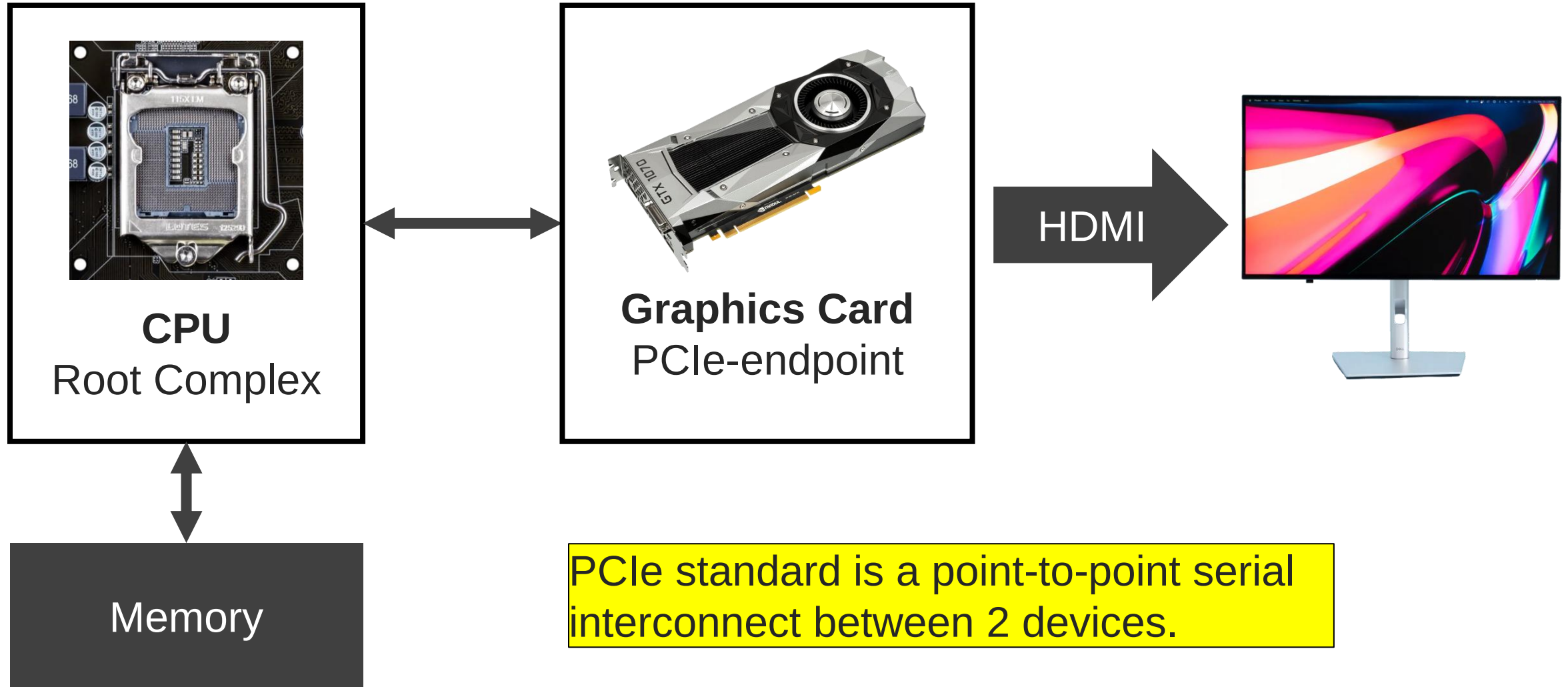
An OCZ RevoDrive SSD, a full-height **x4** PCI Express card



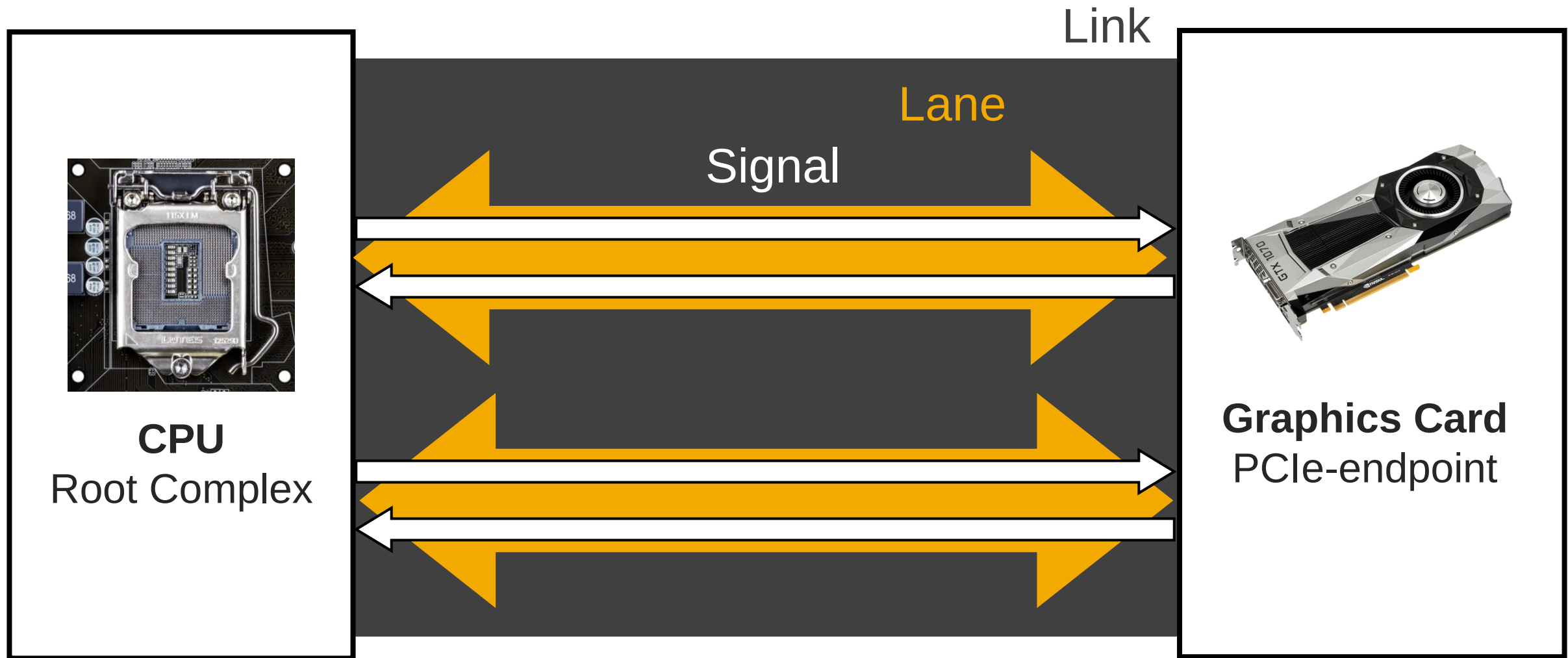
The Nvidia GeForce GTX 1070, a PCI Express 3.0 **x16** Graphics card

PCIe standard has a wide reach of applications

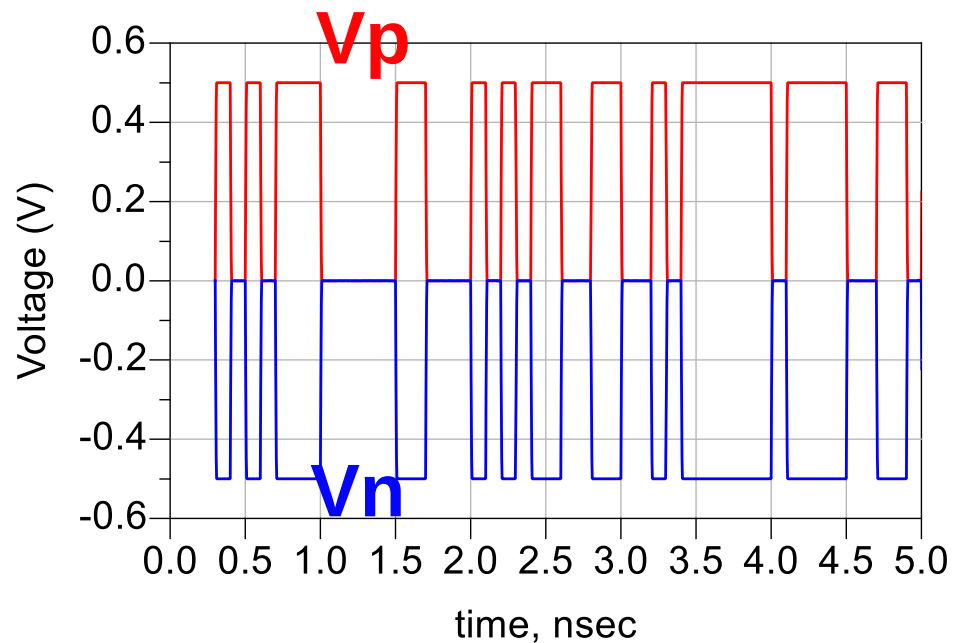
# Point-to-point Topology of the PCIe Standard



# Illustration of Link, Lane, and Signal



# PCIe Implements Differential Signaling

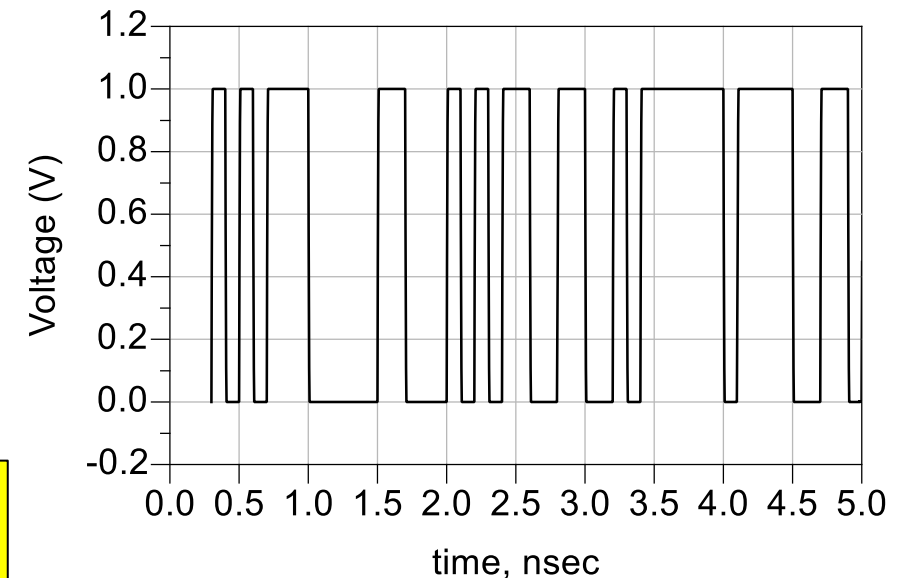


$$V_{RX} = V_p - V_n$$

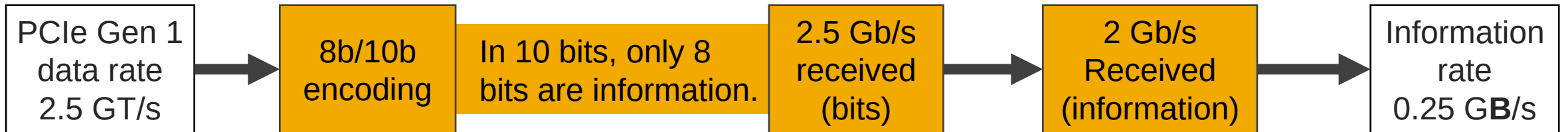
But why?

$$V_{RX} = (V_p + N) - (V_n + N)$$

Differential signaling reduces the noise in each of signal lines.

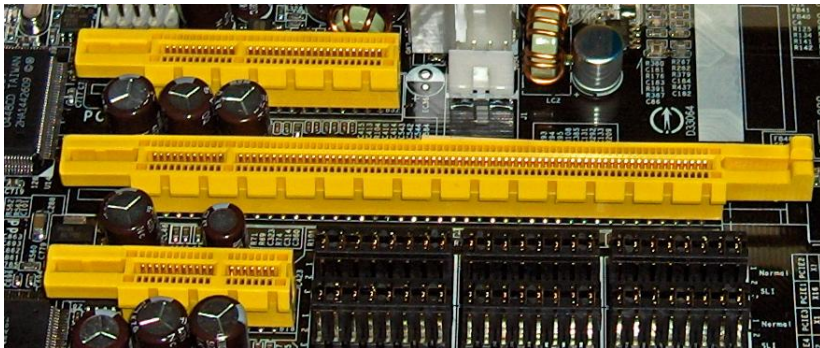


# PCIe Gen 1 Throughput (Usable Data) Calculation Example



$$2.5 * 0.8 = 2$$

8 bits per Byte



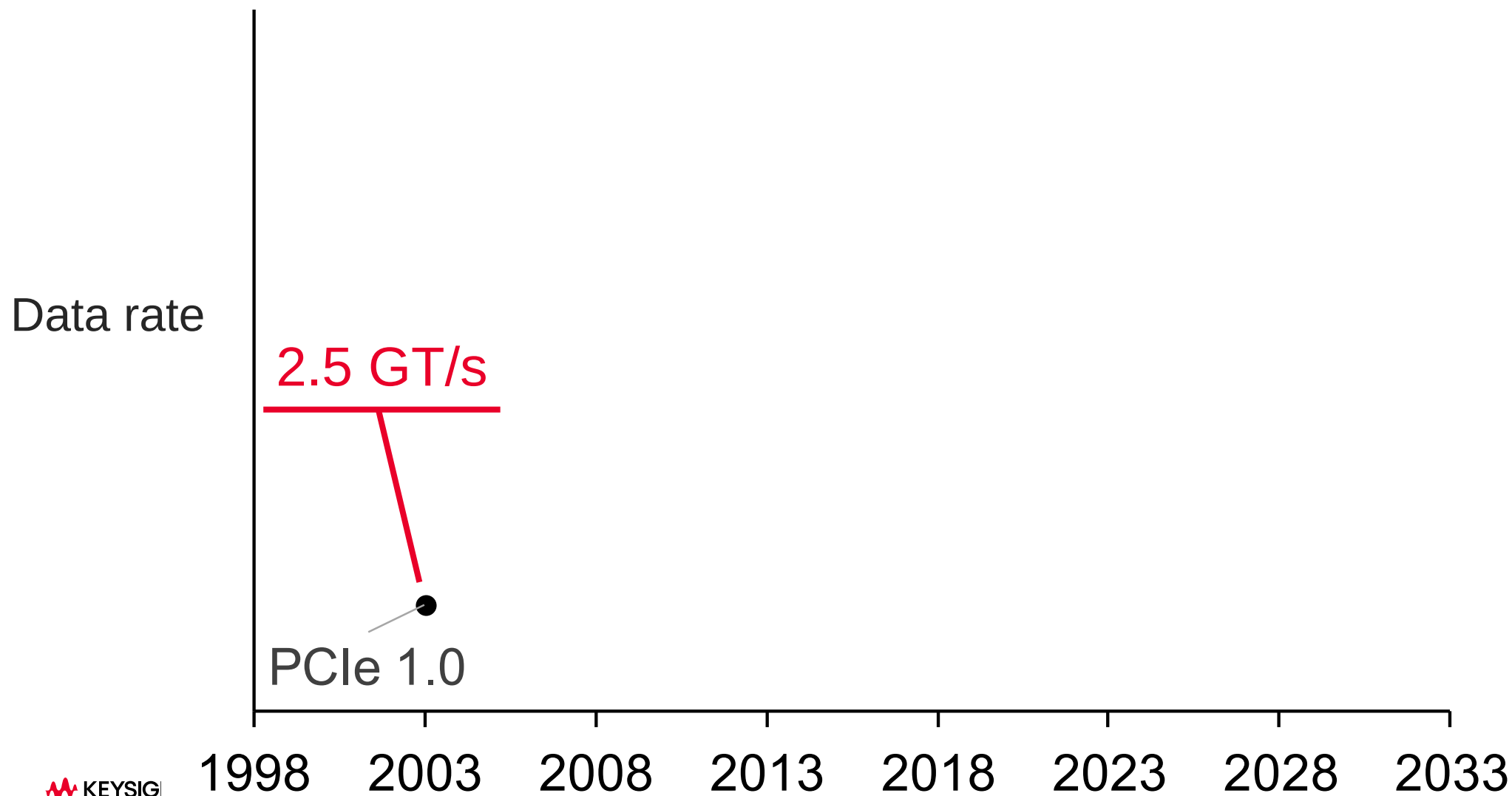
PCI Express x4

PCI Express x16

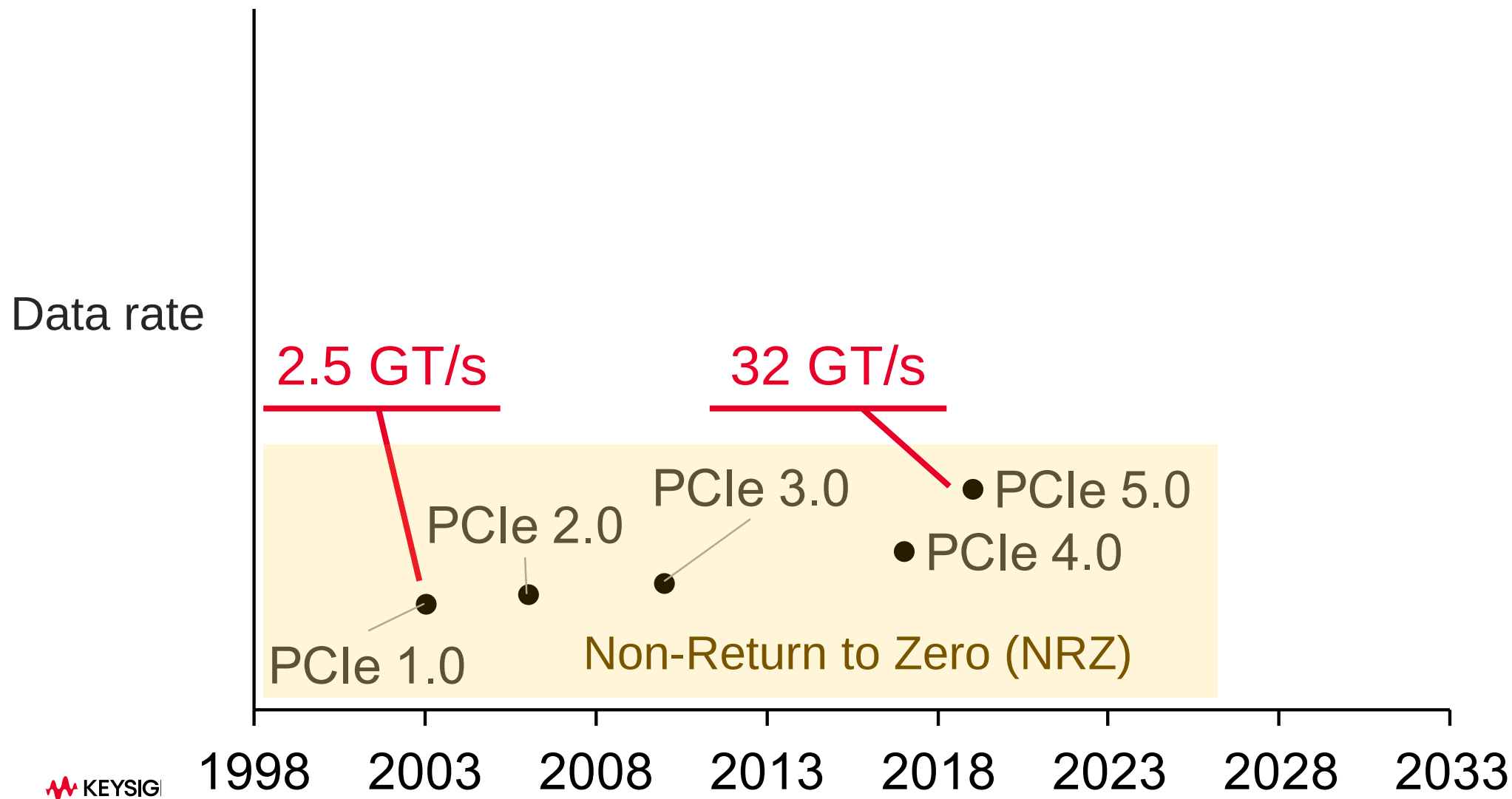
PCI Express x1

PCIe standard is backward compatible. All new standards have to work the Gen 1 at 2.5 GT/s

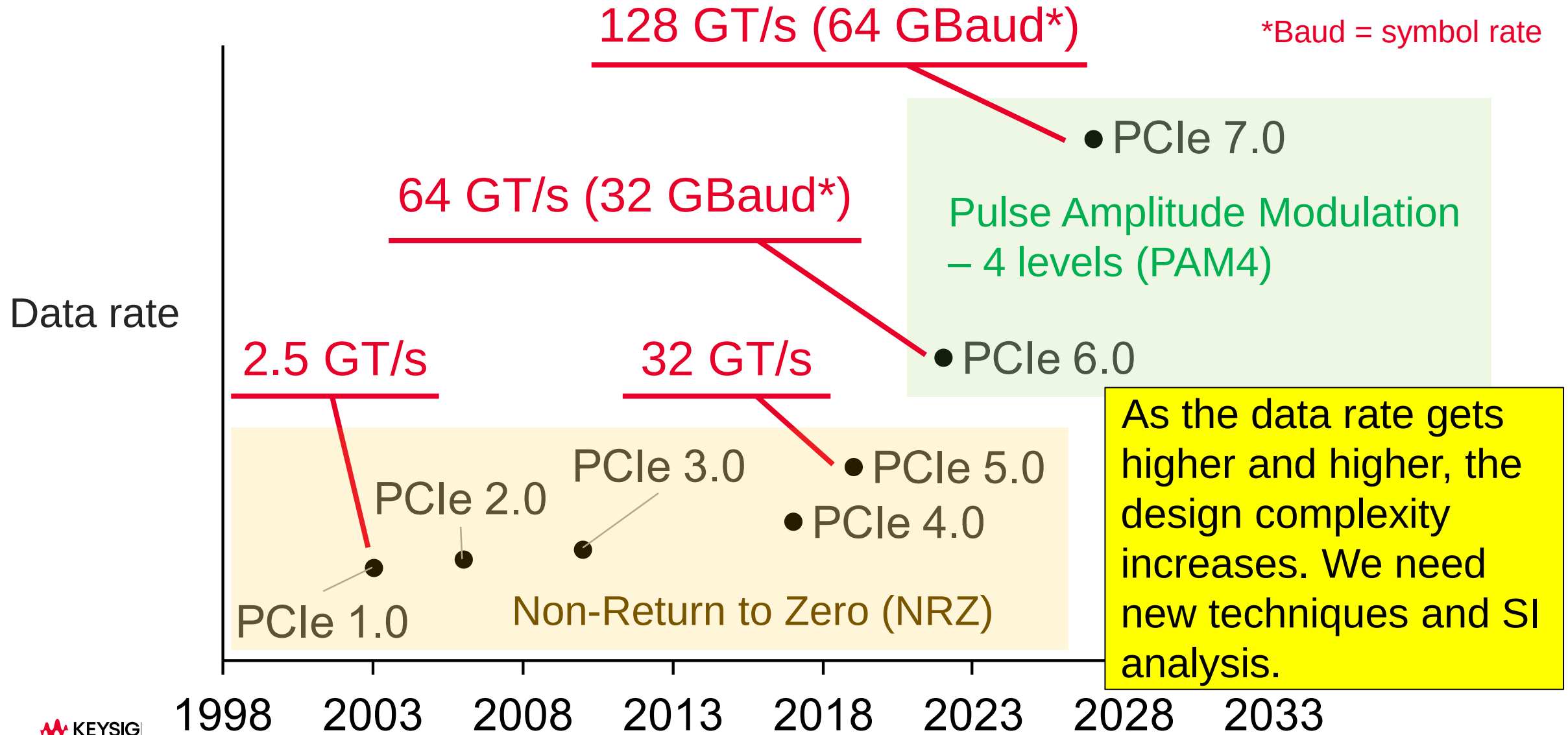
# SI is Important as Data Rate Increases Rapidly for PCIe



# SI is Important as Data Rate Increases Rapidly for PCIe

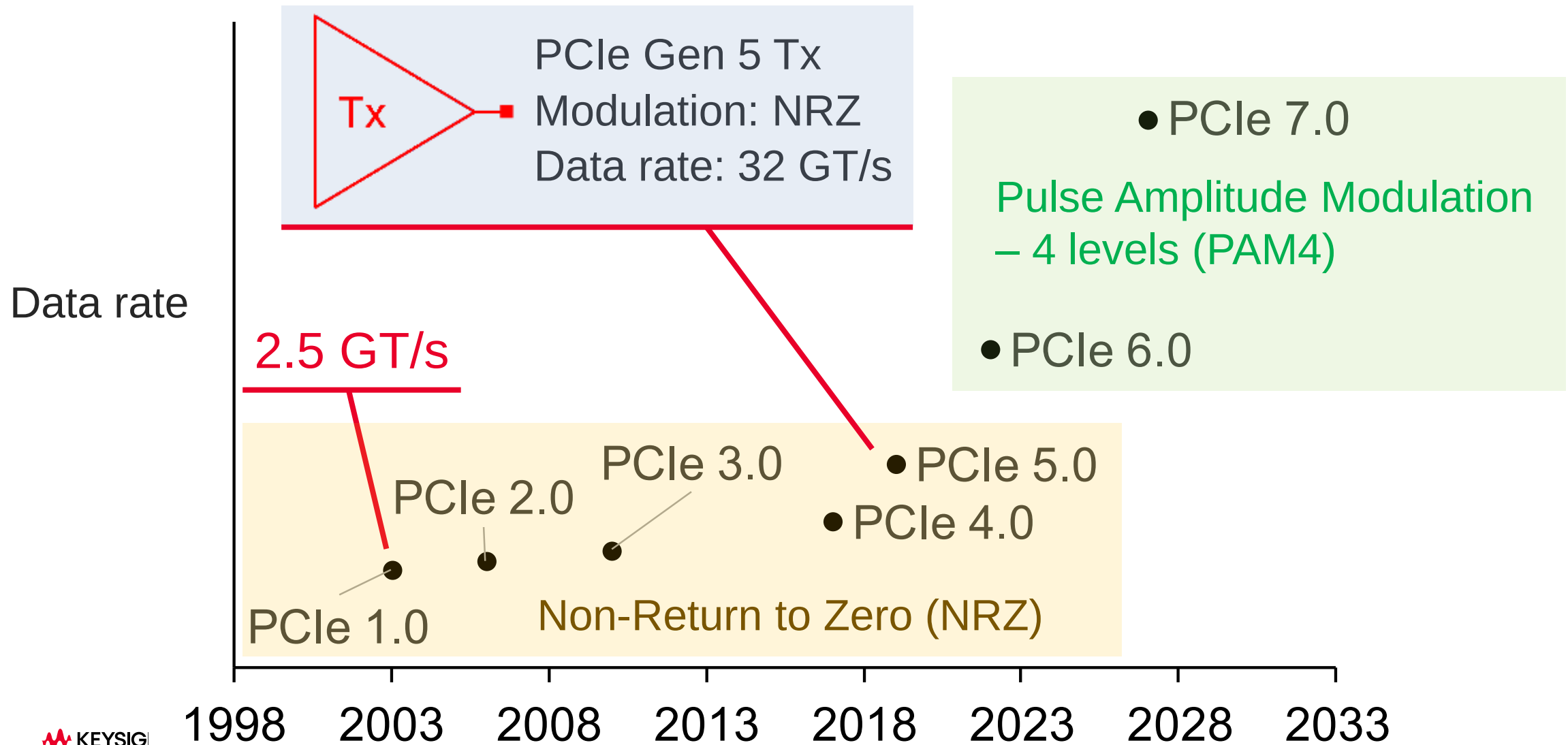


# SI is Important as Data Rate Increases Rapidly for PCIe

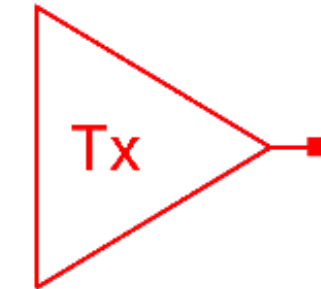
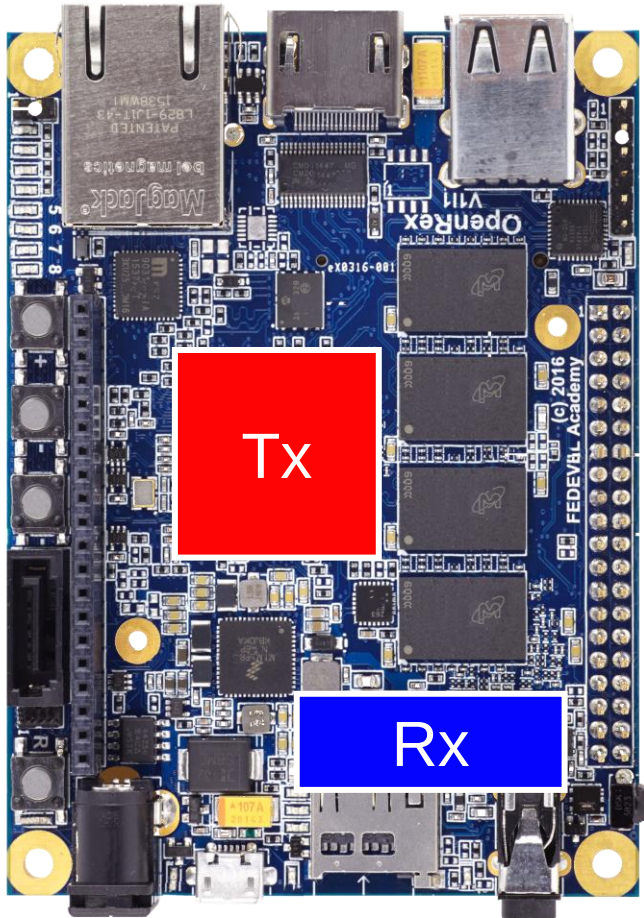


# Signal Integrity in Action

# Look at SI Analysis of a Gen 5 Tx as a Steppingstone



# Look at SI Analysis of a Gen 5 Tx as a Steppingstone

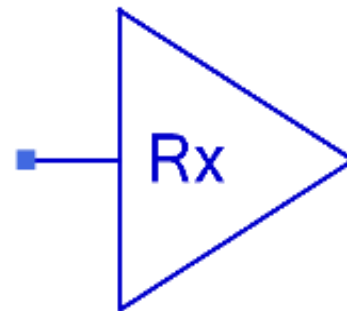


PCIe Gen 5 Transmitter

Modulation: NRZ

Data rate: 32 GT/s

Nyquist frequency: 16 GHz



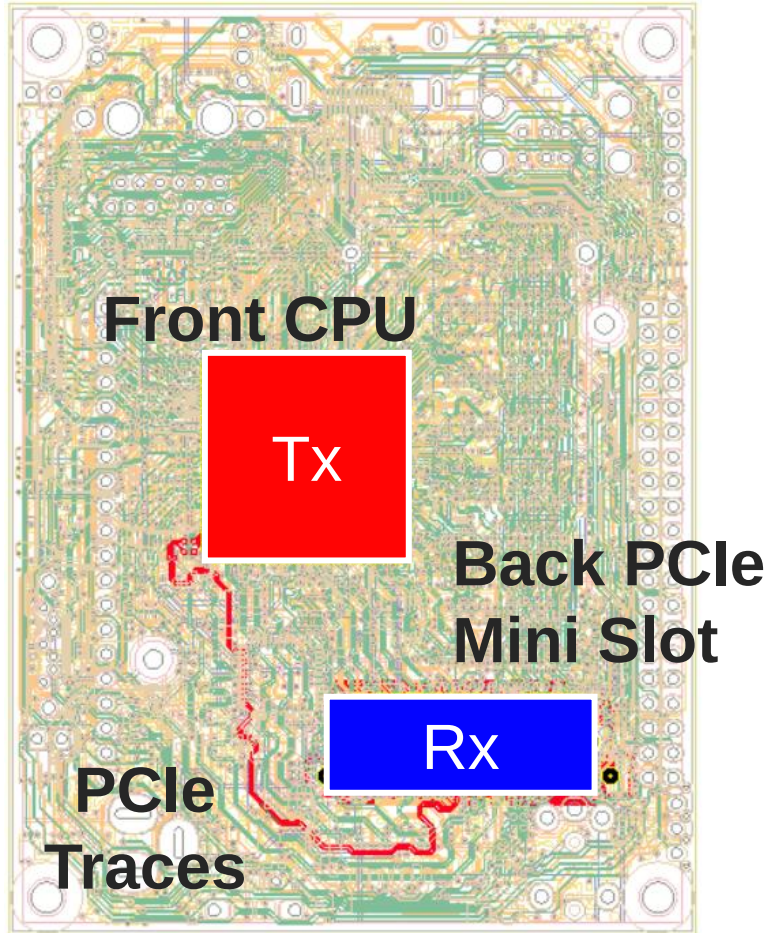
Equalization: N/A

Picture credit: <https://www.imx6rex.com/open-rex/>

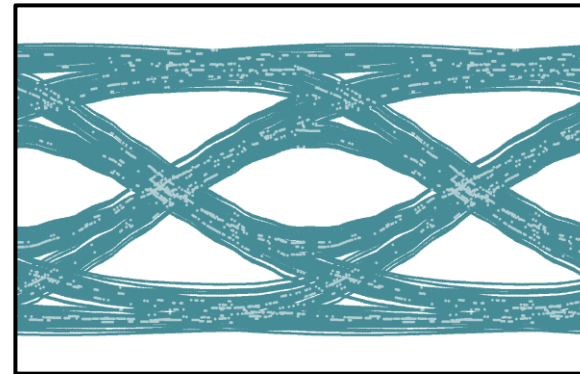
# PCIe SI Analysis of OpenRex – Three SI Metrics

## Rule #9: Anticipate Before You Measure or Simulate\*

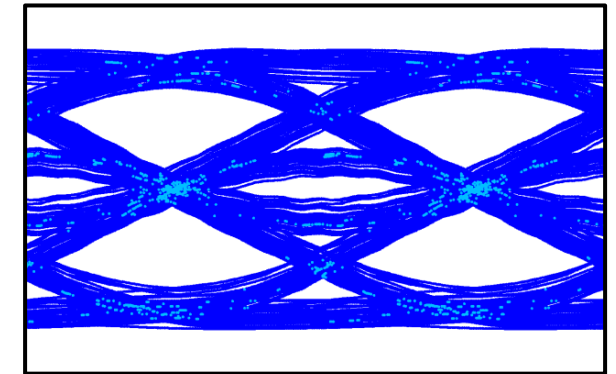
\*E. Bogatin, "Bogatin's 20 Rules for Engineers," Signal Integrity Journal, [Online]. Available: <https://www.signalintegrityjournal.com/blogs/4-eric-bogatin-signal-integrity-journal-technical-editor/post/1539-bogatins-20-rules-for-engineers>



Expected Rx eye

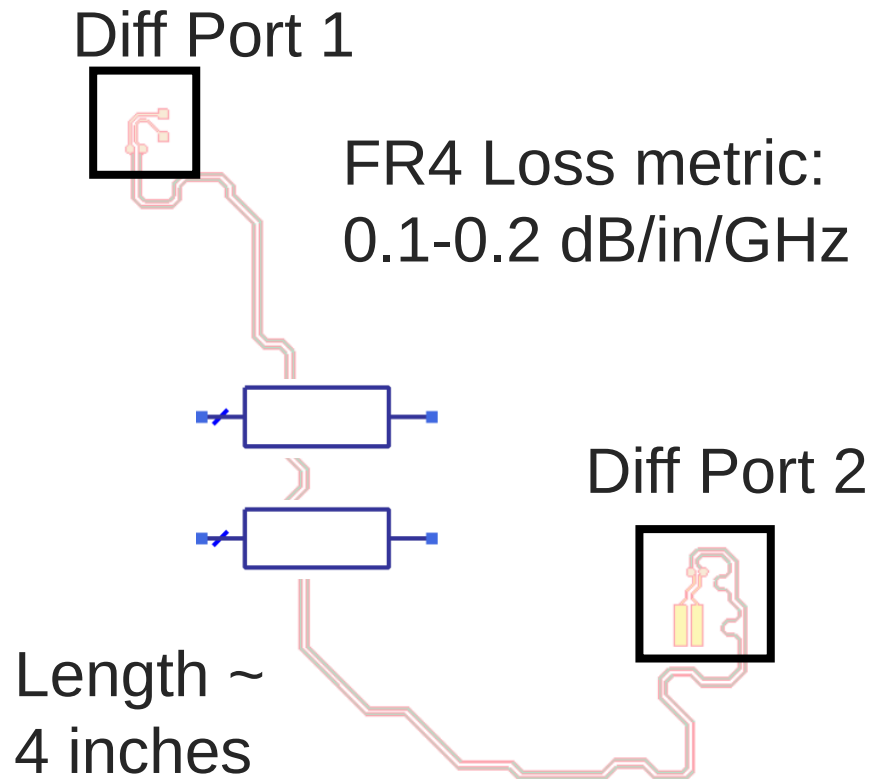


Resulted Rx eye



- Insertion loss
- Impedance
- Return loss

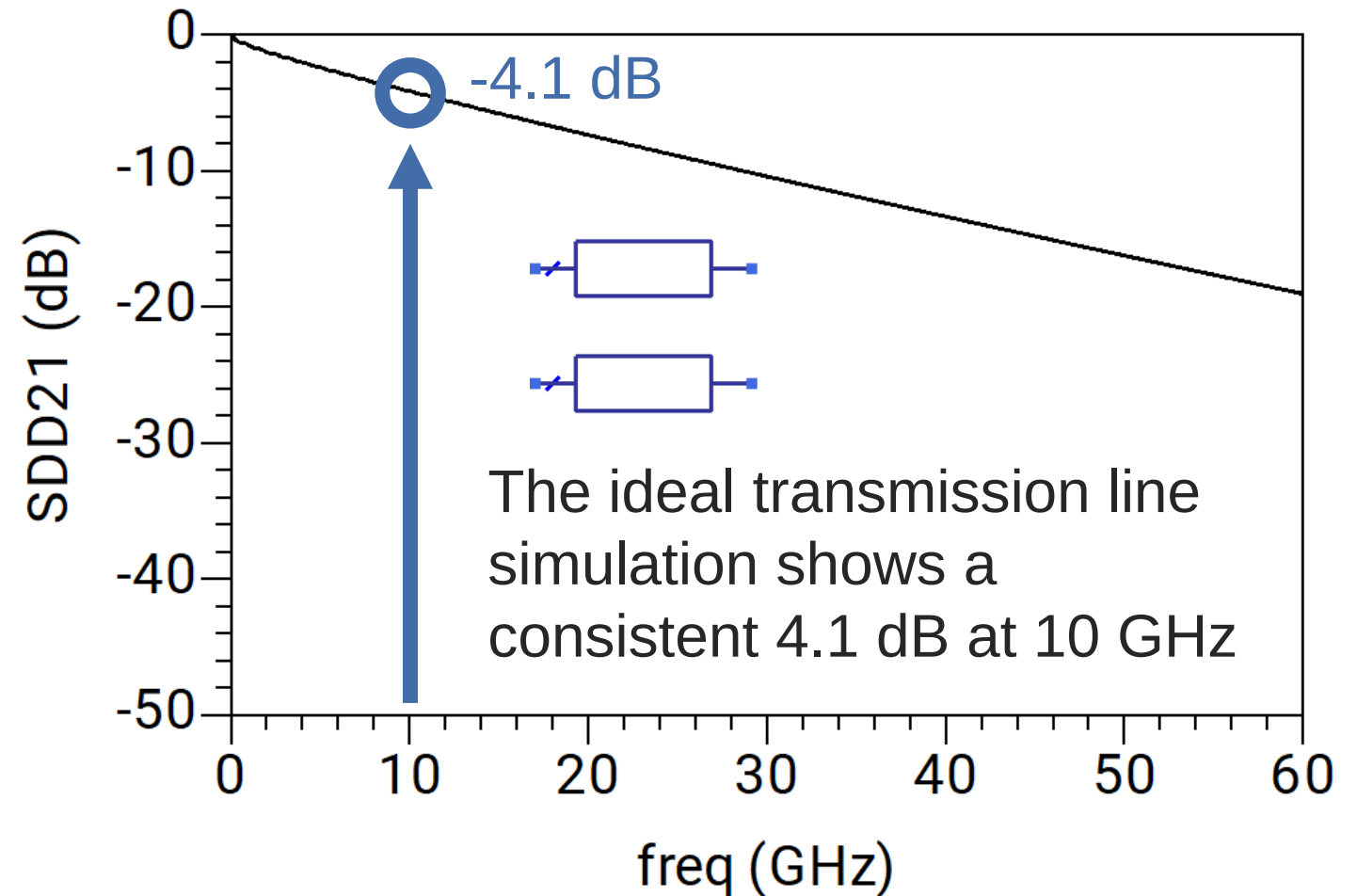
# Expected Ideal SDD21 Plot with Loss Metric 0.1-0.2 dB/in/GHz



Insertion loss from loss metric  
and ideal simulated results are  
consistent with each other

Expected SDD21 at 10 GHz?

→ SDD21 ~ 4 dB at 10 GHz



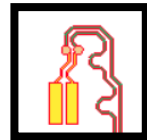
# Unexpected SDD21 Dips in Layout Simulation

Diff Port 1



Expected ~4  
dB at 10 GHz

Diff Port 2

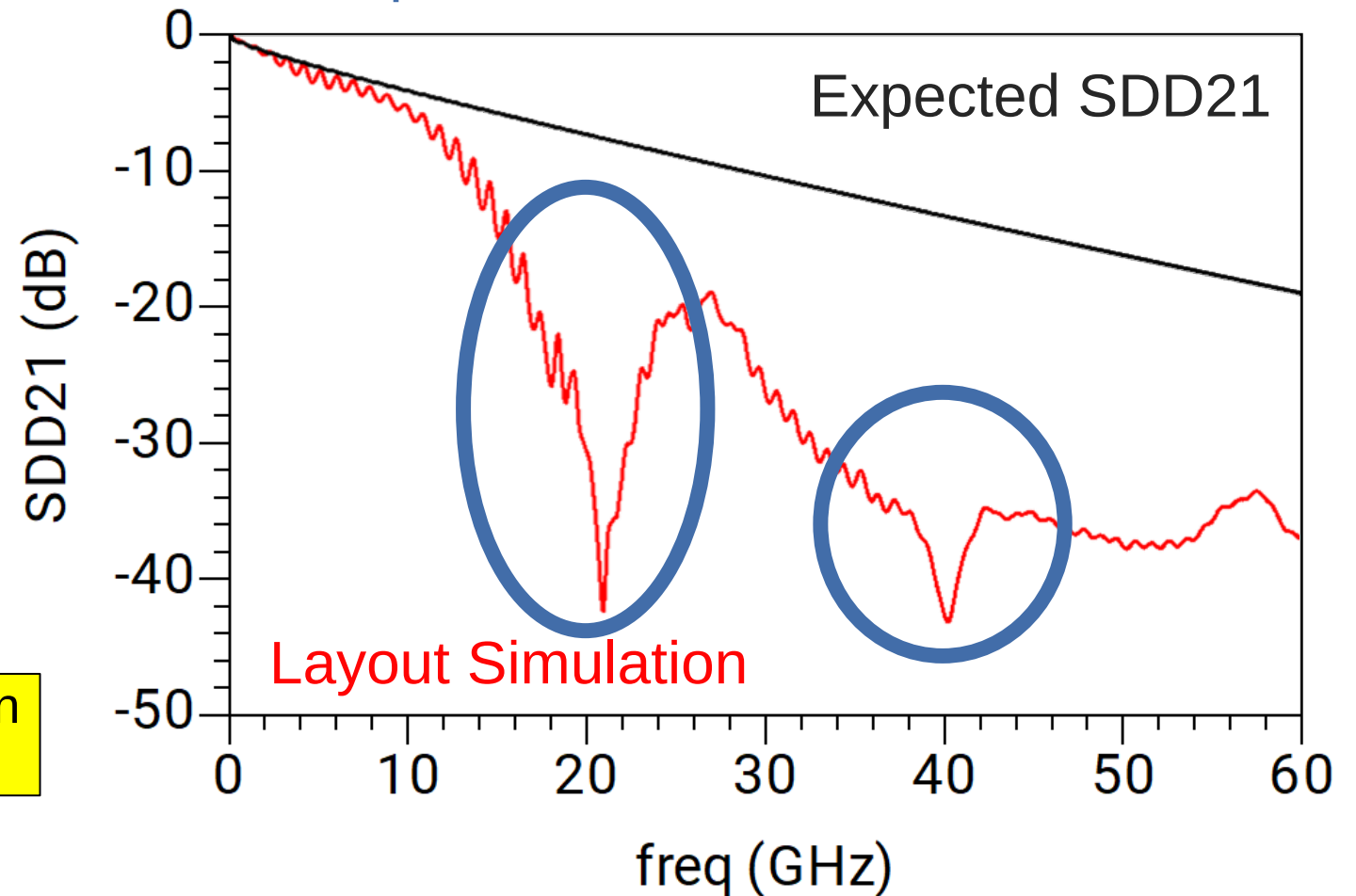


Insertion loss from layout simulation  
is different than expected

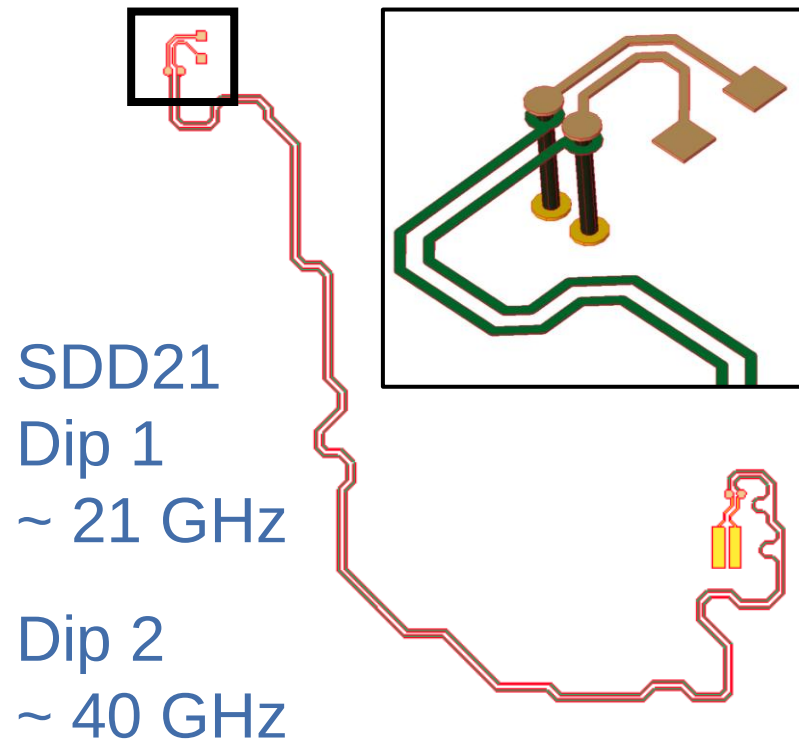
Unexpected SDD21 dips in layout simulation

Dip 1 ~ 21 GHz

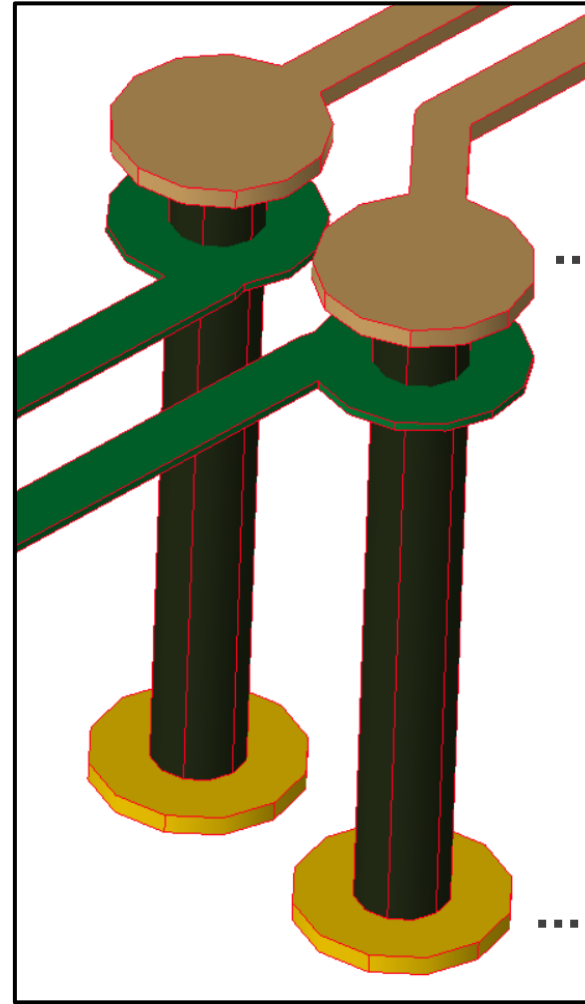
Dip 2 ~ 40 GHz



# Stub Resonance as a Possible Cause for One of the Dips



The insertion loss dip around 20 GHz can be caused by the via stub



Stub resonance estimation  
(Assumes FR4)

$$f_{\text{res}} = 1.5 / \text{stub length (inch)}$$

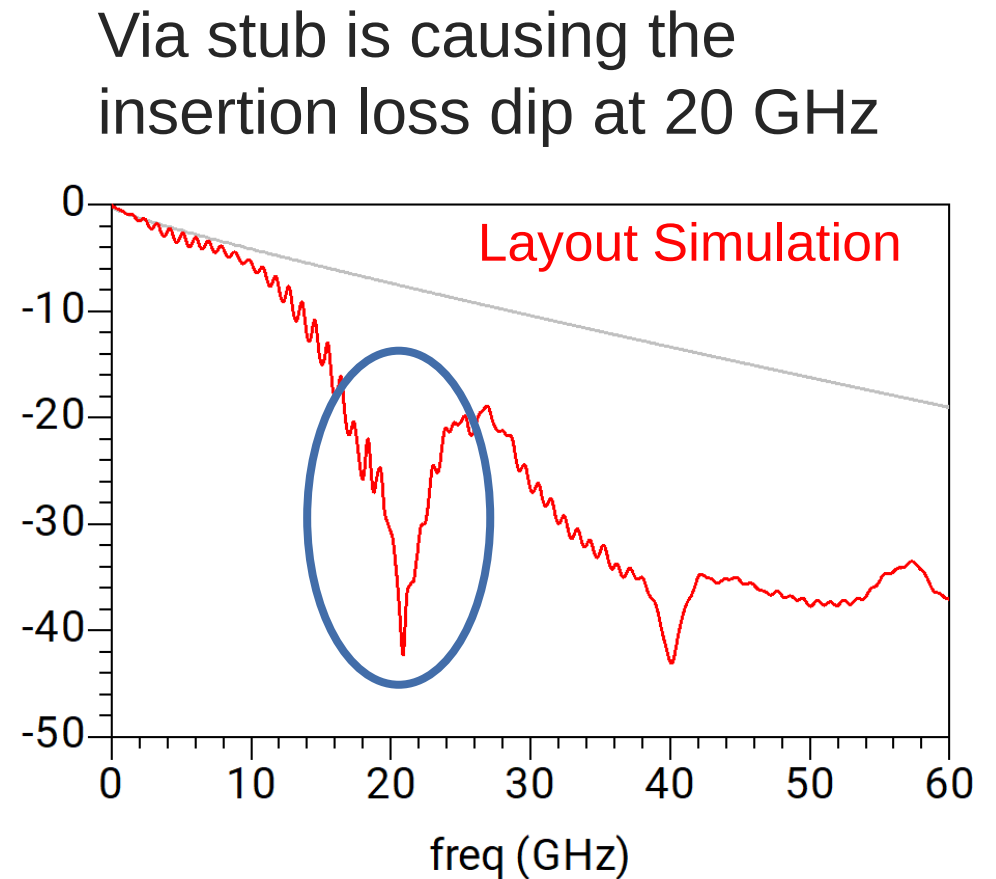
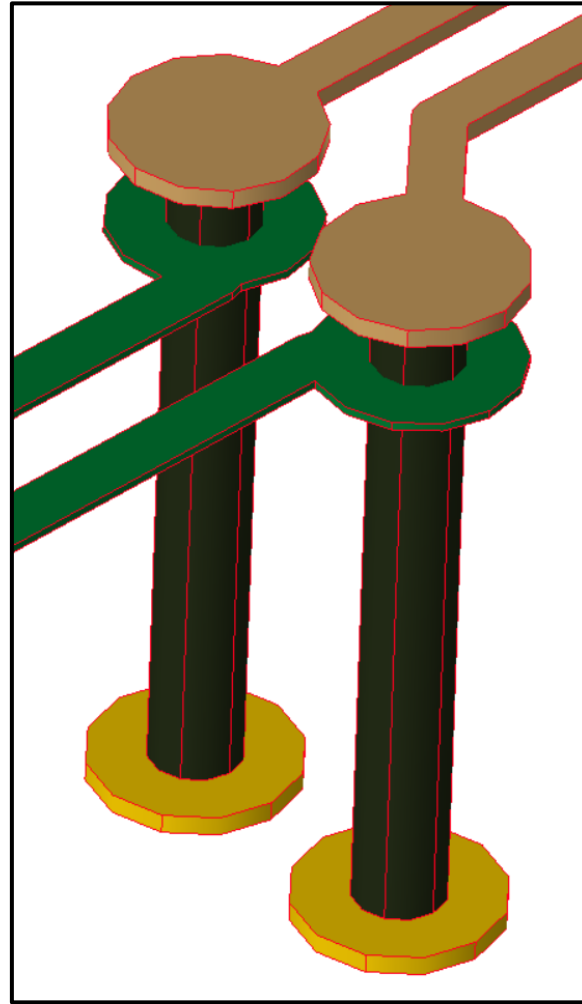
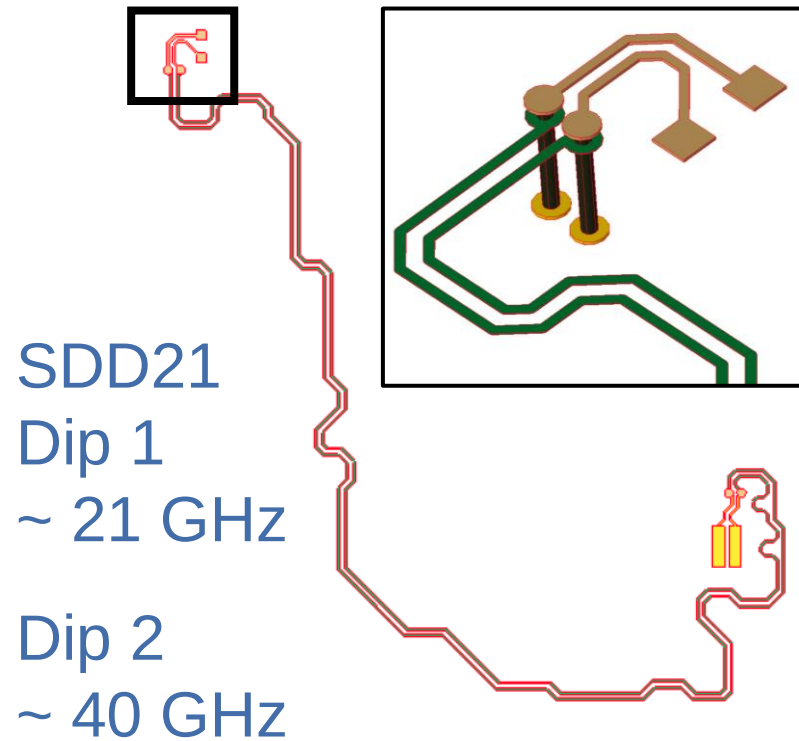
Length:  
~ 1.6 mm / 64 mil / 0.064 inch

Expected resonance

$$f_{\text{res}} \sim 23.4 \text{ GHz}$$

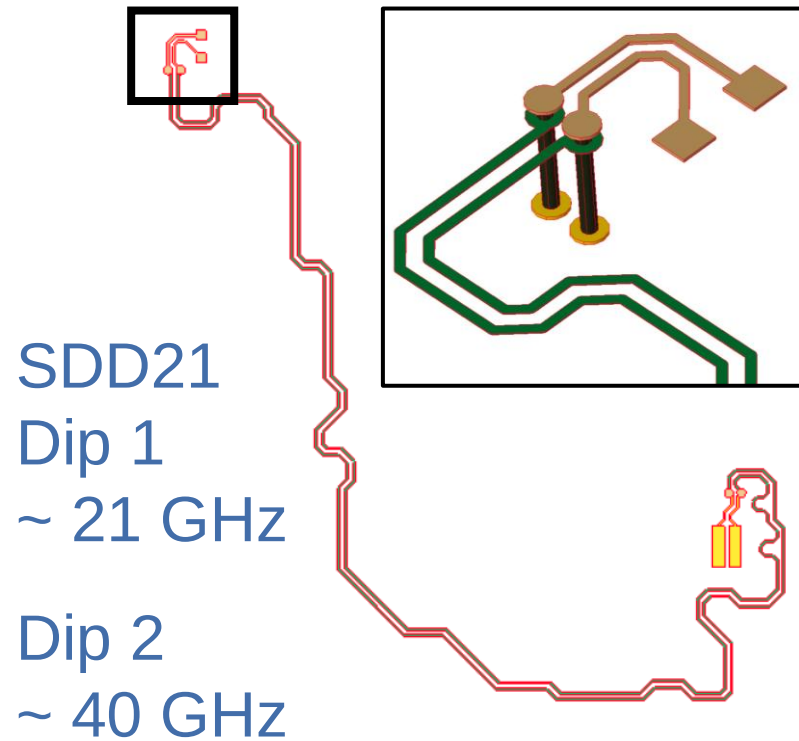
SDD21 Dip 1  
~ 21 GHz

# Virtual Back-drilling in Layout Simulation Fixed the Dip

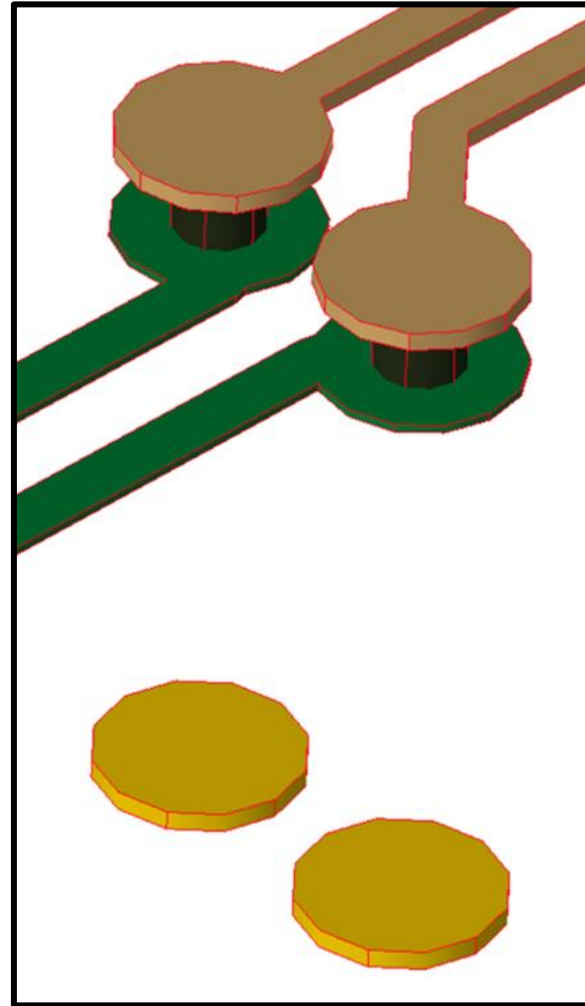


Remove the stub to solve the problem!

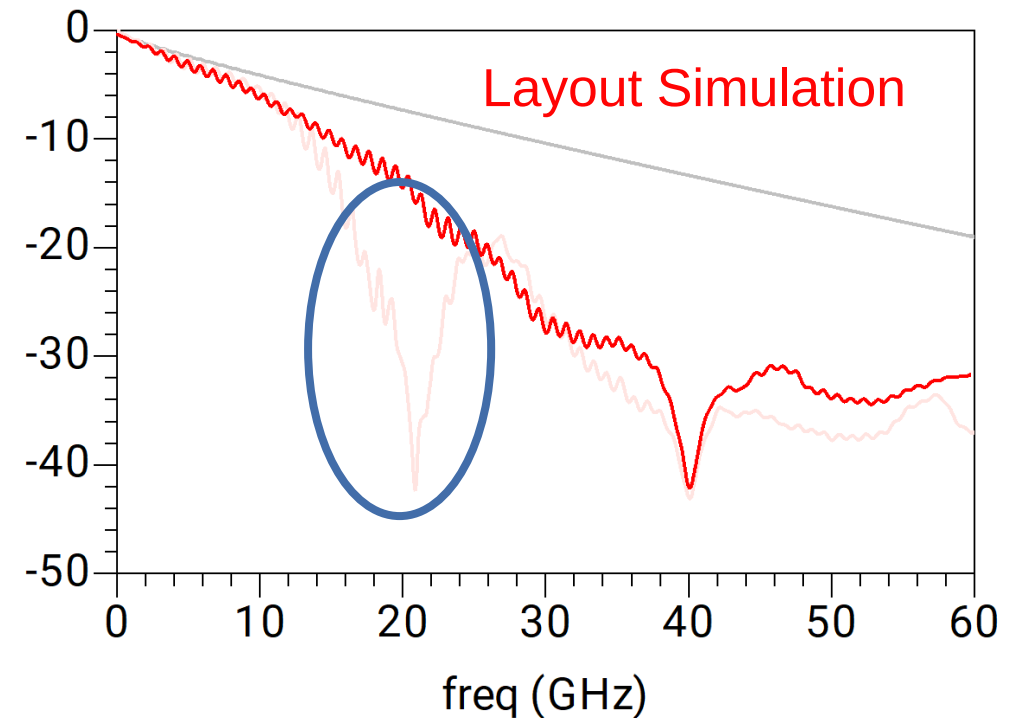
# Virtual Back-drilling in Layout Simulation Fixed the Dip



Virtual back-drilling removes the stub and removes the resonance at ~20 GHz

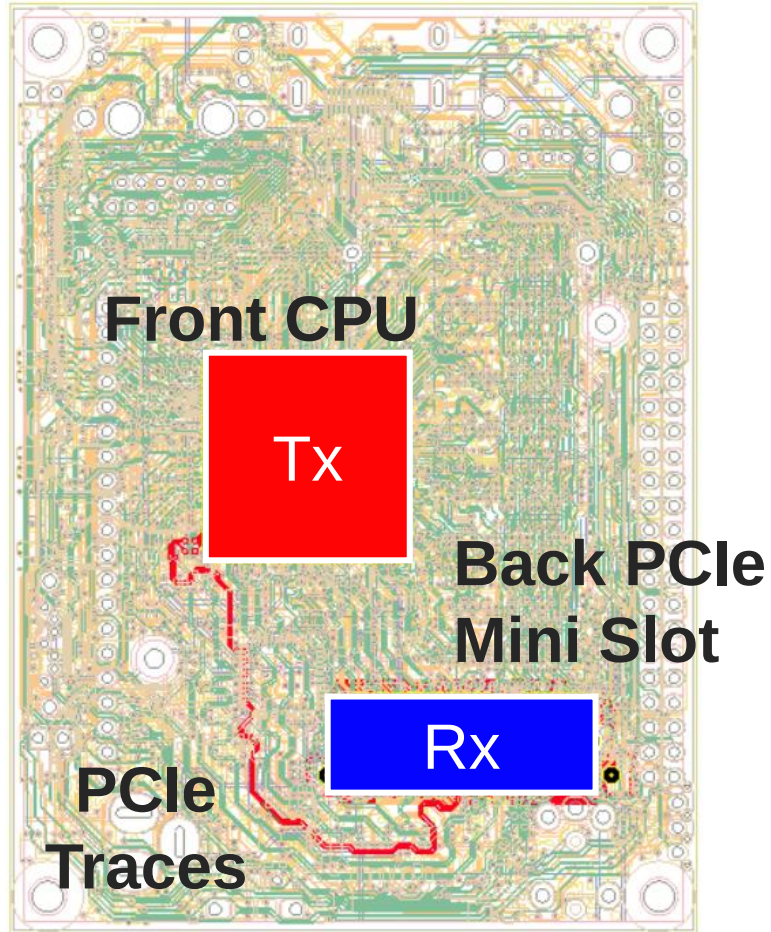


Remove the stub with back-drilling

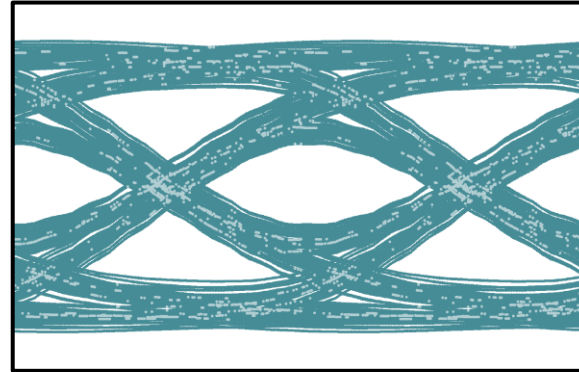


Bonus: What about the 40 GHz dip?

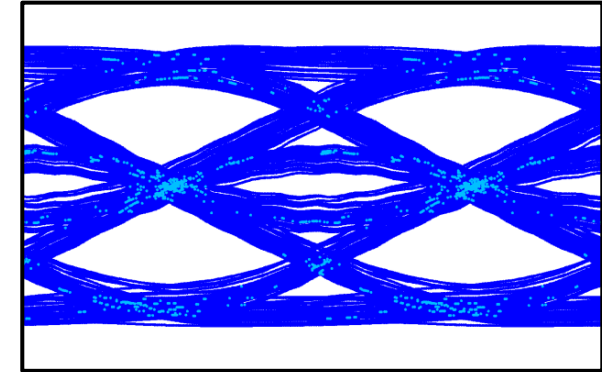
# Fixing the Stub Resonance Improves the Eye



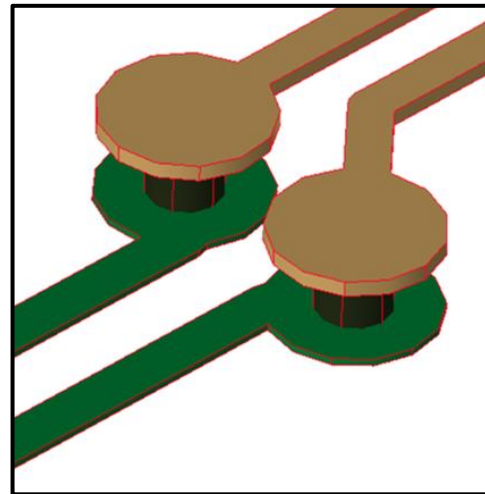
Expected Rx eye



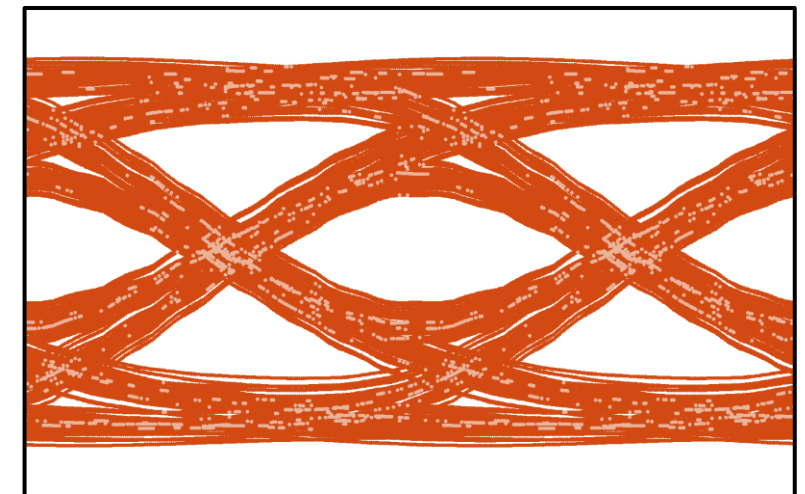
Resulted Rx eye



Root Cause



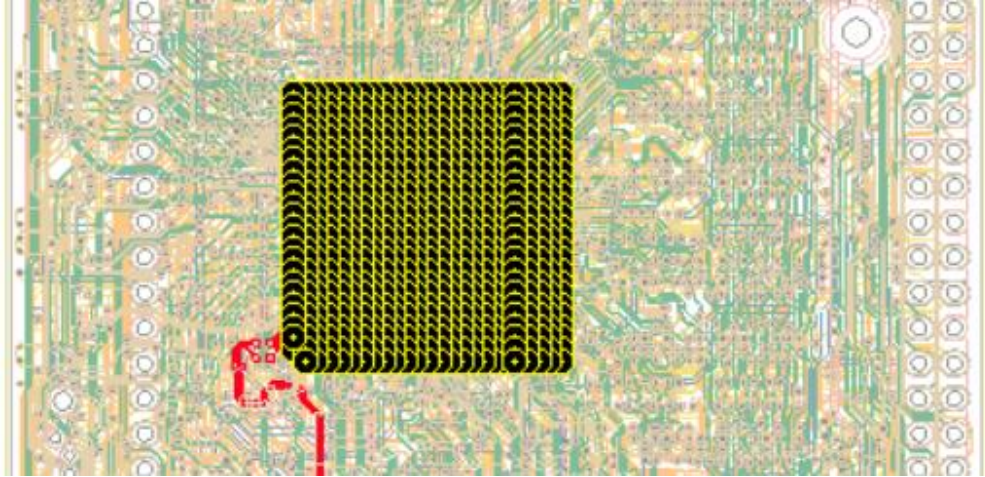
Fixed Rx eye



Virtual back-drilling removes the stub and removes the resonance at ~20 GHz

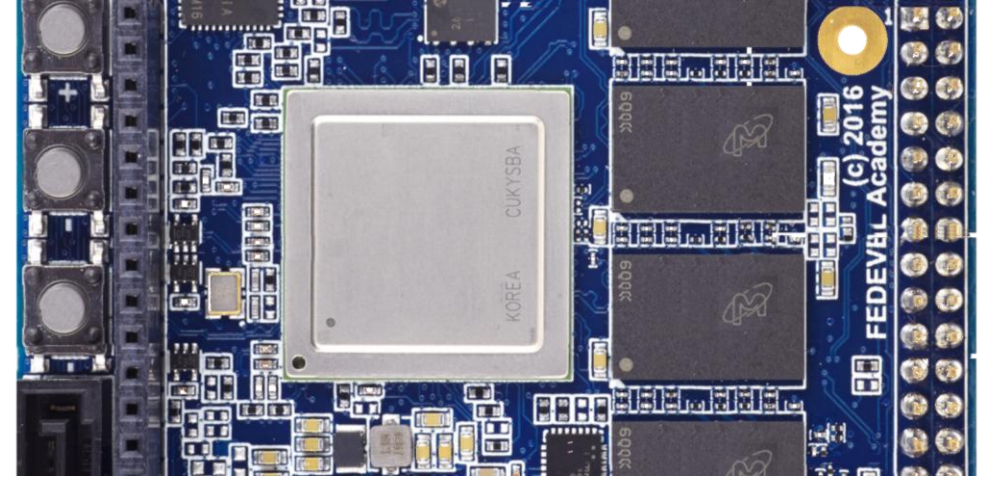
# Unexpected Impedance Result

# Unexpected Controlled Impedance Difference



As-designed stripline  
differential impedance

85  $\Omega$



As-fabricated stripline  
differential impedance

89  $\Omega$

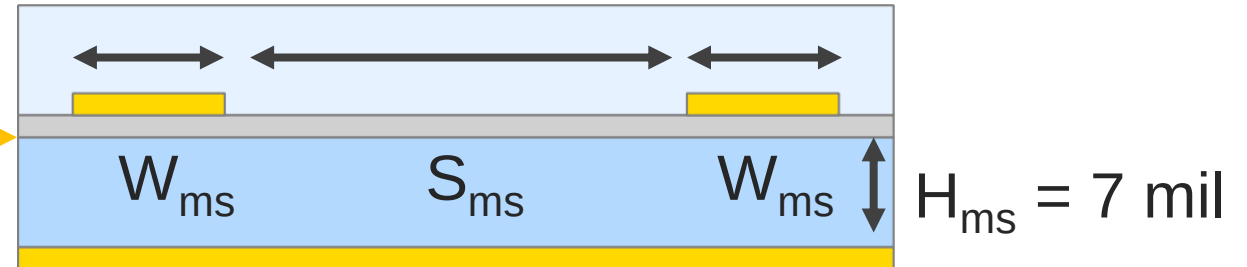
What's causing the differences?

Spacing?

Trace width?

# Impedance Expectation Based on Stack-up and Spacing

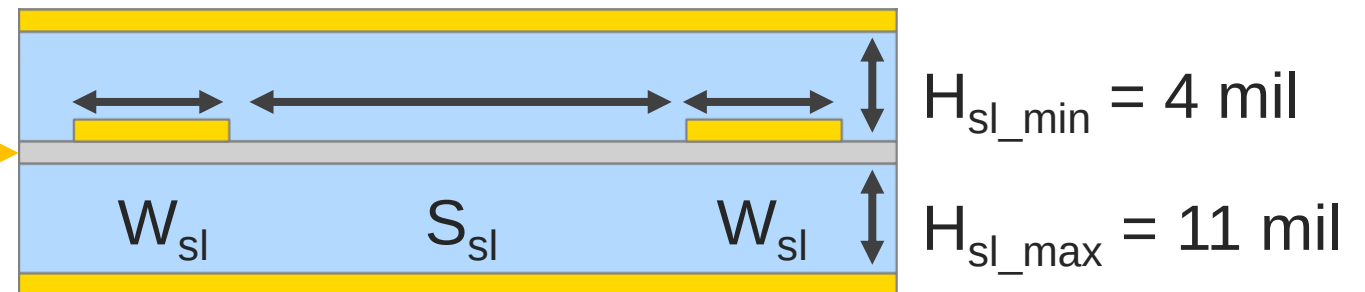
## Microstrip differential pair



Assume:  $S_{ms} > 3 W_{ms}$

$Z_{diff}$ : ~100 Ohm if  $W_{ms} = 2H$

## Stripline differential pair



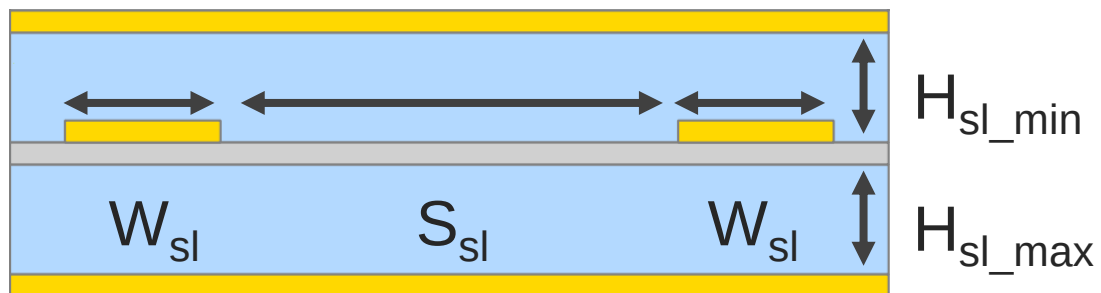
Assume:  $S_{sl} > 3 W_{sl}$

$Z_{diff}$ : ~100 Ohm if  $W_{sl} = 2 H_{sl\_min}$

When the traces are uncoupled (spacing is more than 3 times of the width), making trace width twice the substrate height gives you  $Z_{diff} = 100 \text{ Ohm}$

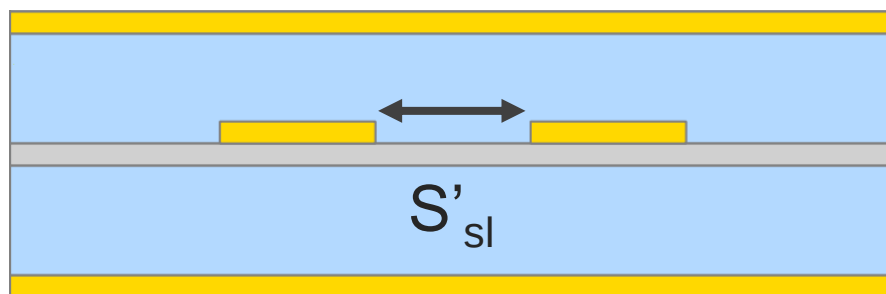
# $Z_{\text{diff}}$ Decreases as the Spacing Decreases

Stripline differential pair

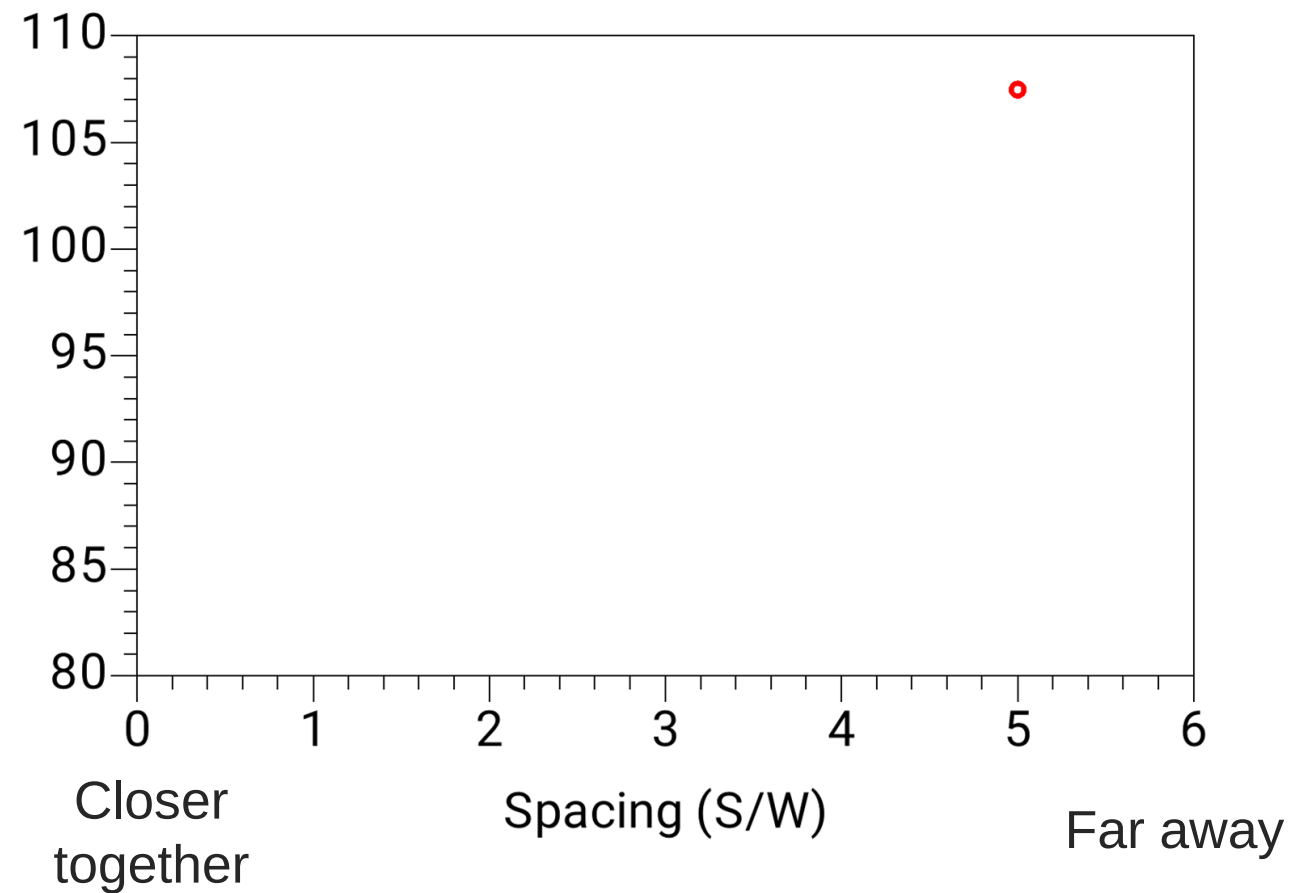


Assume:  $S_{\text{sl}} > 3 W_{\text{sl}}$

$Z_{\text{diff}}$ :  $\sim 100$  Ohm if  $W_{\text{sl}} = 2 H_{\text{sl\_min}}$

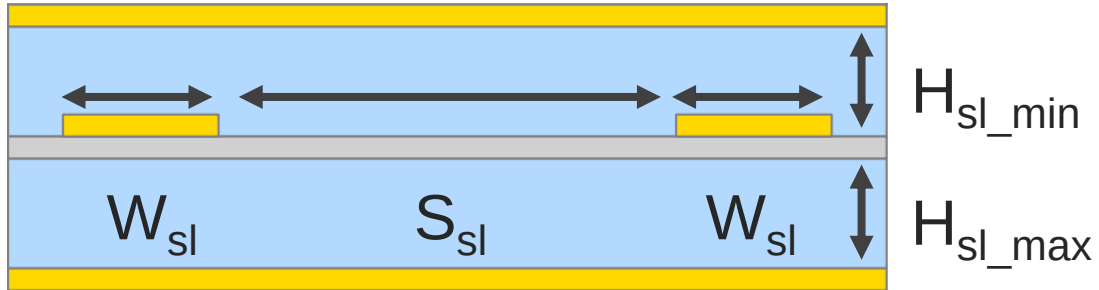


Assume:  $W_{\text{sl}}$  stay unchanged



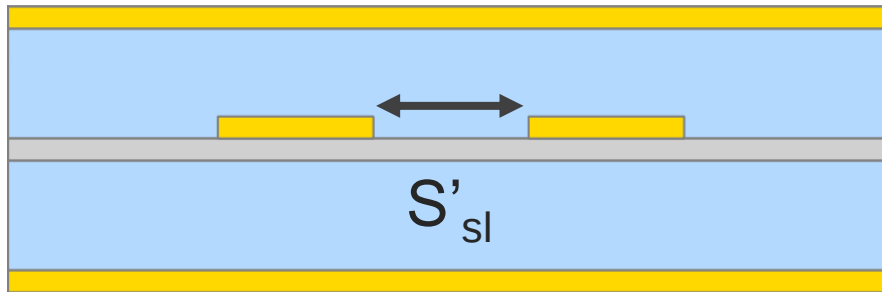
# $Z_{diff}$ Decreases as the Spacing Decreases

Stripline differential pair



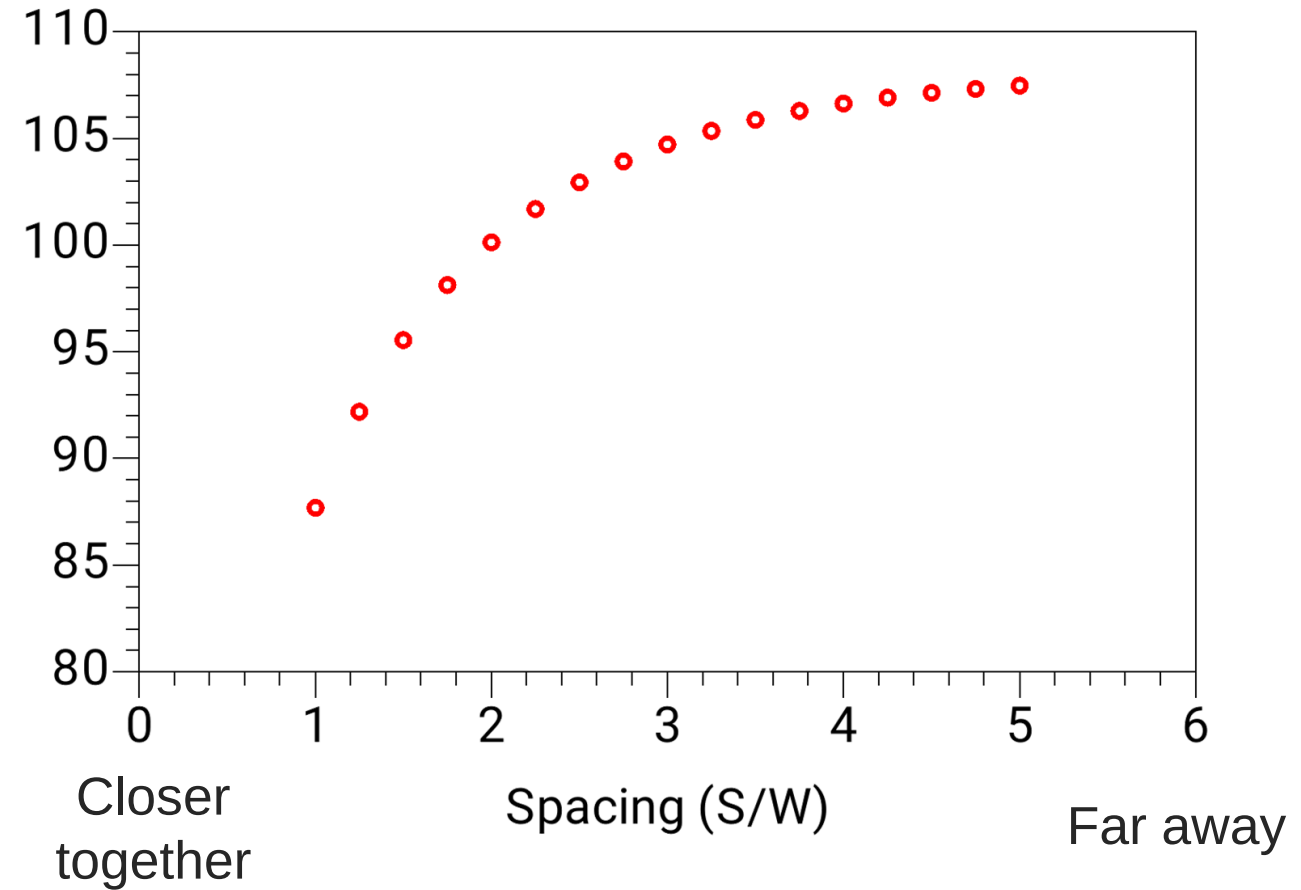
Assume:  $S_{sl} > 3 W_{sl}$

$Z_{diff}$ : ~100 Ohm if  $W_{sl} = 2 H_{sl\_min}$



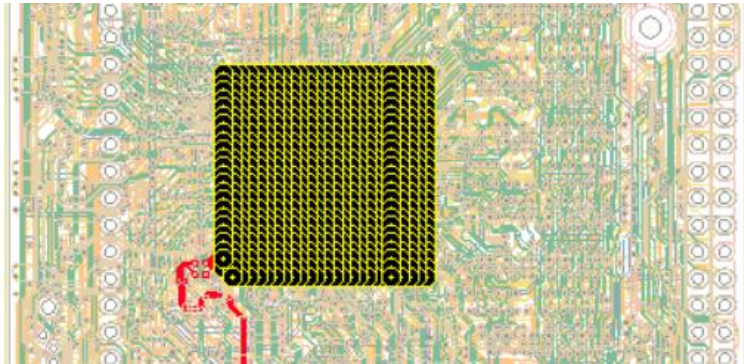
Assume:  $W_{sl}$  stay unchanged

$Z_{diff}$  decreases as the spacing decreases

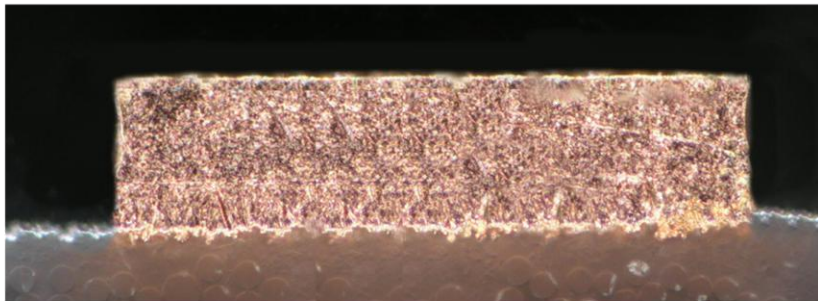


When the spacing reduces, the  $Z_{diff}$  decreases. Deviation of spacing is not the root cause of impedance increase.

# PCB Process Produces Etch-back that Increases Impedance



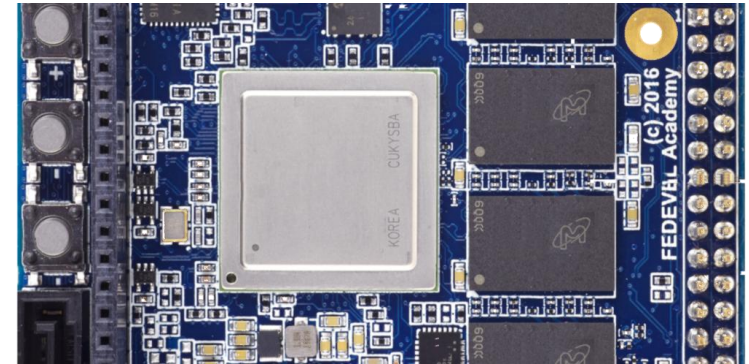
As-designed:  $85\ \Omega$



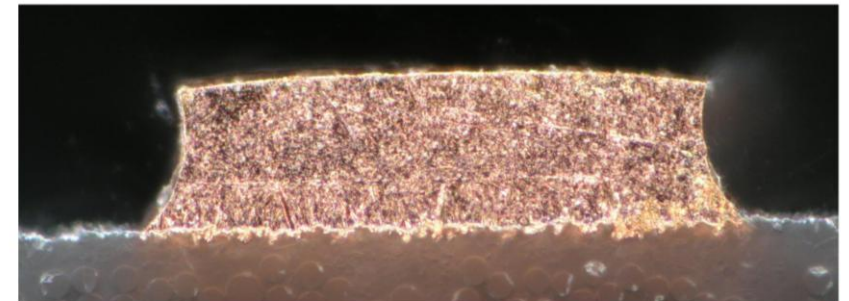
as - designed  
trace is rectangular

Printed Circuit  
Board  
Fabrication  
Process

Fabrication introduces  
etch-back that increases  
trace impedance

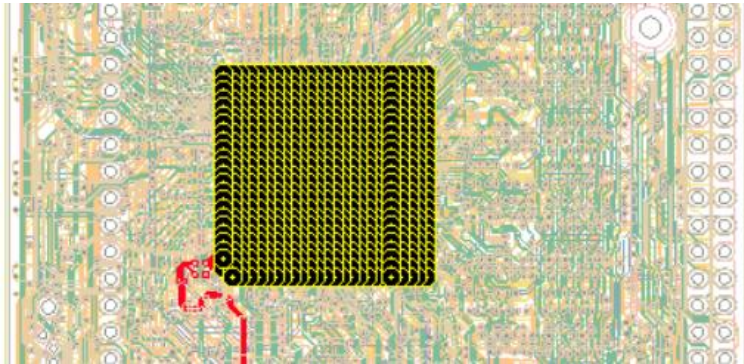


As-fabricated:  $89\ \Omega$

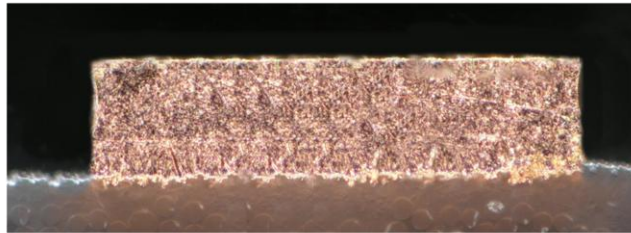
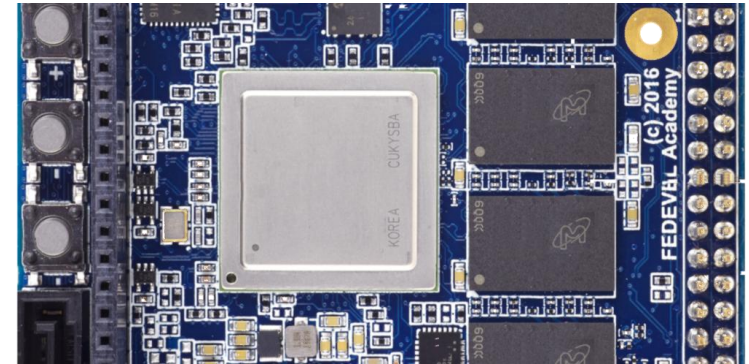


as-fabricated  
trace is trapezoidal

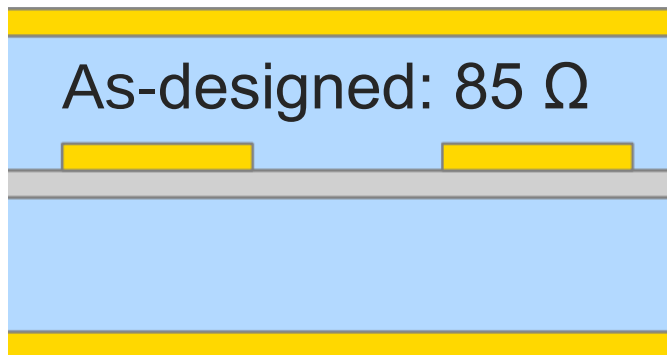
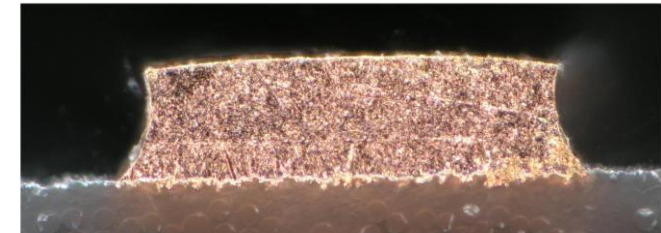
# Etch-back in Simulation Confirms the As-fabricated Increase



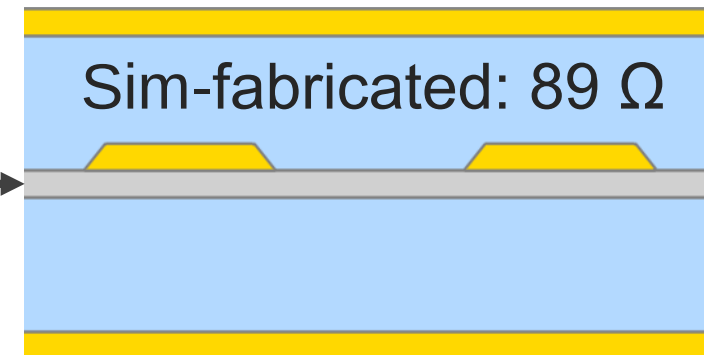
Printed Circuit  
Board  
Fabrication  
Process



Simulation confirms etch-back increases trace impedance.

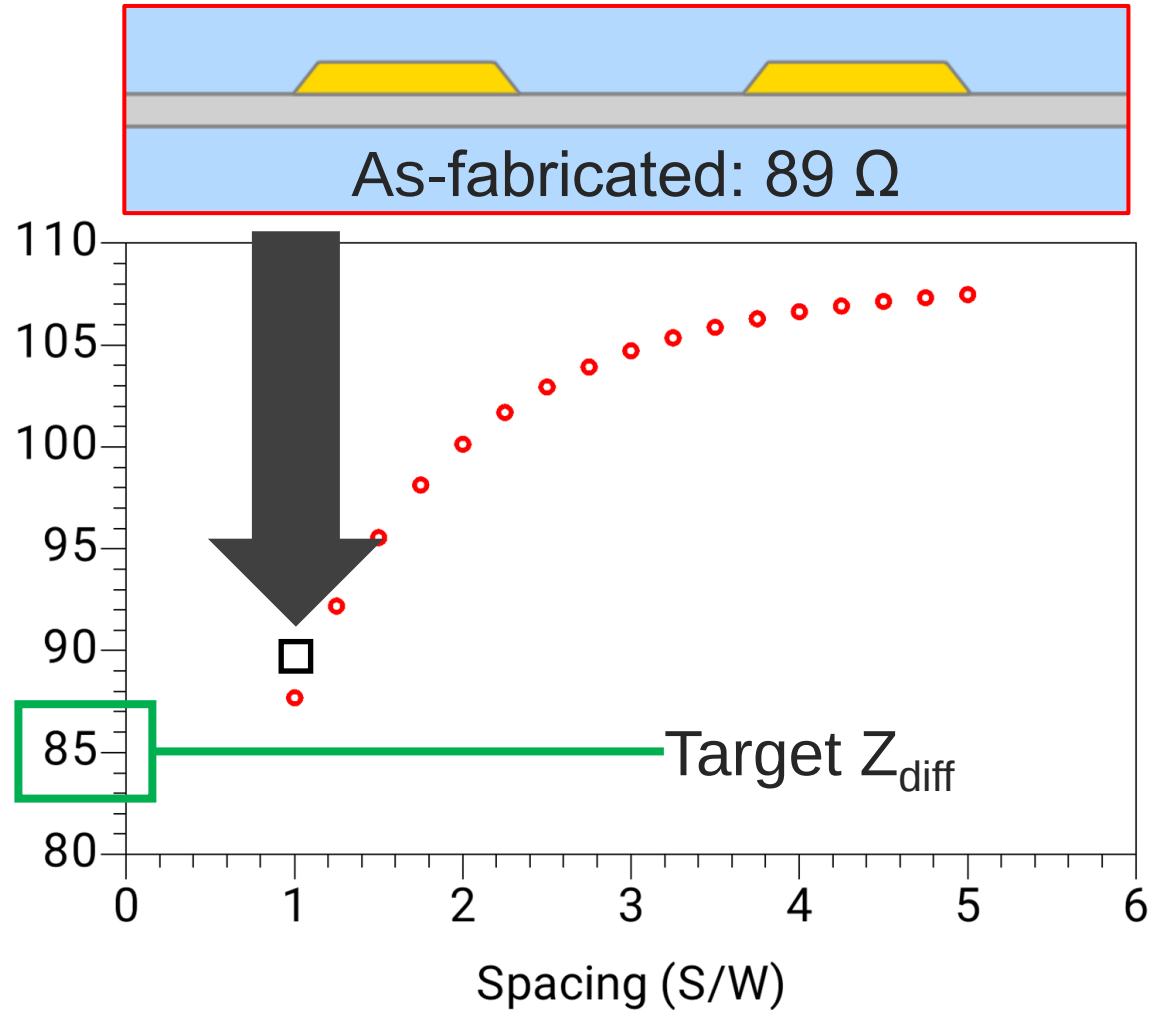


Add etch-back  
in simulation

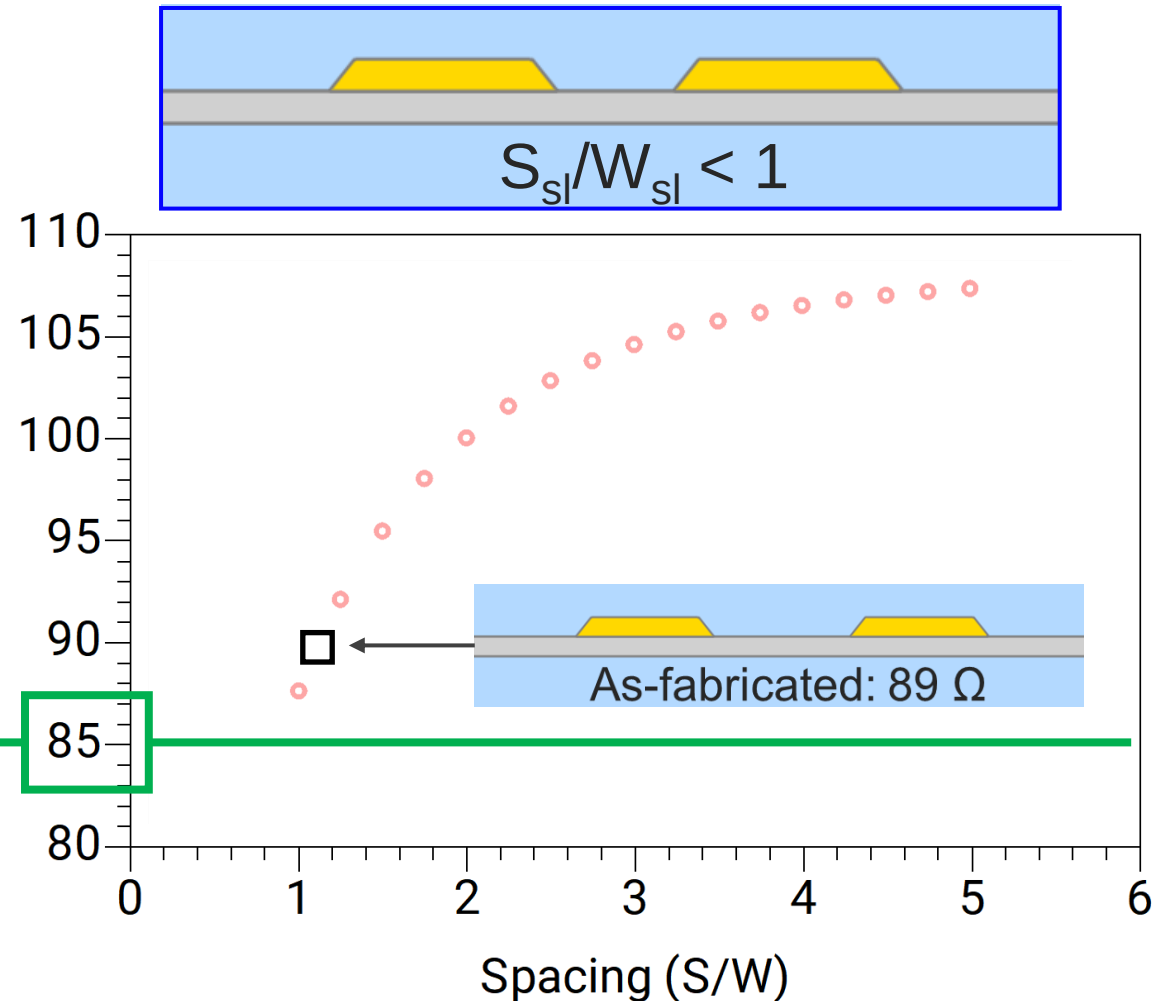
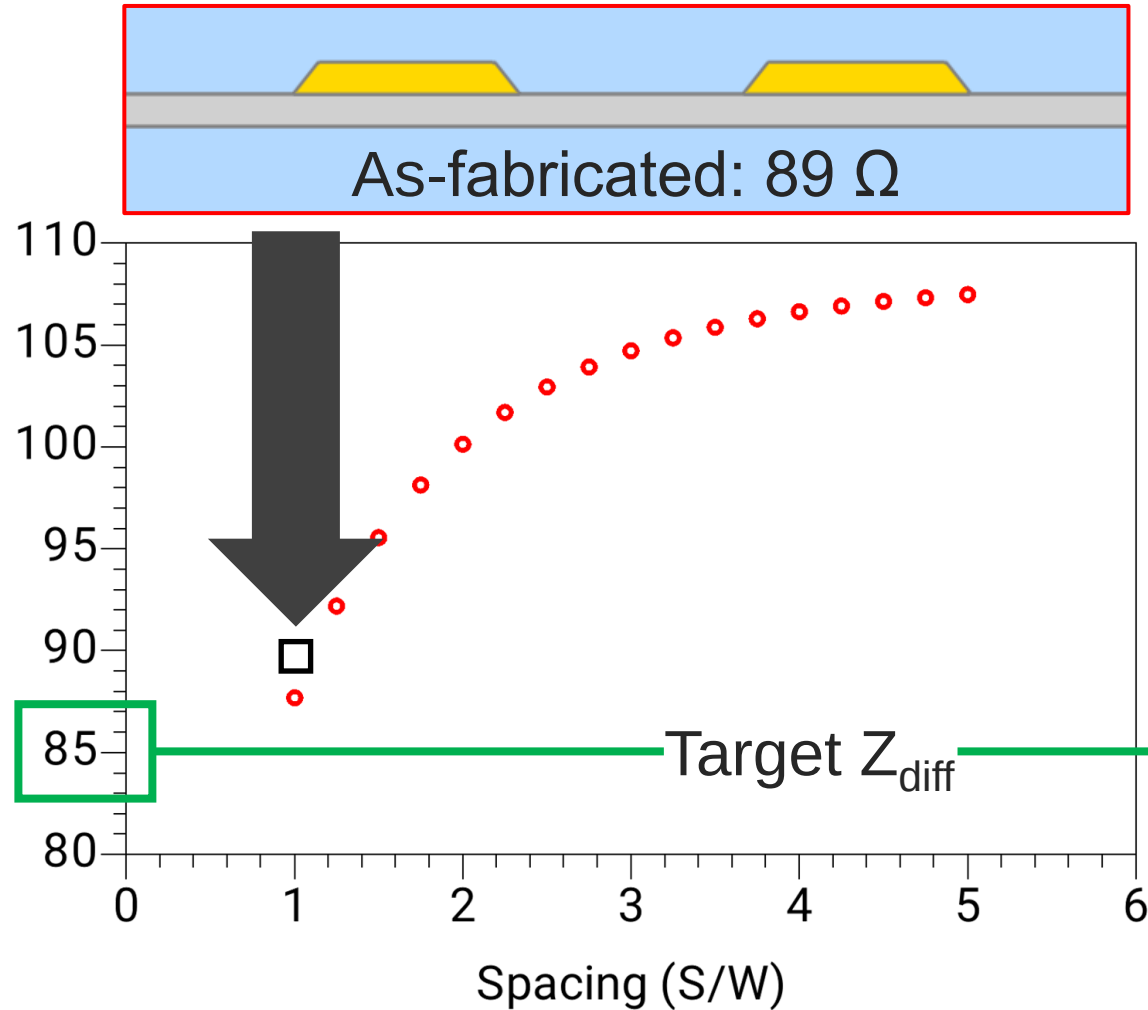


Now what?!

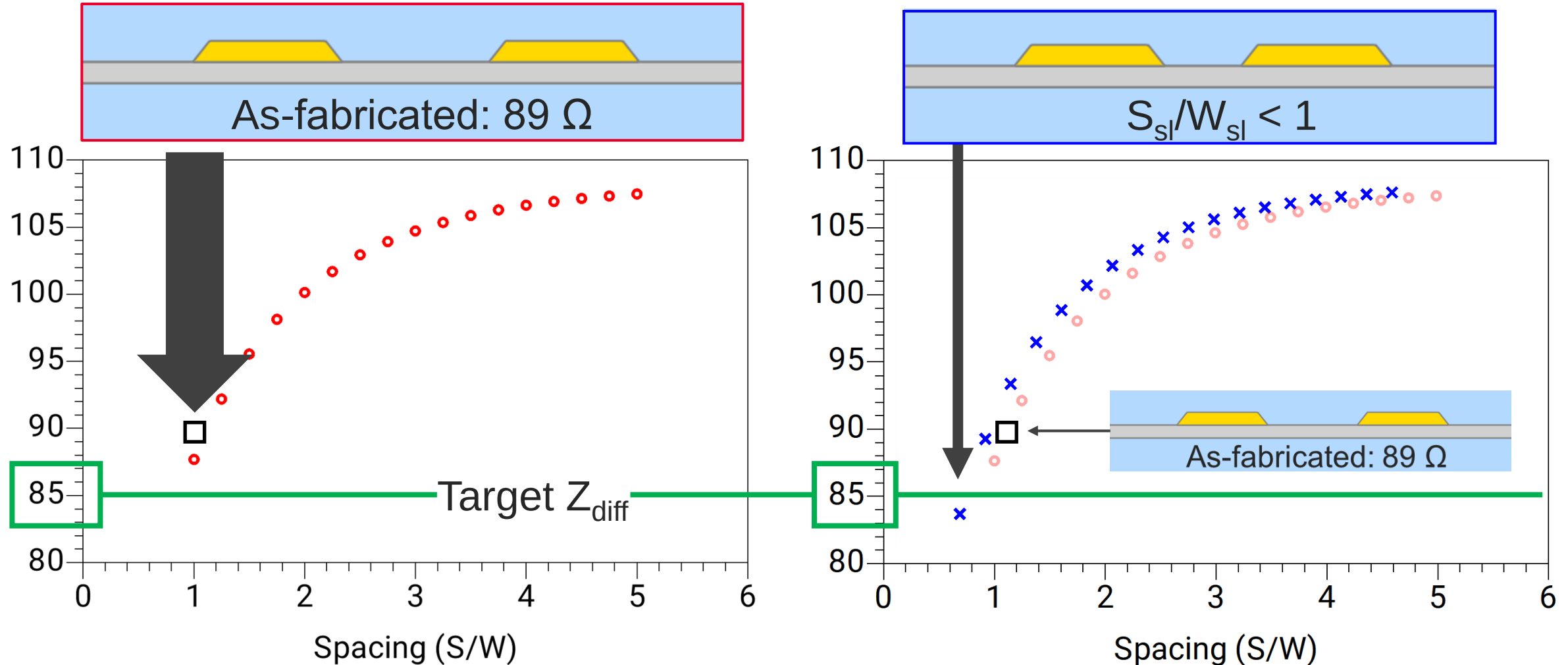
# Reduce Spacing to Compensate for the Impedance Increase



# Reduce Spacing to Compensate for the Impedance Increase

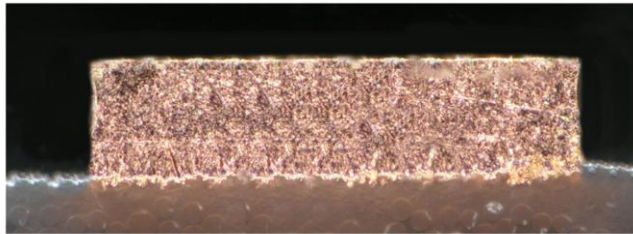


# Reduce Spacing to Compensate for the Impedance Increase



Knowing that etch-back will increase the impedance, we can bring the traces even closer. This approach can increase trace density.

## Start with Wider Traces to Compensate for the Increase

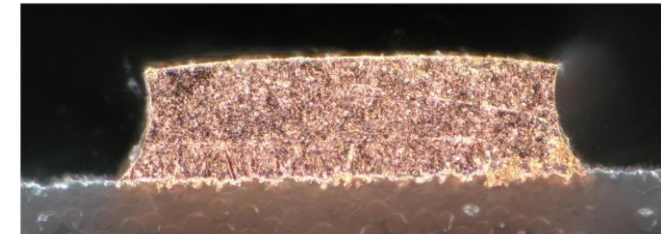


As-designed

Original

4.4 mil (85  $\Omega$ )

Printed Circuit  
Board  
Fabrication  
Process



As-fabricated

89  $\Omega$

Improved

4.9 mil (81  $\Omega$ )

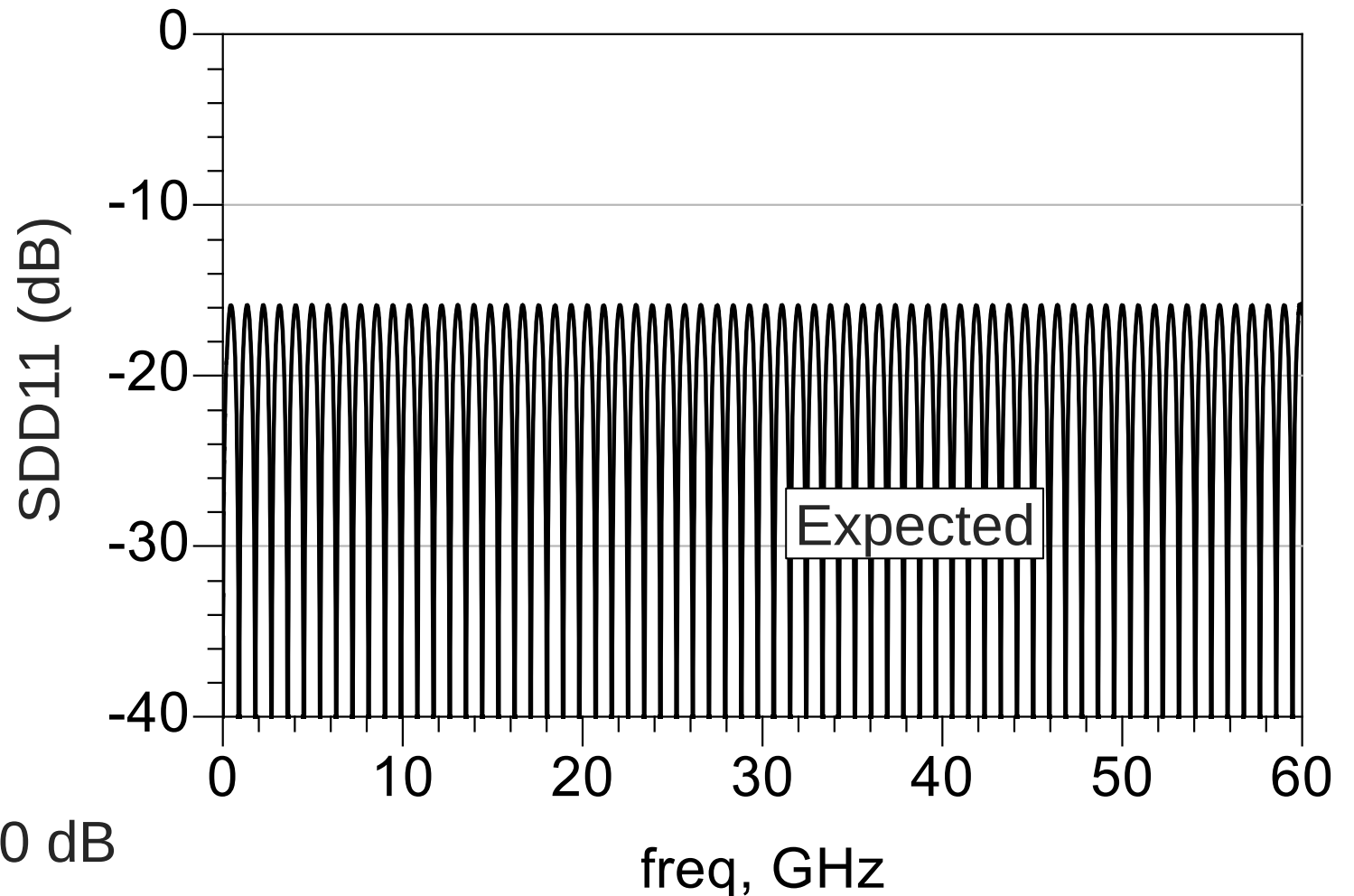
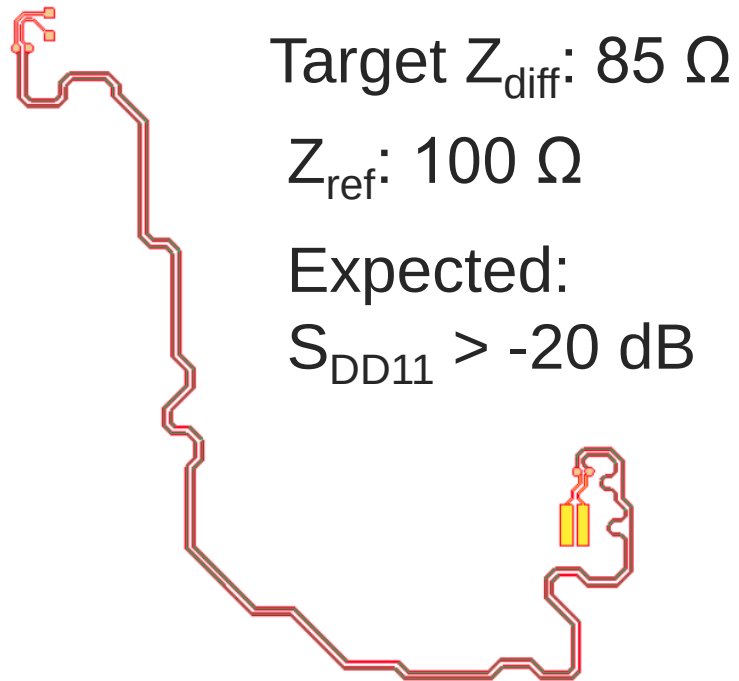
85  $\Omega$

Knowing that etch-back will increase the impedance, we can start with a wider trace width. This approach maintain the same spacing.

# Unexpected SDD11 Result

# Observation: SDD11 Ramp-up as Frequency Increases

Expected: Flat SDD11 throughout frequency range



Expected  $S_{\text{DD11}} \sim 20\log(2\Gamma)$

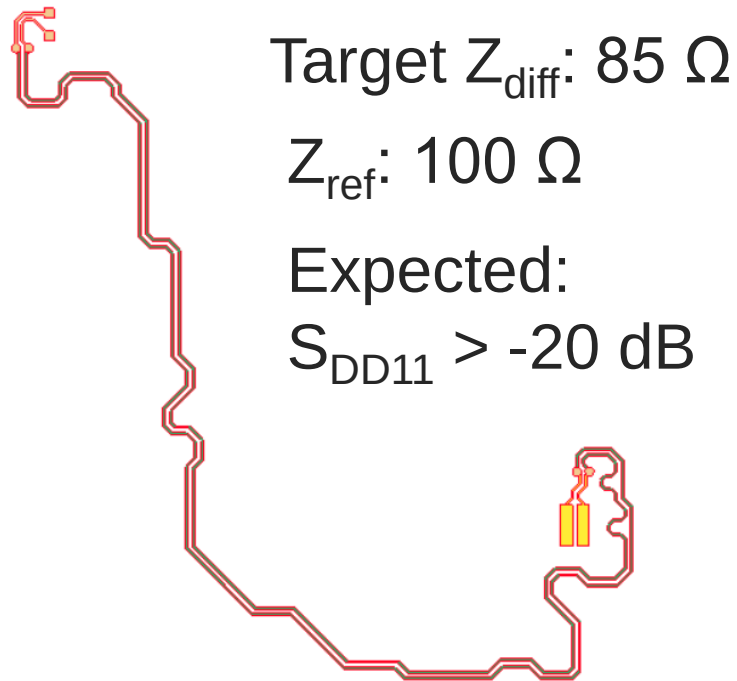
$$\Gamma = (Z_{\text{diff}} - Z_{\text{ref}}) / (Z_{\text{diff}} + Z_{\text{ref}})$$

$2\Gamma \sim 15\%$     10% reflected  $\sim 20$  dB

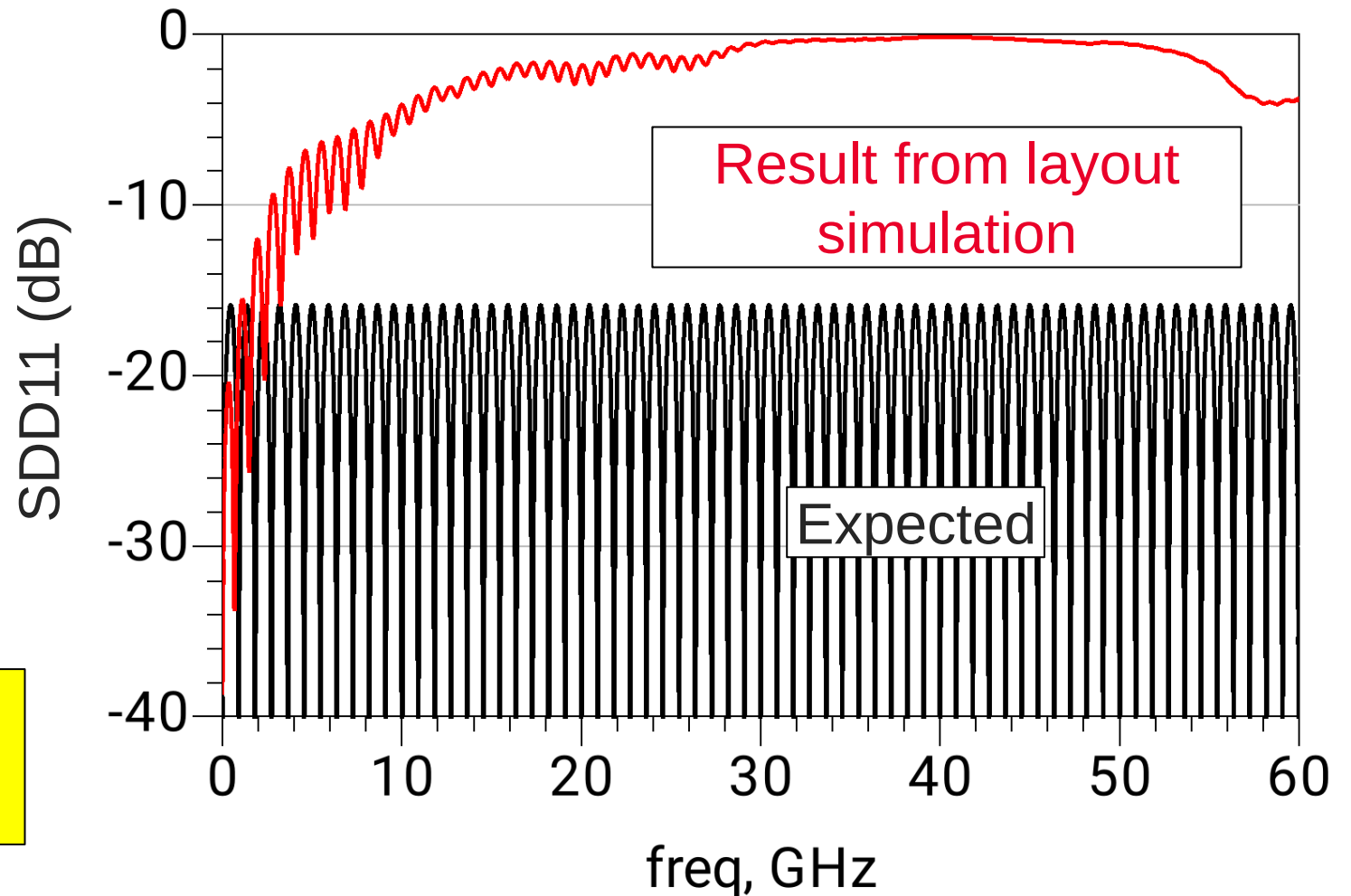
# Observation: SDD11 Ramp-up as Frequency Increases

Expected: Flat SDD11 throughout frequency range

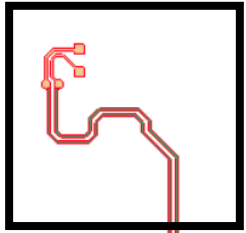
Observed: SDD11 ramping up as frequency increases



Expected SDD11 is different than simulated SDD11. Simulated SDD11 shows a ramp-up.



# Small Impedance Discontinuity Causes SDD11 Ramp-up



Target  $Z_{\text{diff}}$ : 85  $\Omega$

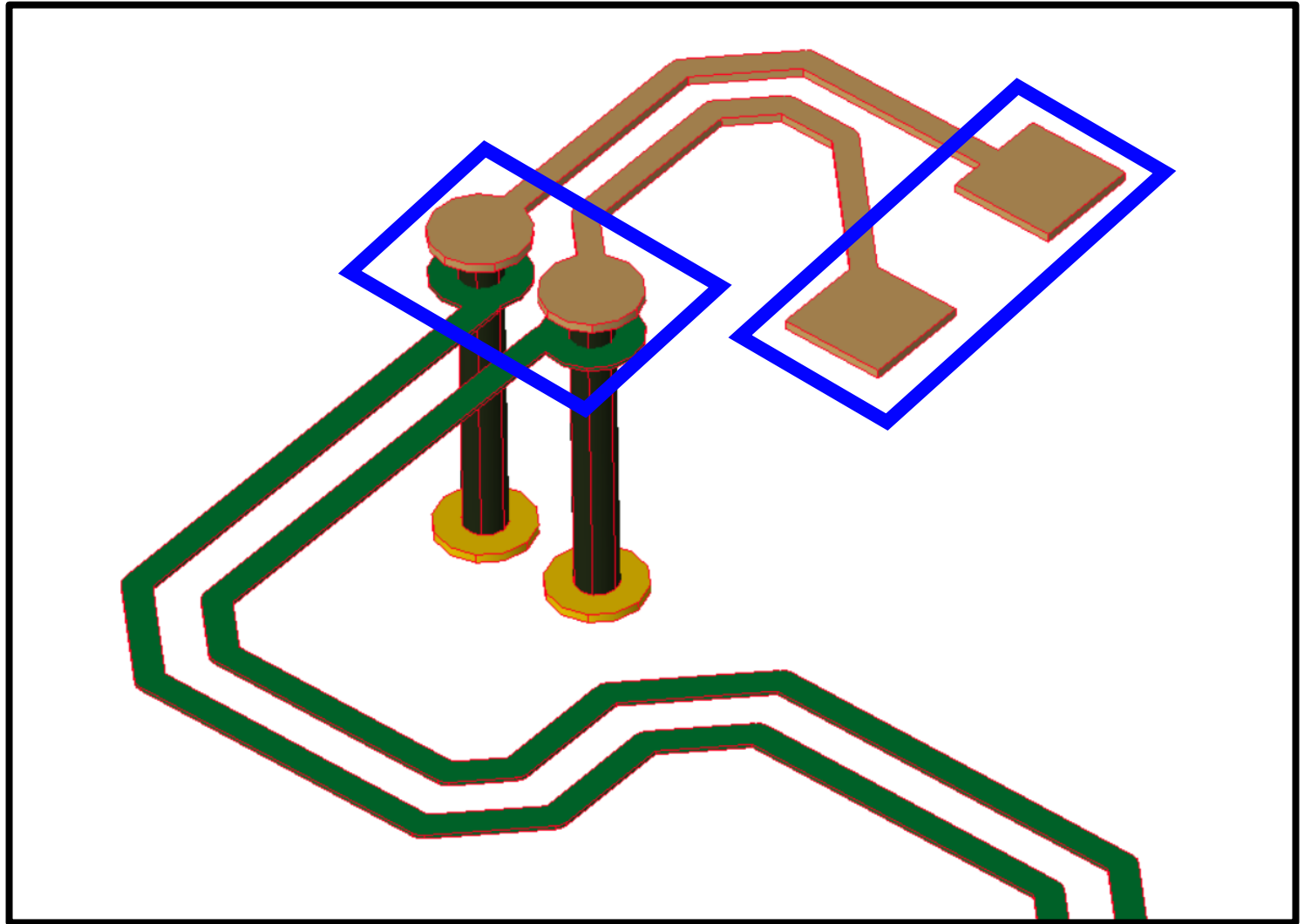
$Z_{\text{ref}}$ : 100  $\Omega$

Expected:

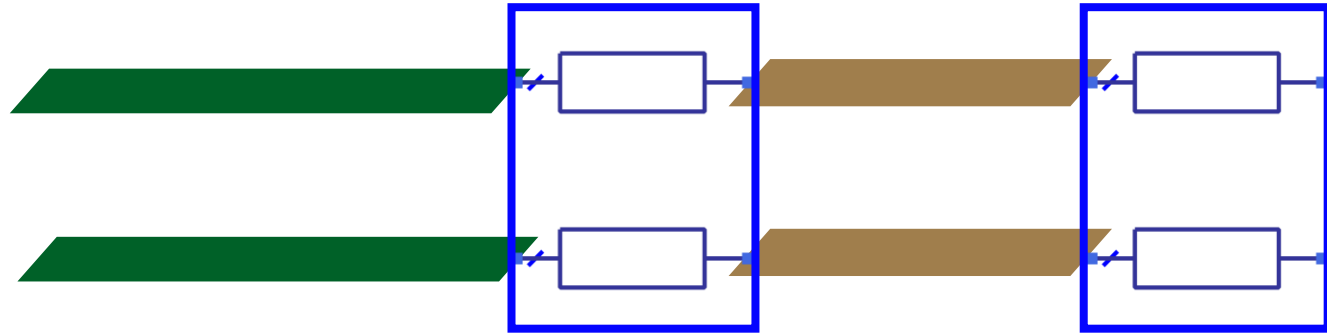
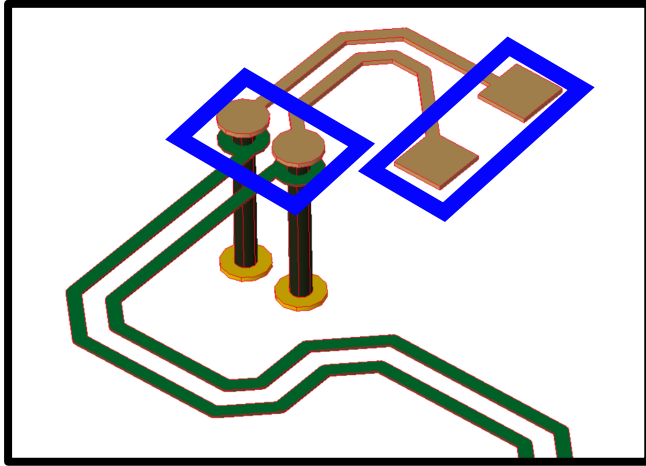
$S_{\text{DD11}} > -20 \text{ dB}$



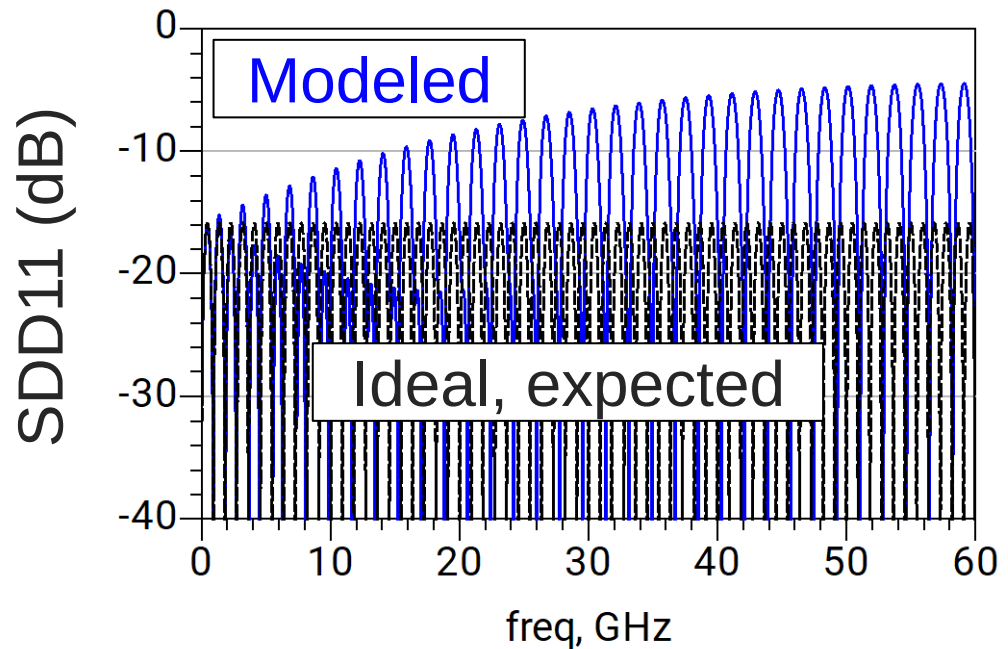
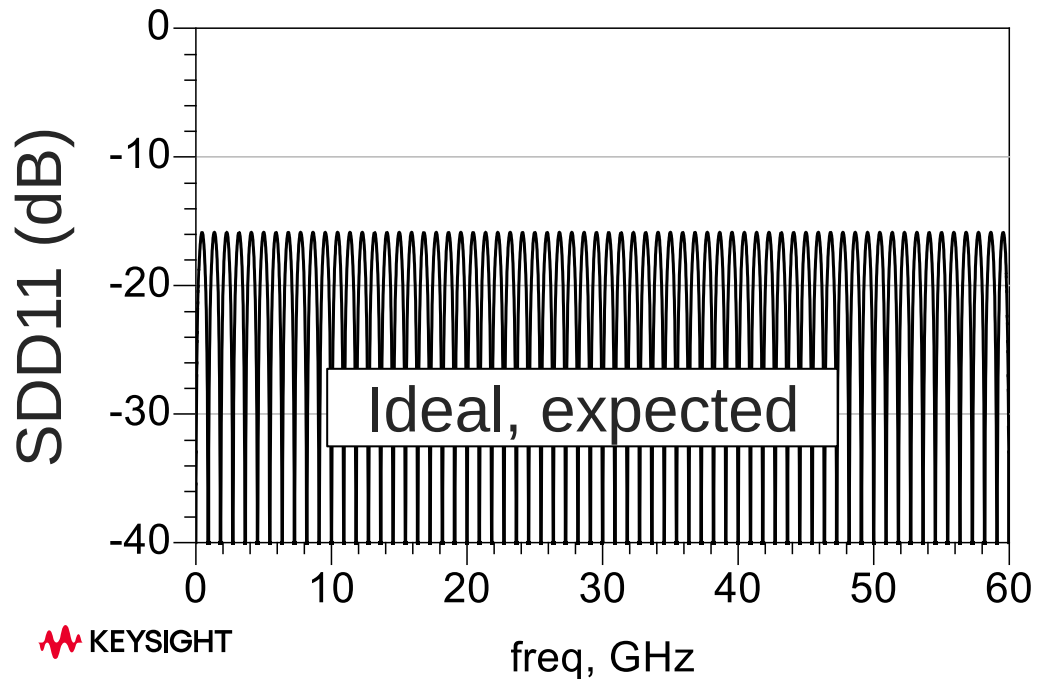
The probable cause is the small impedance discontinuities when the signal encounters the pads



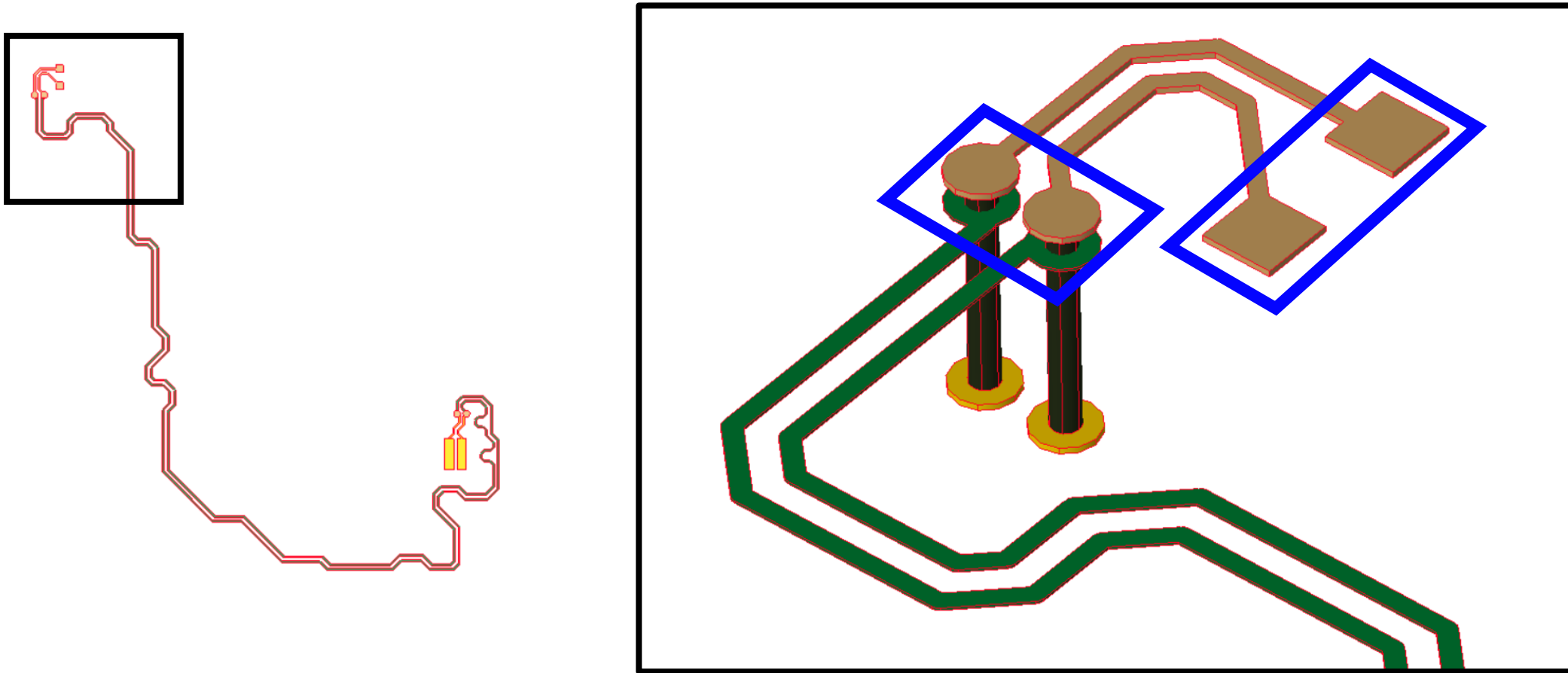
# T-Line Modeling Confirms Small Zs Causing Ramp-up



The transmission line model confirms that it is the small impedance discontinuities that are causing the ramp-up.



# Discontinuities: Unavoidable and Critical to Include in Analysis



The small impedance discontinuities are unavoidable in the real world, and we should calibrate our expectation of SDD1.

### 3 Typical Unexpected Behaviors and Fixes in PCIe SI Analysis

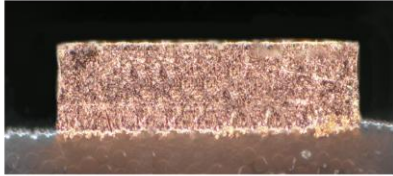
Expected

Resulted

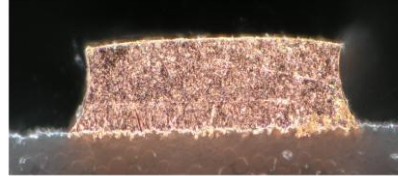
Cause

Fix

$Z_{diff}$



85  $\Omega$

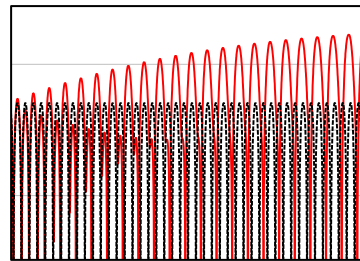
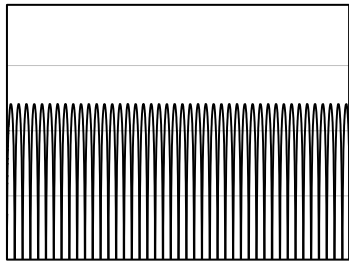


89  $\Omega$

$Z_{diff}$  is higher than expected because of etch-back

- Reduce starting spacing
- Increase starting trace width

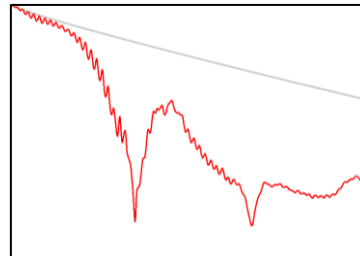
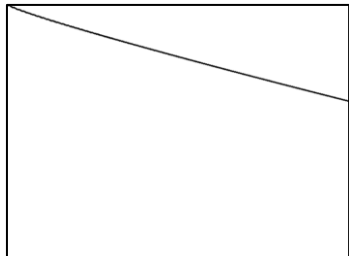
SDD11



SDD11 ramps up because of small impedance discontinuity

- Maintain controlled impedance
- Include the impact in SI analysis

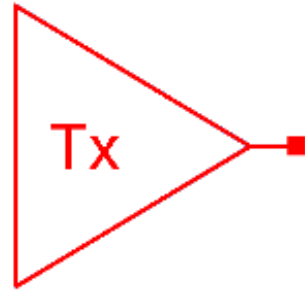
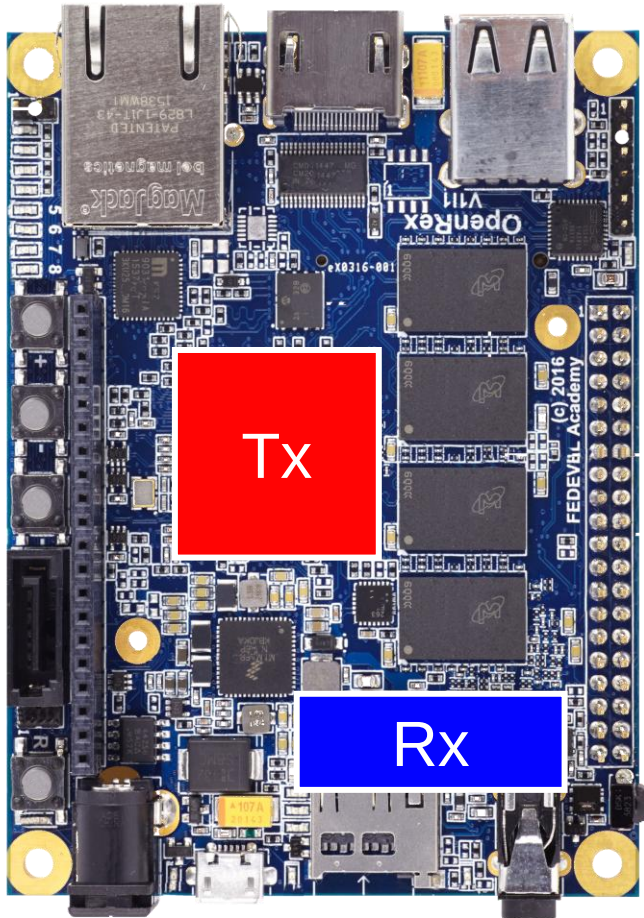
SDD21



SDD21 has a dip because of stub resonance

- Remove stub with back-drilling

# Recap PCIe Gen 5 SI Analysis – from Layout to Eye Diagram

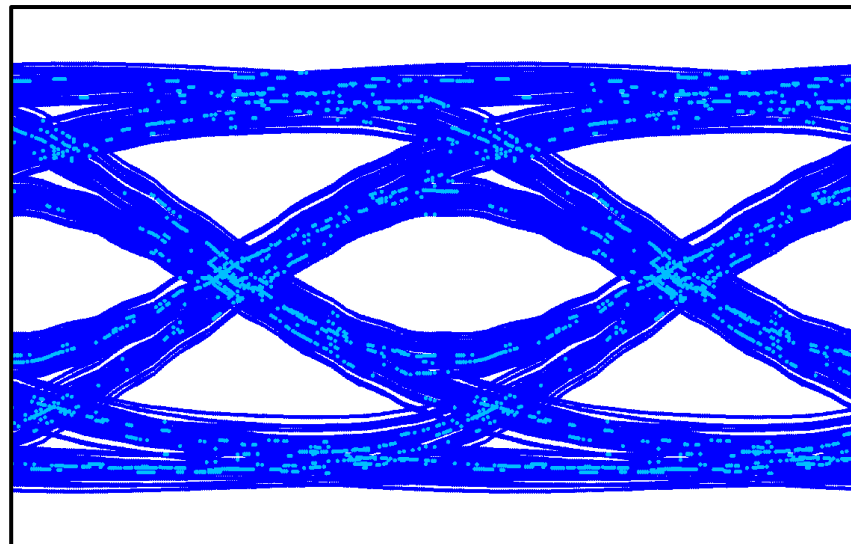


PCIe Gen 5 Transmitter

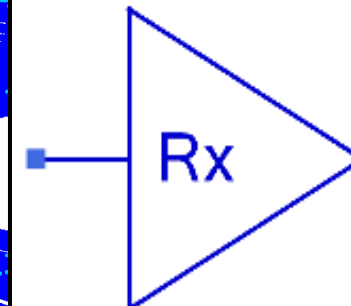
Modulation: NRZ

Data rate: 32 Gbps

Nyquist frequency: 16 GHz

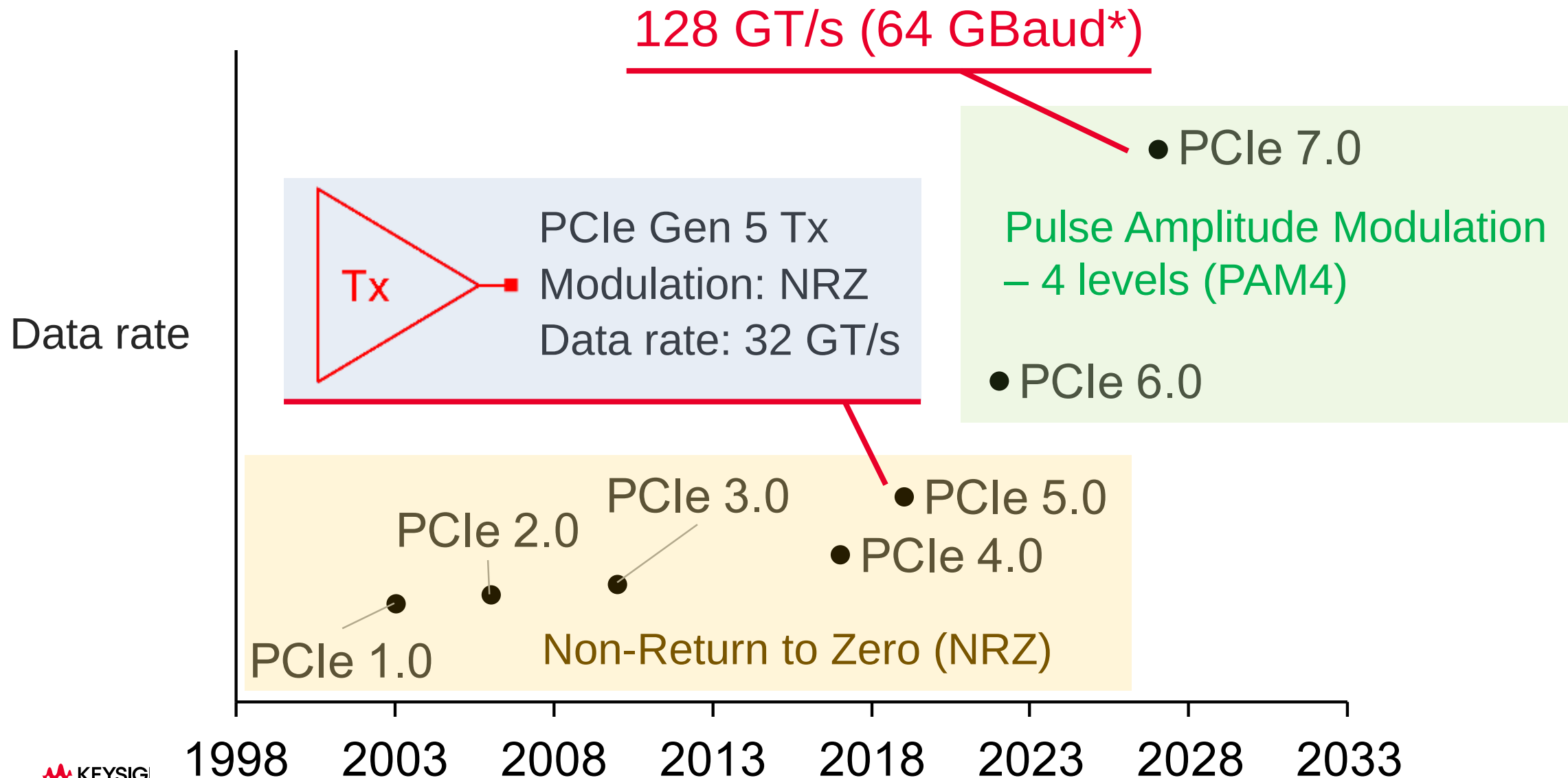


Equalization: N/A

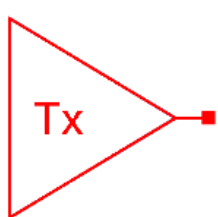


Picture credit: <https://www.imx6rex.com/open-rex/>

# What Does it Take to Reach 128 GT/s?



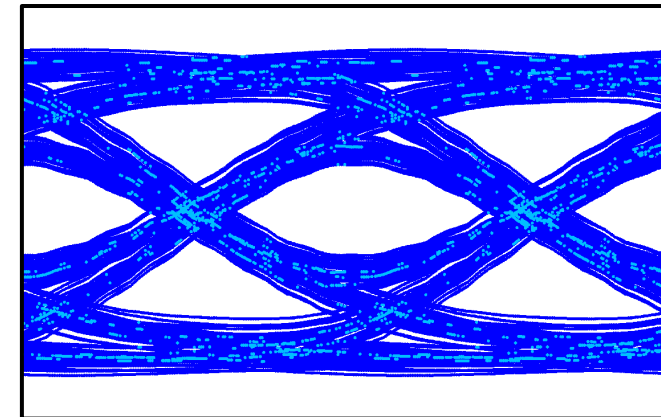
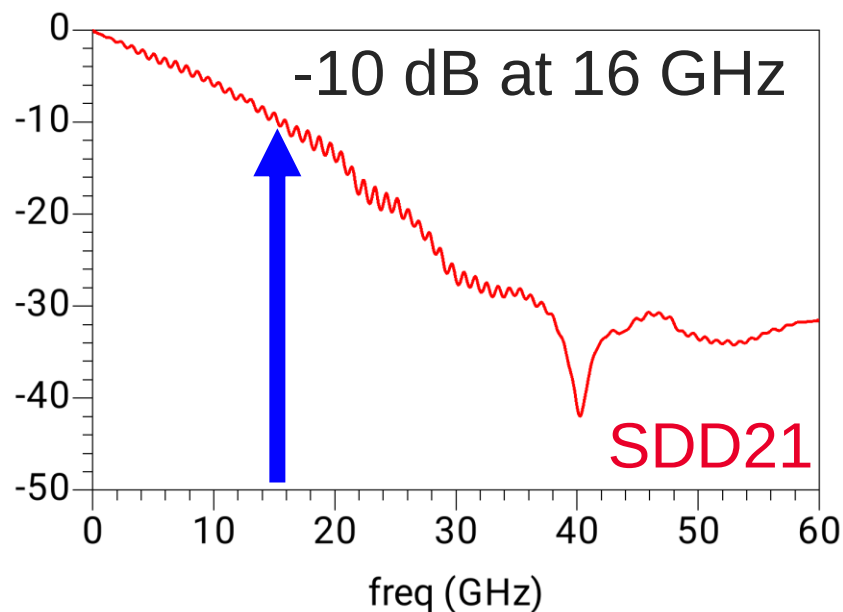
# Need to Find Another Ways to Reach the Higher Data Rate



PCIe Gen 5

Data rate: 32 GT/s

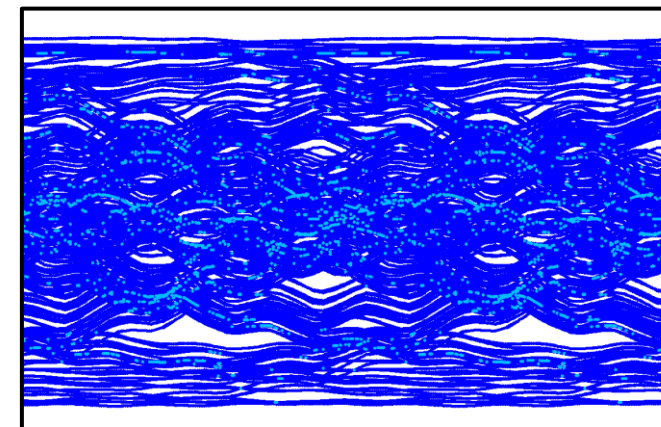
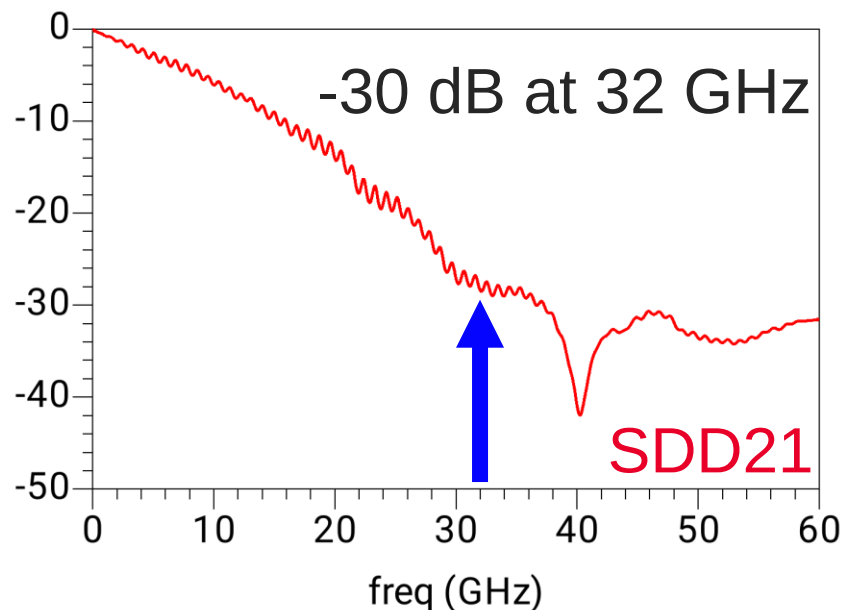
Nyquist frequency: 16 GHz



NRZ Gen 6

Data rate: 64 GT/s

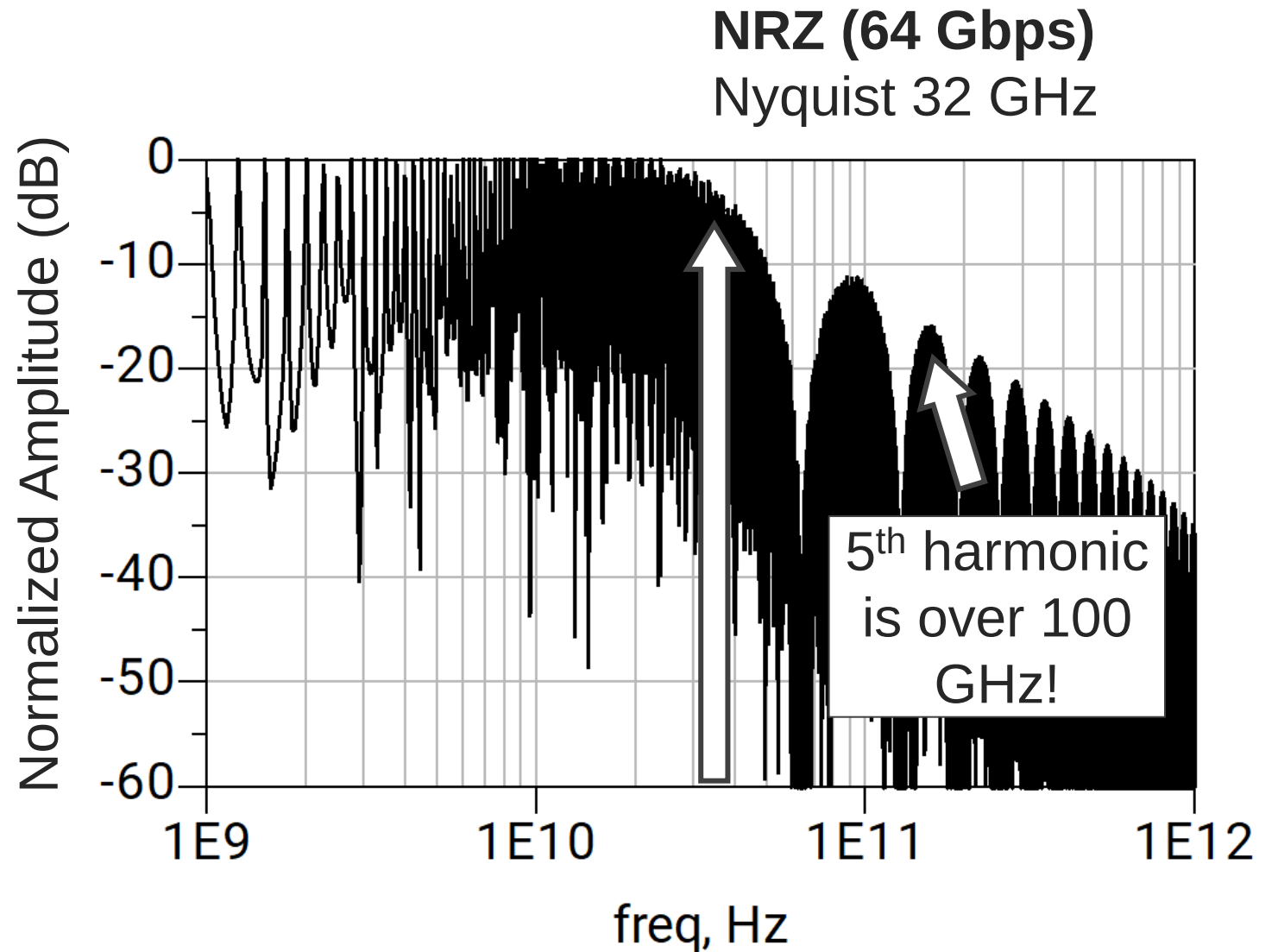
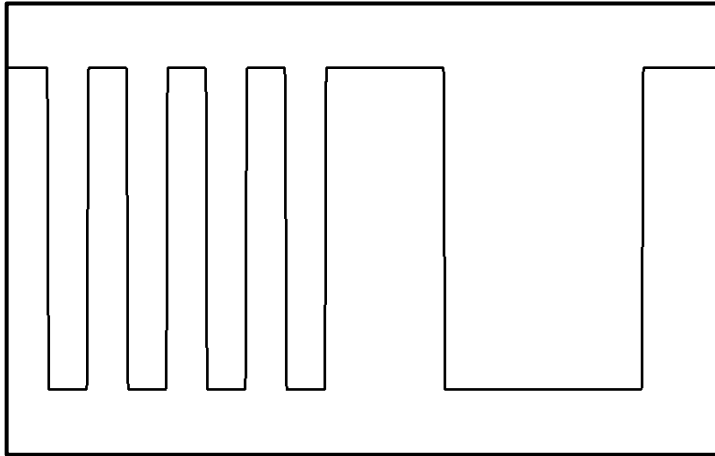
Nyquist frequency: 32 GHz



NRZ reaches its limit as the data rate increases. To reach higher rates, we need to lower the Nyquist.

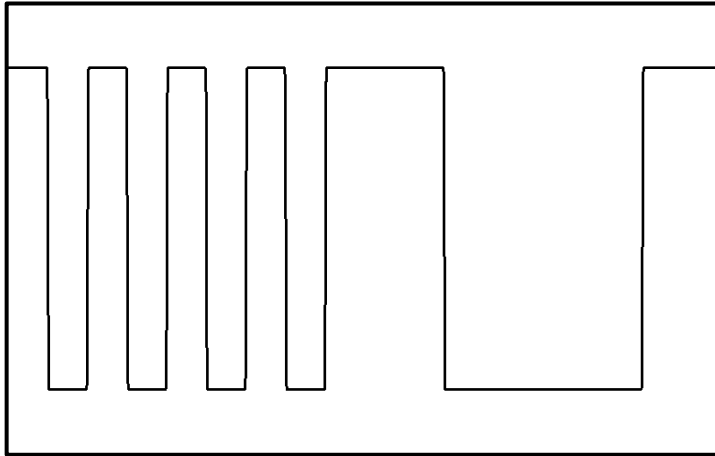
# Fight the High Loss at High Frequency with Modulation

NRZ: 1 bit per unit interval

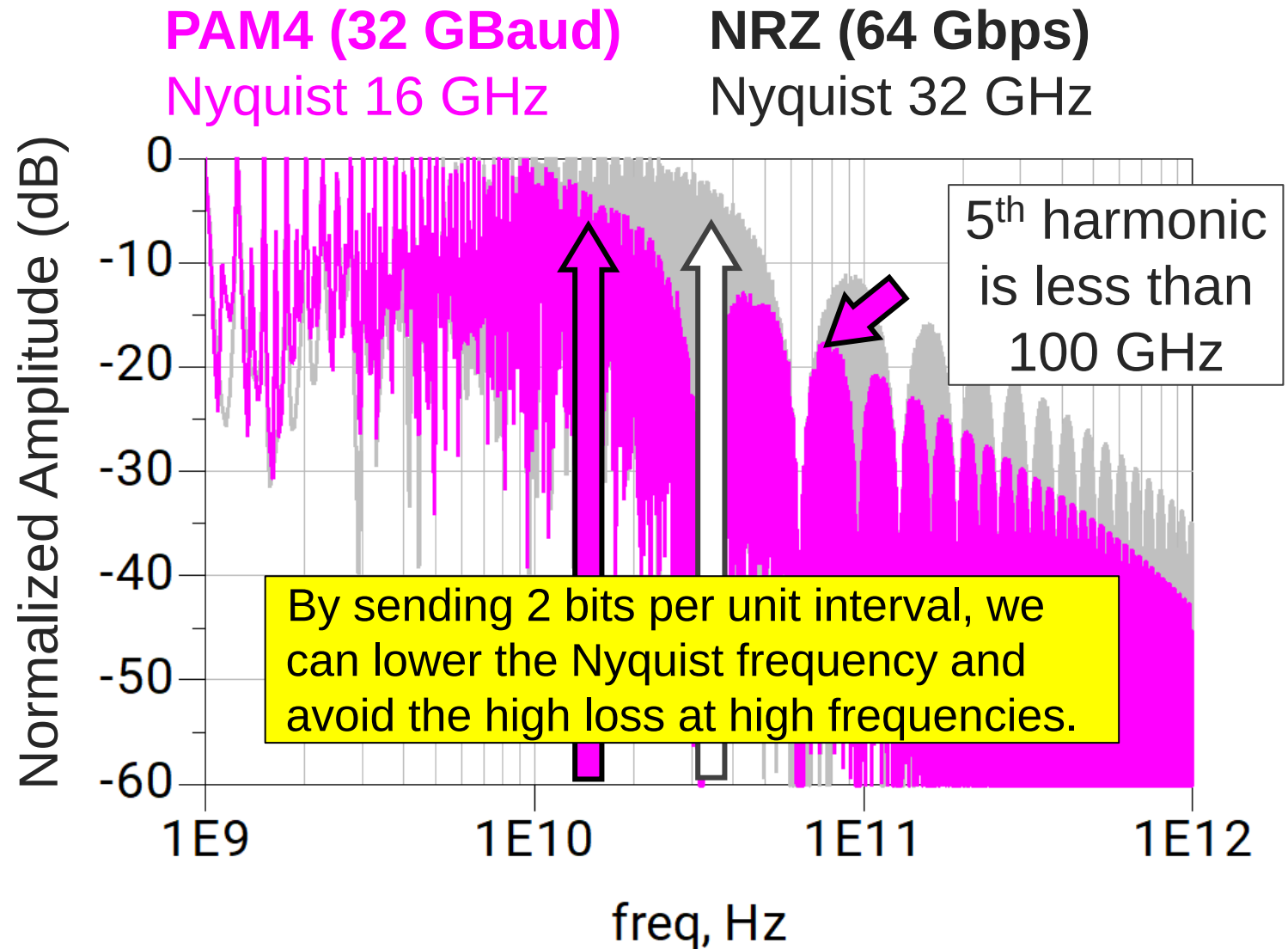
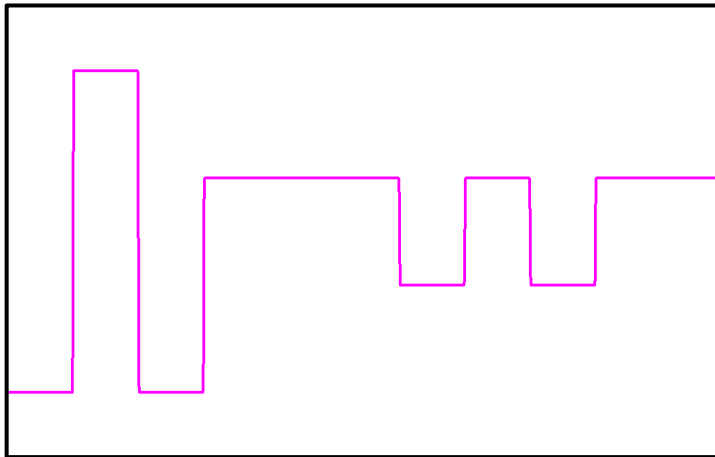


# Fight the High Loss at High Frequency with Modulation

NRZ: 1 bit per unit interval

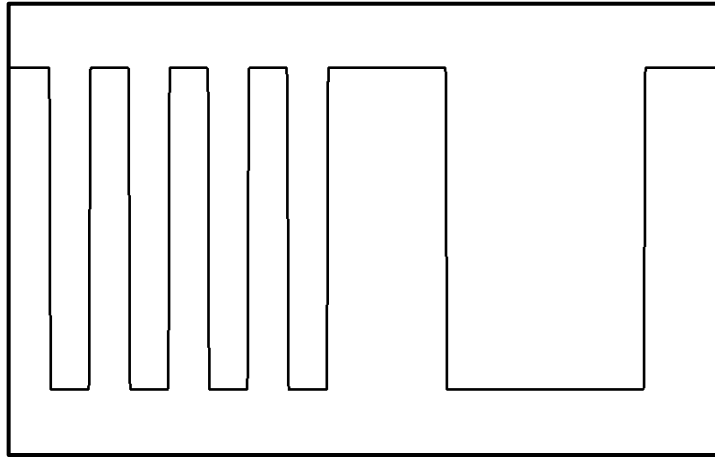


PAM4: 2 bits per unit interval



# PAM4 Lowers Nyquist Freq and Has a Larger Unit Interval

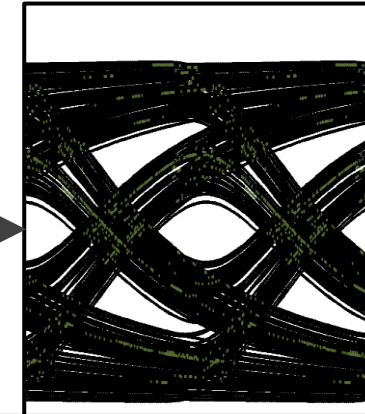
NRZ: 1 bit per unit interval



NRZ (64 Gbps)

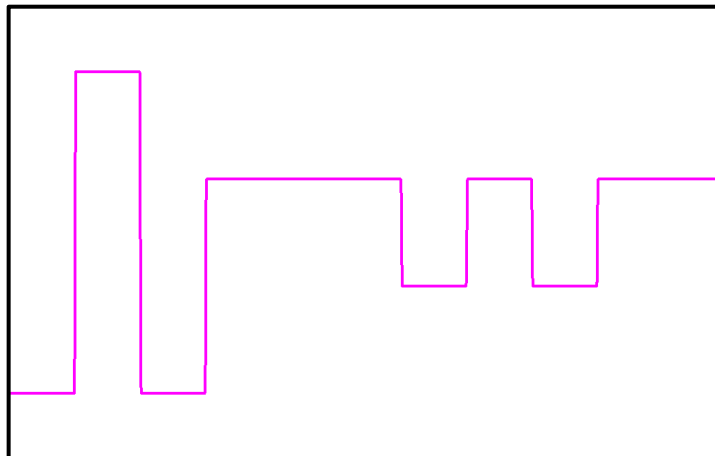
Example channel

2UI = 31.25 psec



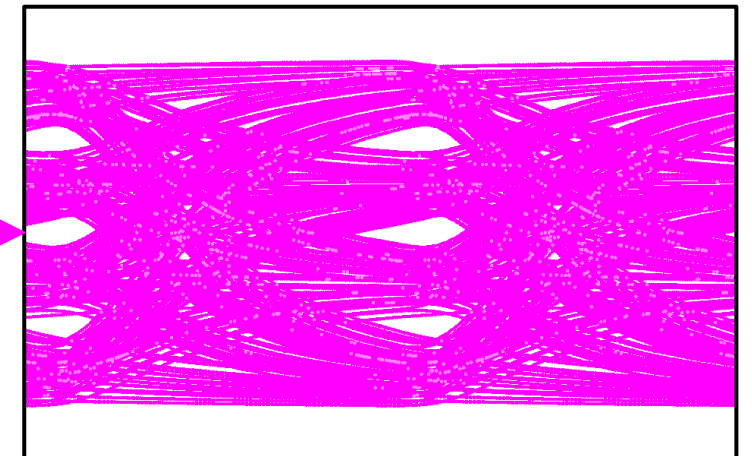
By sending 2 bits per unit interval, PAM4's unit interval is twice as large as that of NRZ at the same data rate.

PAM4: 2 bits per unit interval



PAM4 (32 GBaud)

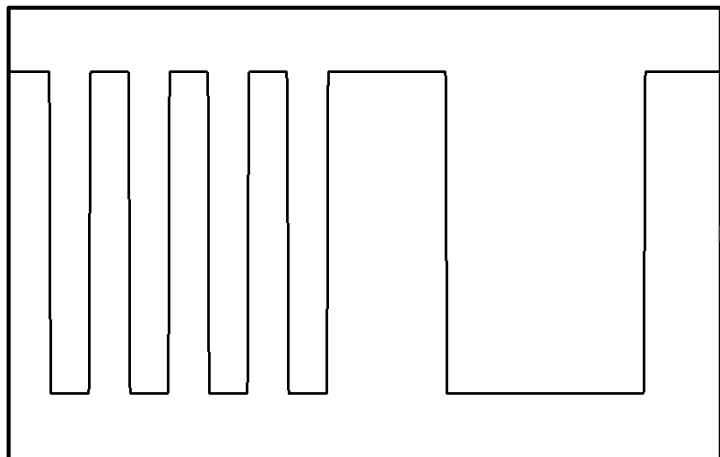
Example channel



2UI = 62.5 psec

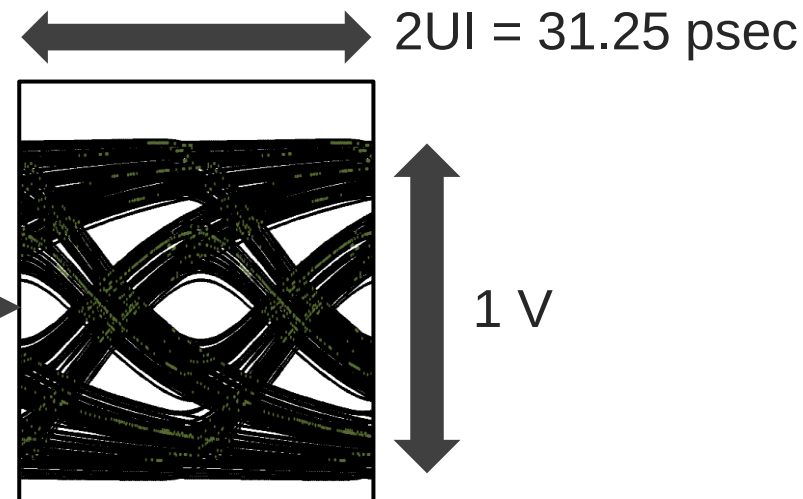
# PAM4 Lowers Nyquist Freq but Has Smaller Voltage Swing

NRZ: 1 bit per unit interval



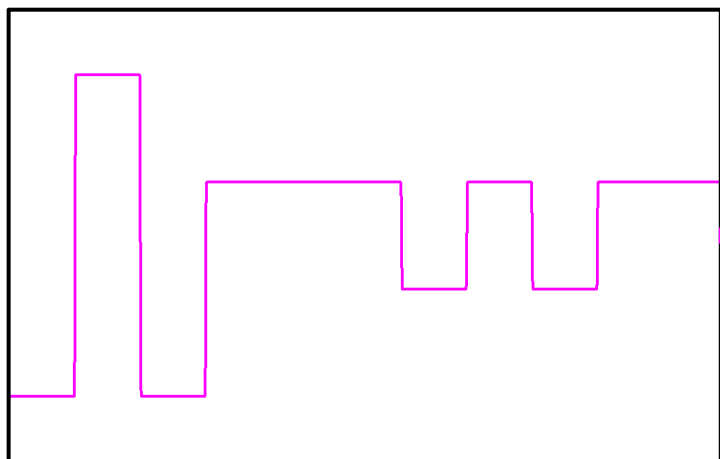
NRZ (64 Gbps)

Example channel



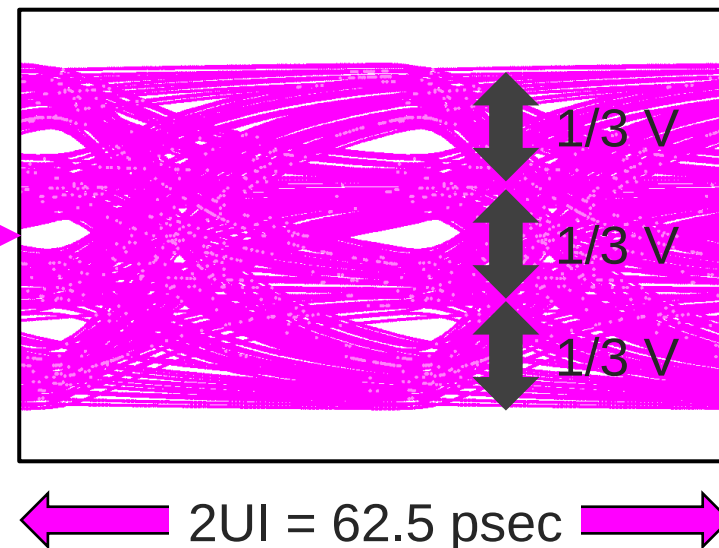
By squeezing 2 bits in the same voltage swing, PAM4 signals have a smaller eye height to work with.

PAM4: 2 bits per unit interval



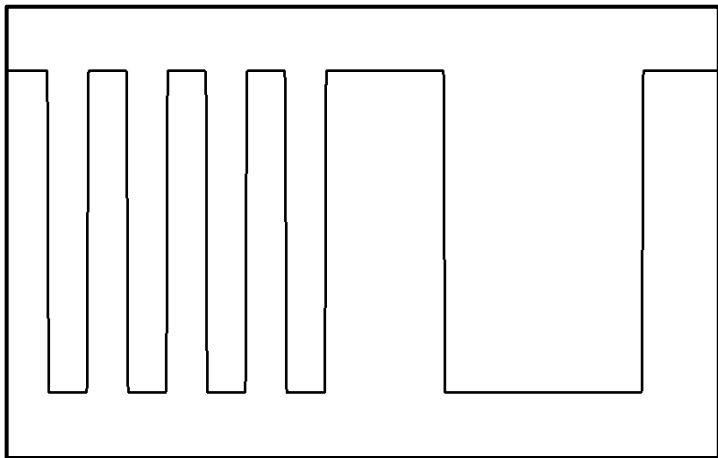
PAM4 (32 GBaud)

Example channel

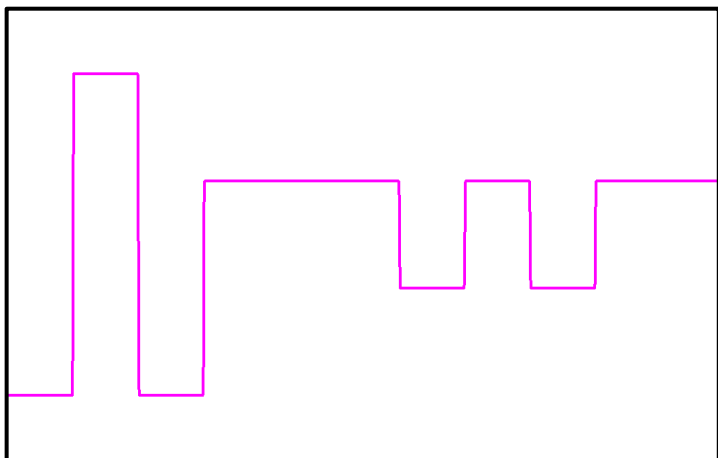


# PAM4 Lowers Nyquist Freq but Loses SNR by ~9.5 dB

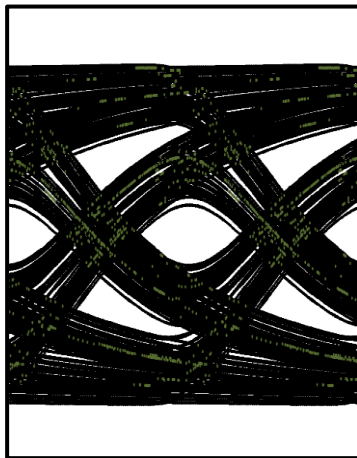
NRZ: 1 bit per unit interval



PAM4: 2 bits per unit interval



NRZ (64 Gbps)



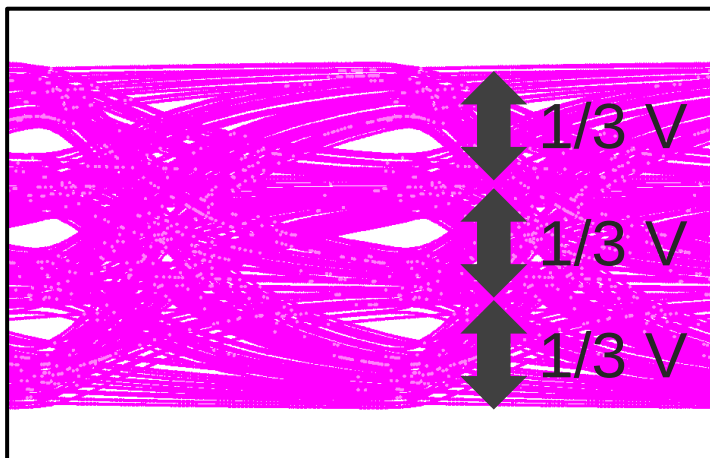
1 V

$$SNR_{NRZ} = \frac{EyeHeight_{NRZ}}{Noise}$$

$$SNR_{PAM4} = \frac{EyeHeight_{PAM4}}{Noise}$$

$$SNR\ Loss = \frac{SNR_{PAM4}}{SNR_{NRZ}} = 20\log\left(\frac{1}{3}\right)$$

PAM4 (32 GBaud)



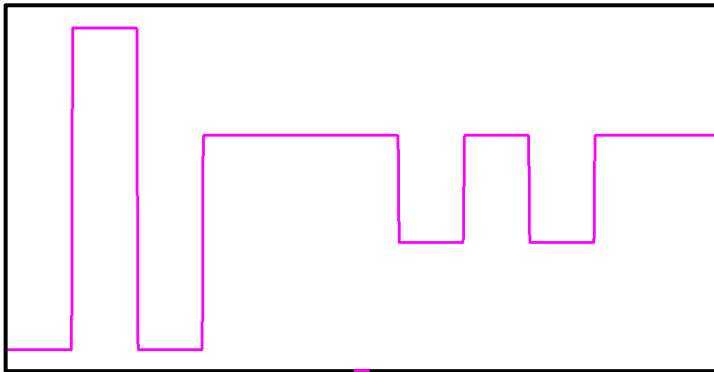
1/3 V  
1/3 V  
1/3 V

SNR Loss ~ 9.5 dB

By squeezing 2 bits in the same voltage swing, PAM4 has a smaller eye height to work with. The signal-to-noise ratio loss is ~9.5 dB.

# Gen 7 (128 GT/s) Expects a Closed Eye at the Receiver

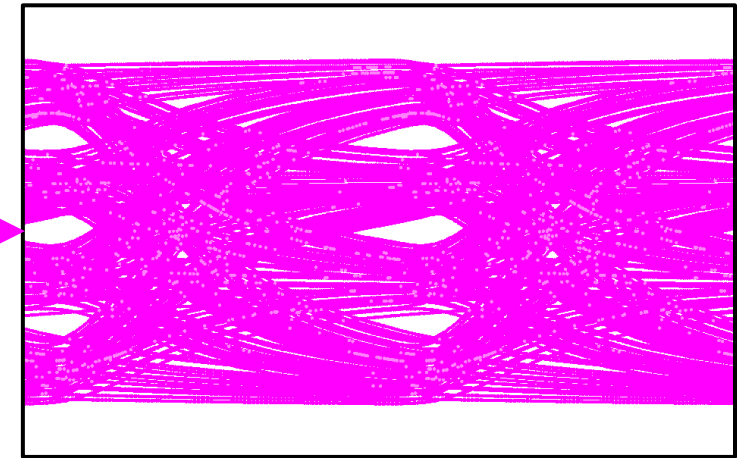
PAM4: 2 bits per unit interval



Example channel

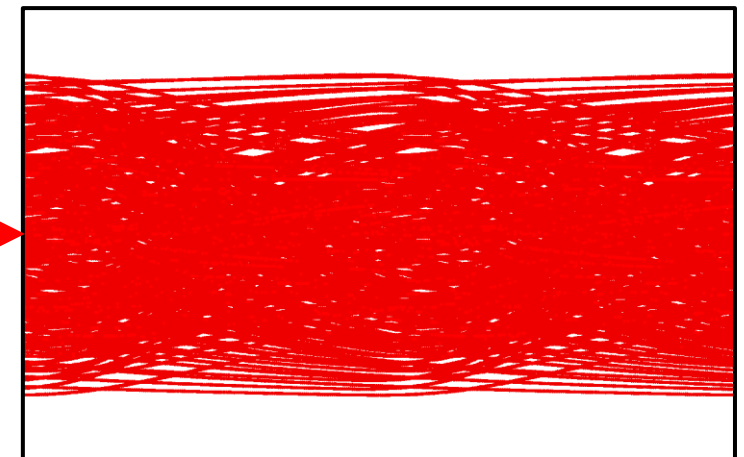
64 GT/s

Gen 6 PAM4 (32 GBaud)



128 GT/s

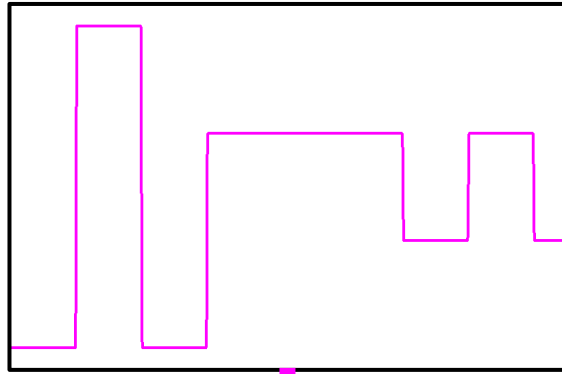
Gen 7 PAM4 (64 GBaud)



At Gen 7 data rate (128 Gbps), the received eye is assumed to be closed. It is necessary to have equalizations to open up the eye.

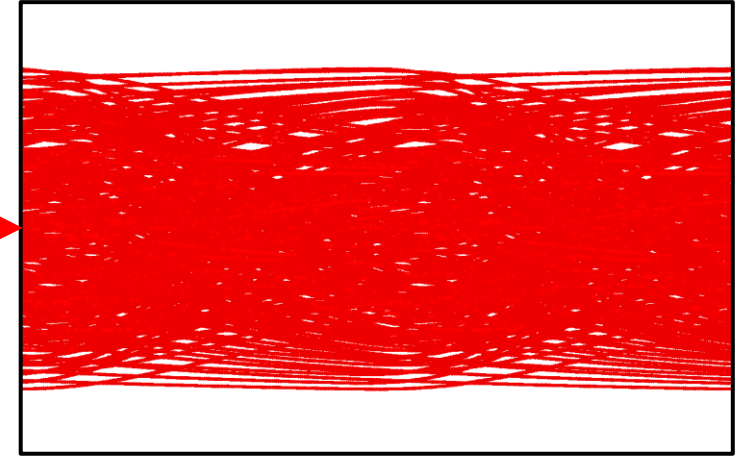
# Gen 7 Required all the Equalization help It needs

64 GBaud PAM4 (128 GT/s)



Example channel

Gen 7 PAM4 (64 GBaud)



Because of Gen 7's high data rate, equalizations at the Tx, Rx are all required to open the eye at the receiver.

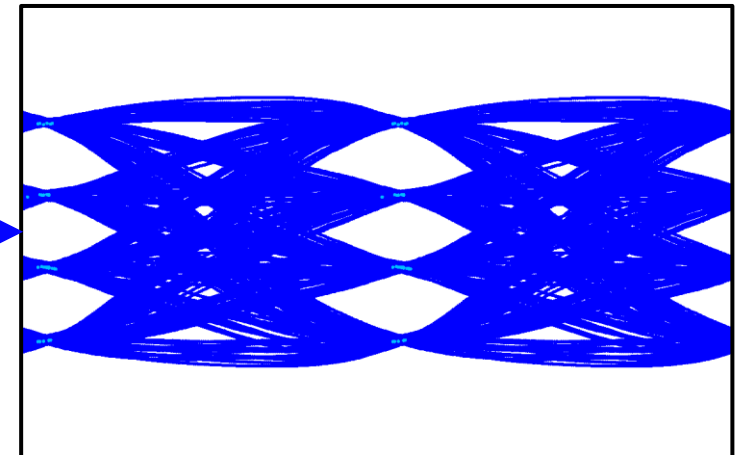
Tx  
FFE

Example  
channel

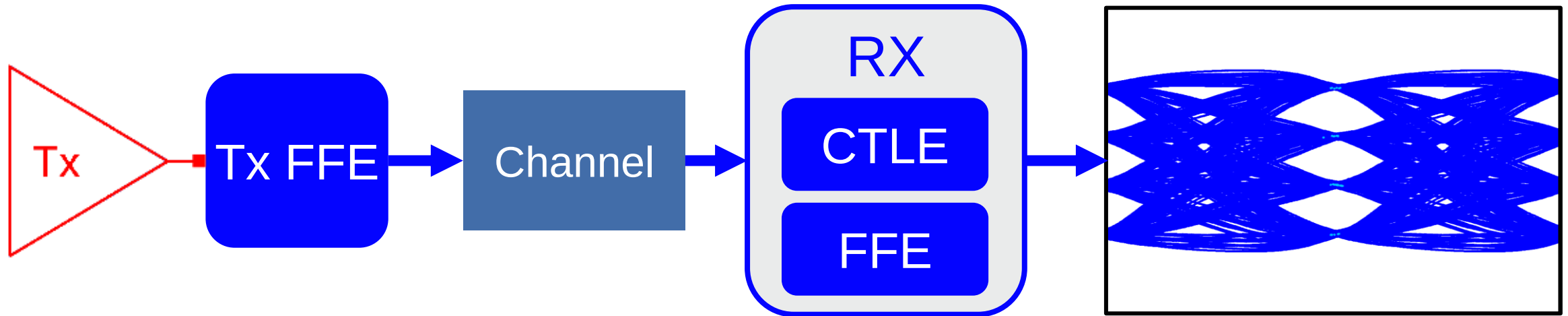
RX

CTLE

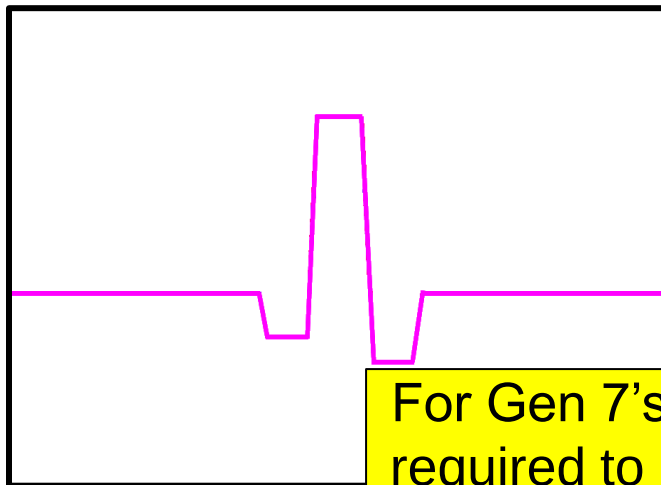
FFE



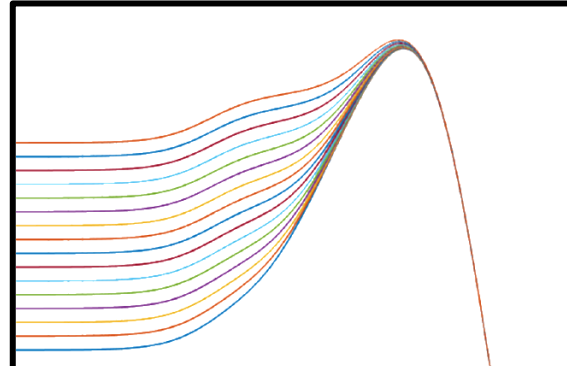
# PCIe Gen 7 Standard Provides Equalization Presets



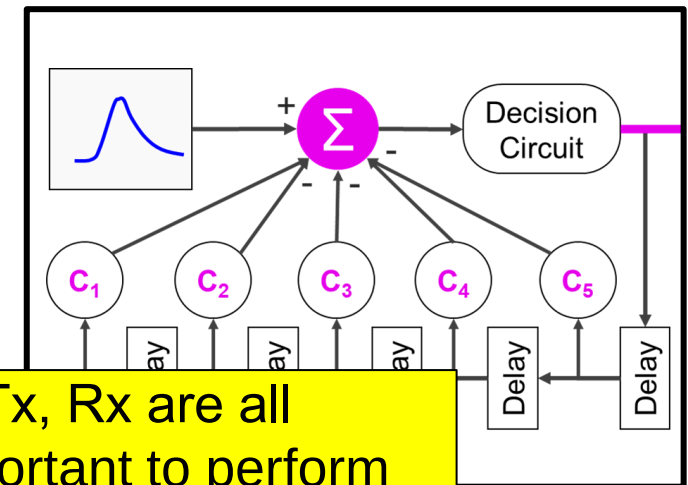
11 Tx Presets



16 Rx CTLE Presets

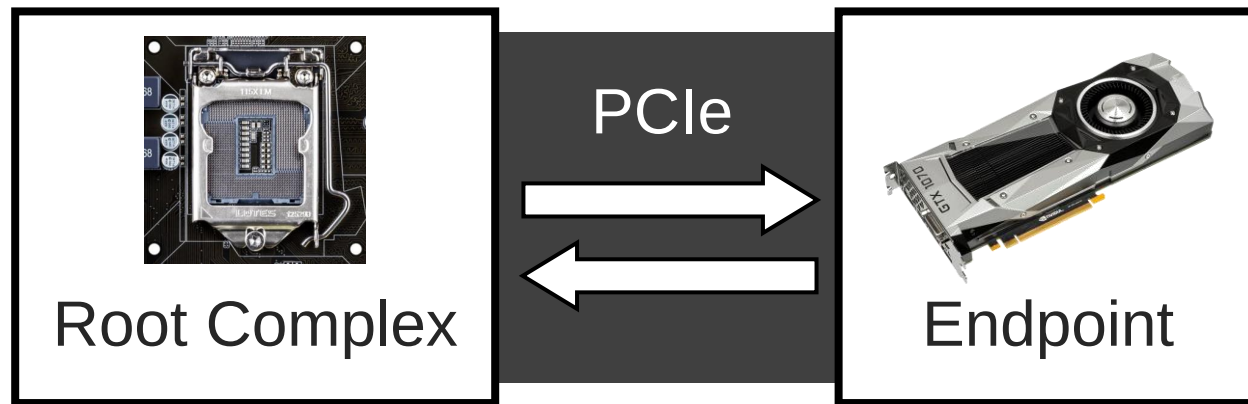


Rx FFE+DFE

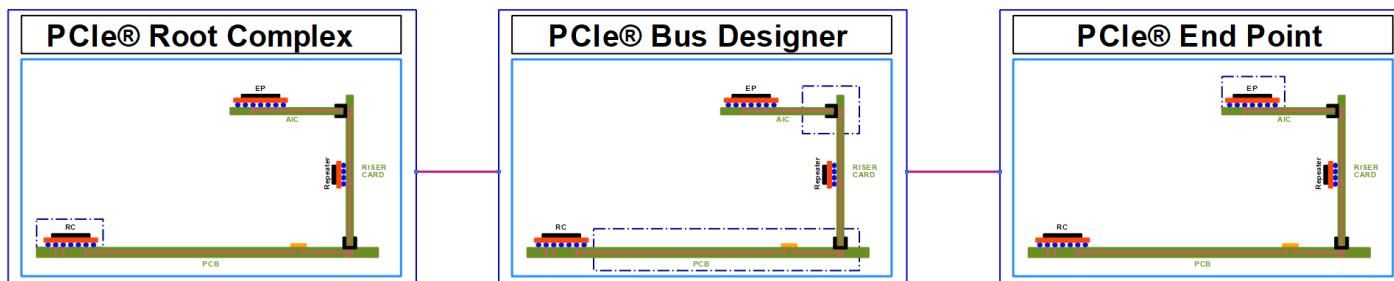


For Gen 7's high data rate, equalizations at the Tx, Rx are all required to open the eye at the receiver. It is important to perform end-to-end system analysis.

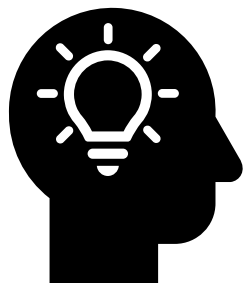
# Key Attributes to a PCIe System Analysis Software



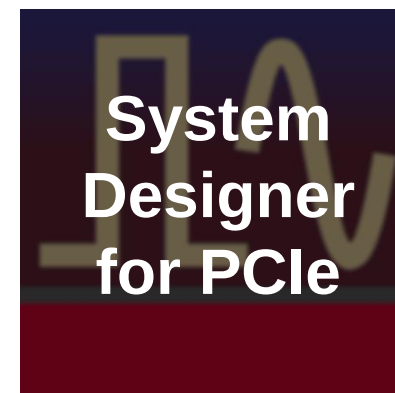
**Standard-focused and Compliance**  
Let the software work for you



**End-to-end System Analysis**  
Identify problems early, reproduce existing problems

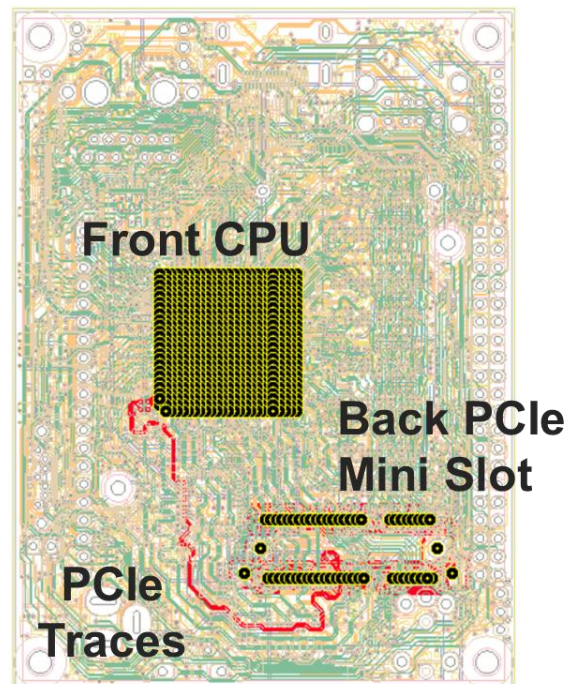
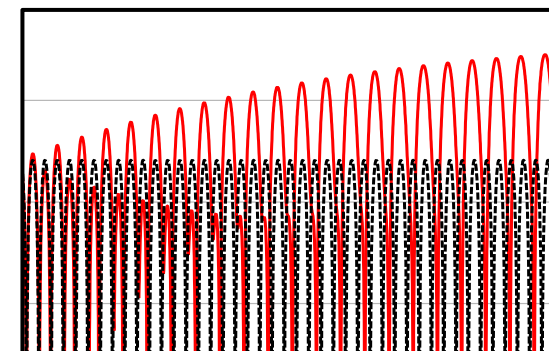
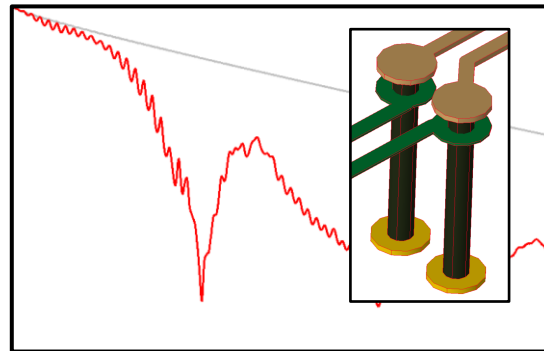
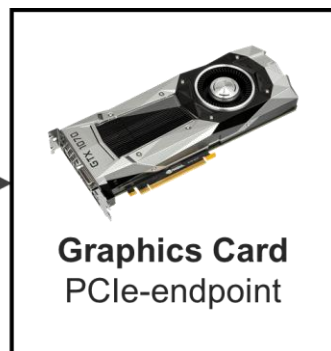
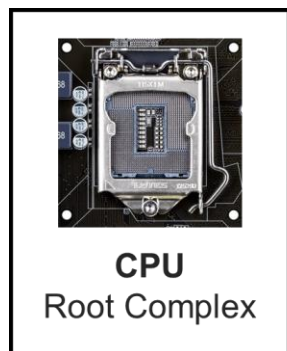


**Usability and Integration**  
Don't work for the computer

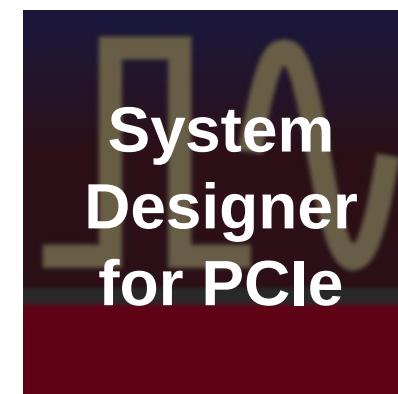
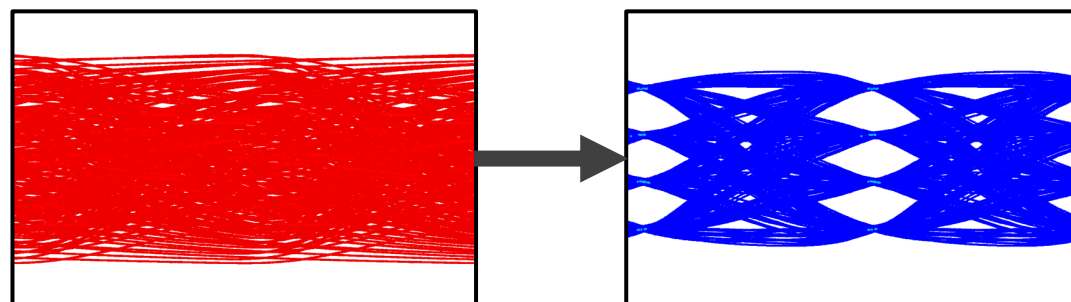


# System Designer for PCIe Demo Video

# Recap of Our PCIe Journey to the Future



## Gen 7 PAM4 (64 GBaud)



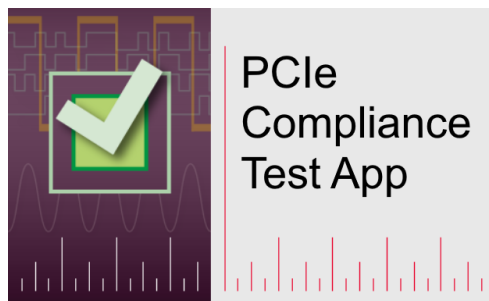
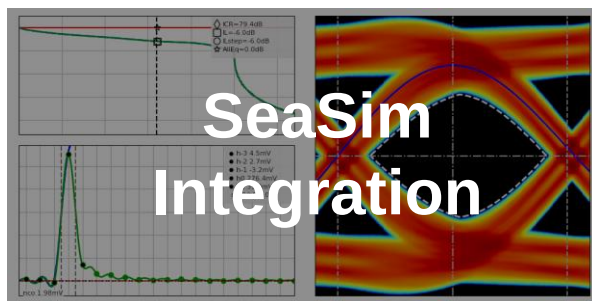
Rule #9: Anticipate Before You Measure or Simulate

System Design for PCIe is not a simple task.  
You need a great partner!

# Why You Should Design PCIe Systems with Keysight W3651B

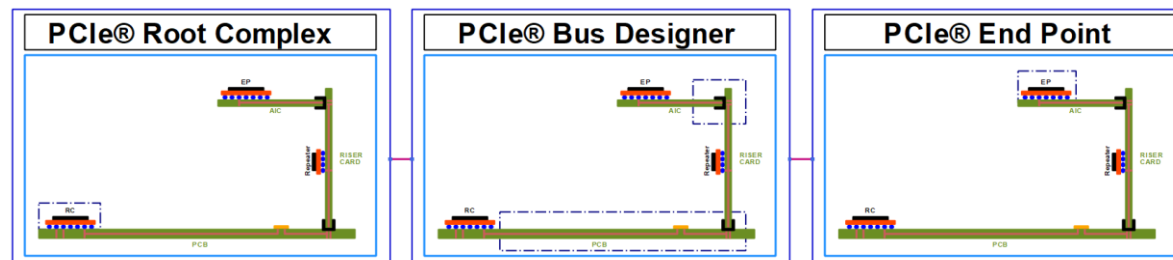
## Standard-focused and Compliance

Improve productivity, ensure interoperability



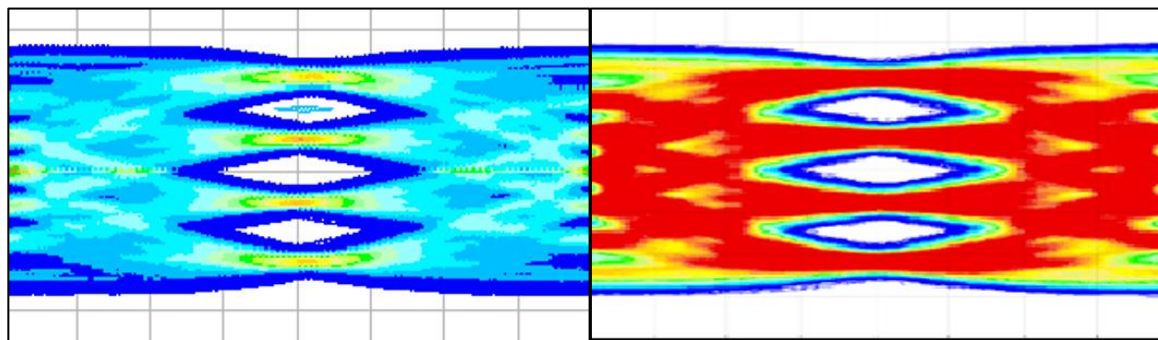
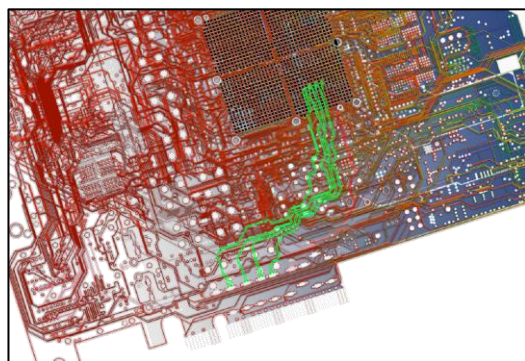
## End-to-end PCIe System Analysis

Identify system level issues, optimize performance



## Simulation and Measurement Solutions

Enable practical design validation, secure first-pass design success



Simulate your PCIe system with ADS2025 Update 2

# Thank you