KEYSIGHT

UCIe vs. BoW: Your Essential Guide to Choosing the Right Chiplet Standard

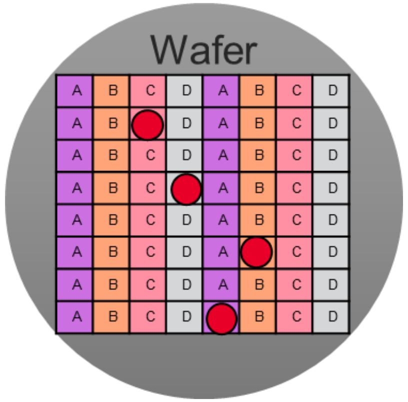
[Your Name | Title]

Agenda: Comparing UCIe and BoW in a Case Study

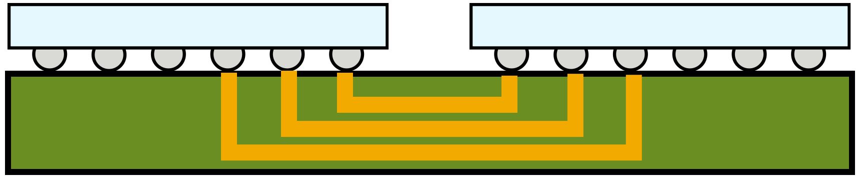
Why is chiplet on the rise?

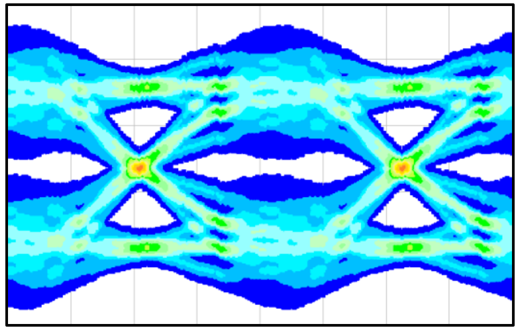
Comparison between UCIe and BoW

The importance of signal integrity and EDA in the chiplet era



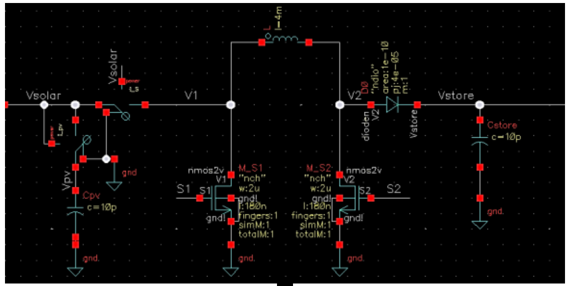
Example channel



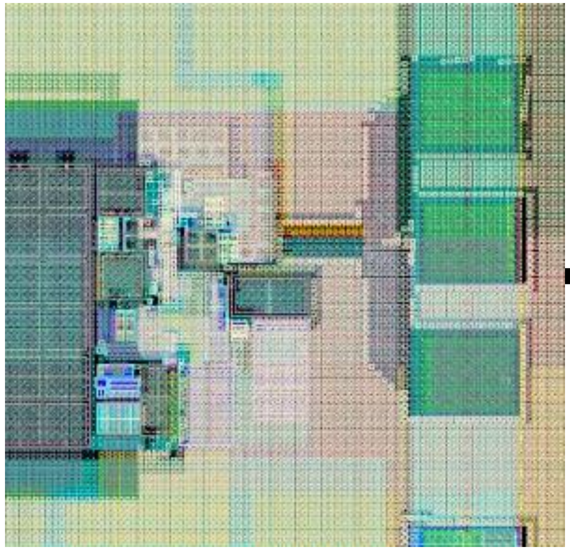


IC Design from the Schematic, Wafer to the Package

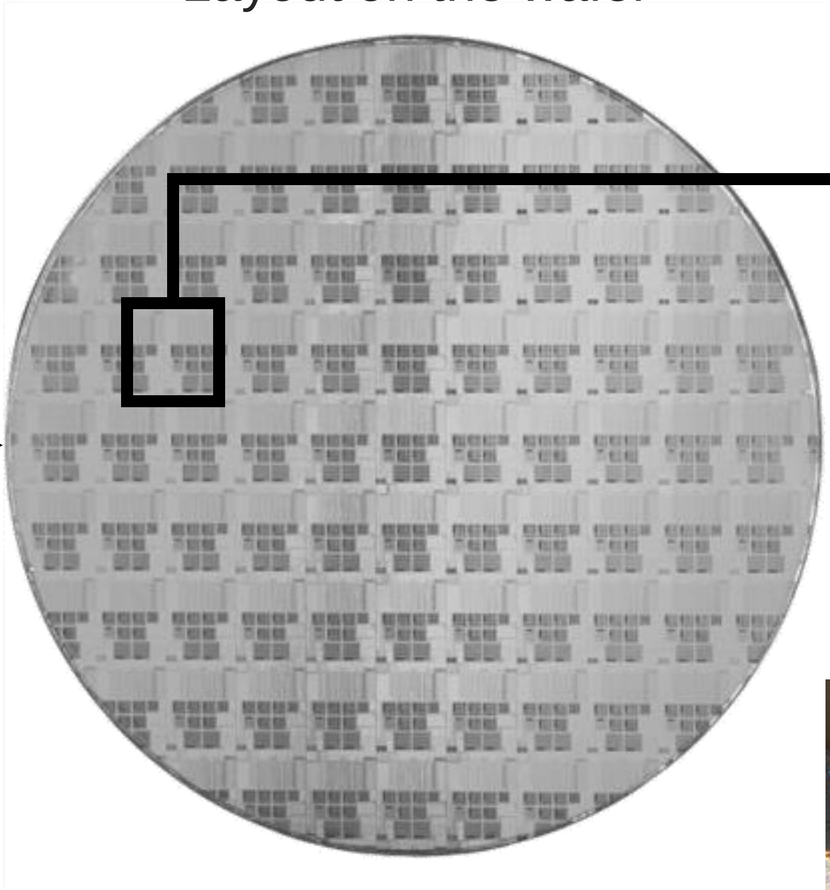
Schematic



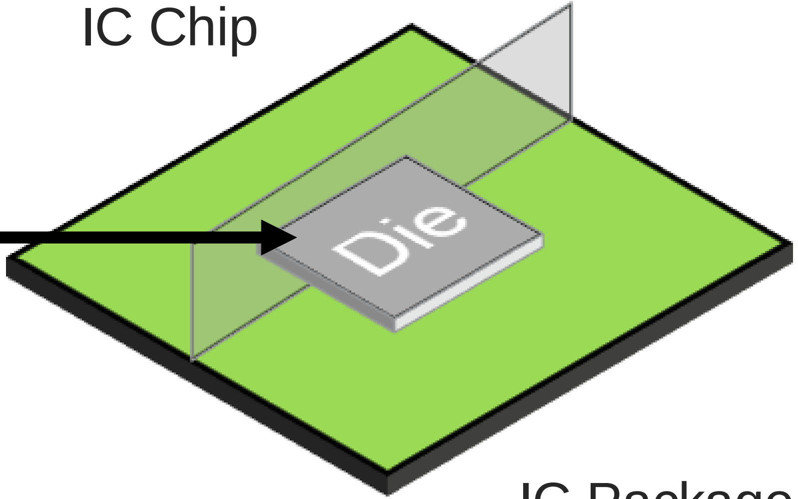
Layout



Layout on the wafer

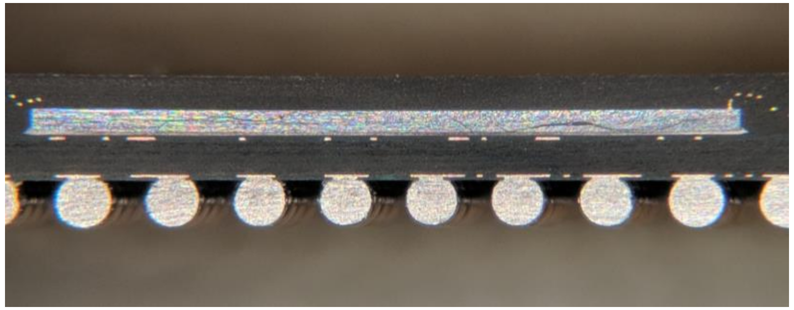


IC Chip



IC Package

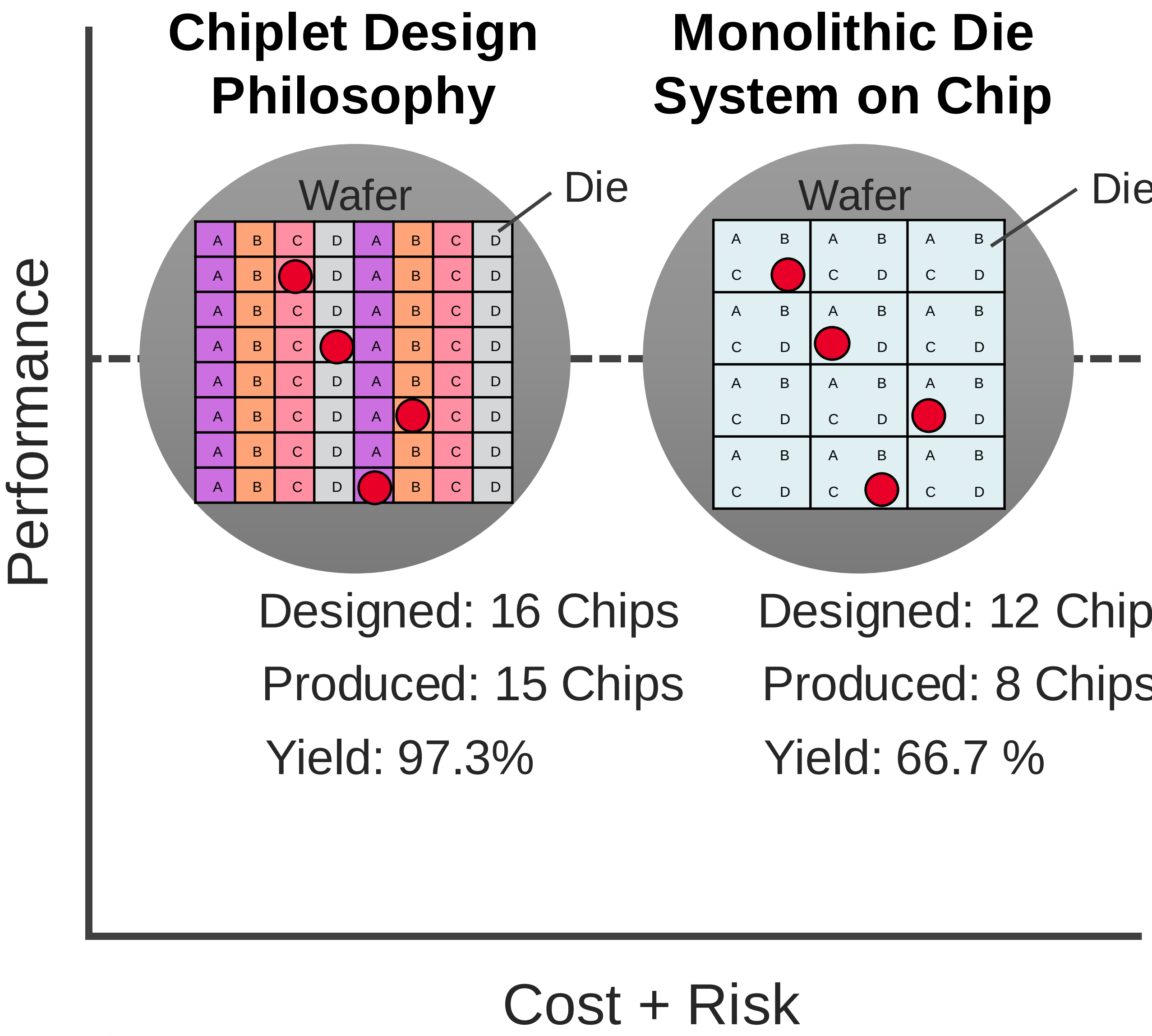
Cross-sectional view



Picture credit: https://miscircuitos.com/design-process-of-chips-asics-flow-from-design-to-tapeout/

Picture credit: https://twitter.com/TubeTimeUS/status/1113567854698225664

Chiplets Improve the Cost vs. Performance of Chip Production



Monolithic approach

4 different functions in one big die

Fn: A (CPU)	Fn: B (Memory)
Fn: C (I/O)	Fn: D (Power)

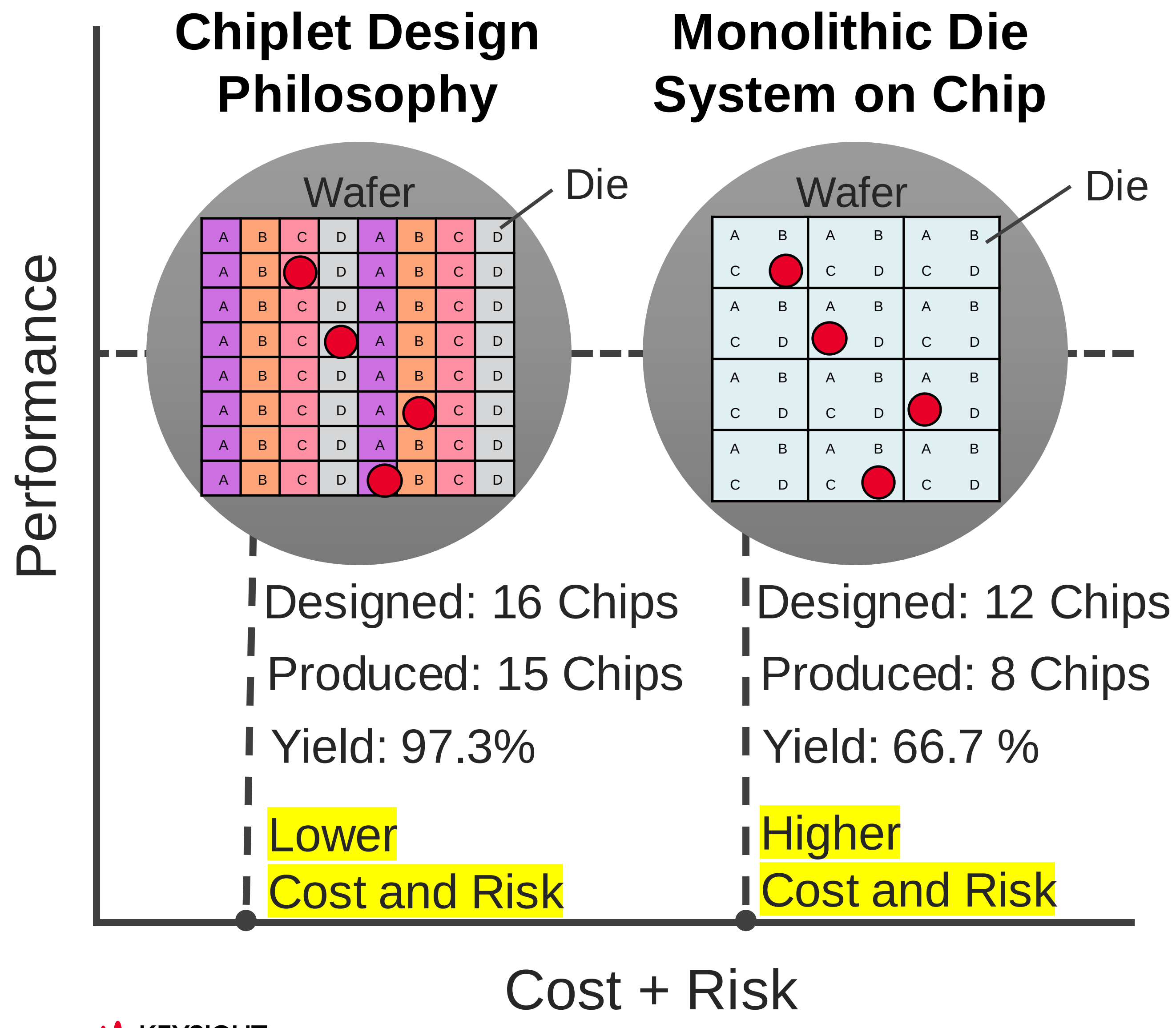
Chiplet approach

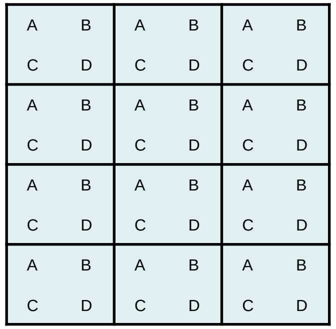
4 different dies for 4 different functions

Die: A	Die: B
Die: C	Die: D

KEYSIGHT

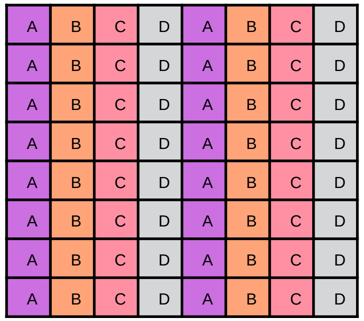
Chiplets Improve the Cost vs. Performance of Chip Production





Monolithic Die SoC

- Requires large mask (reticle) close to fabrication limit
- Has a lower yield
- Higher cost

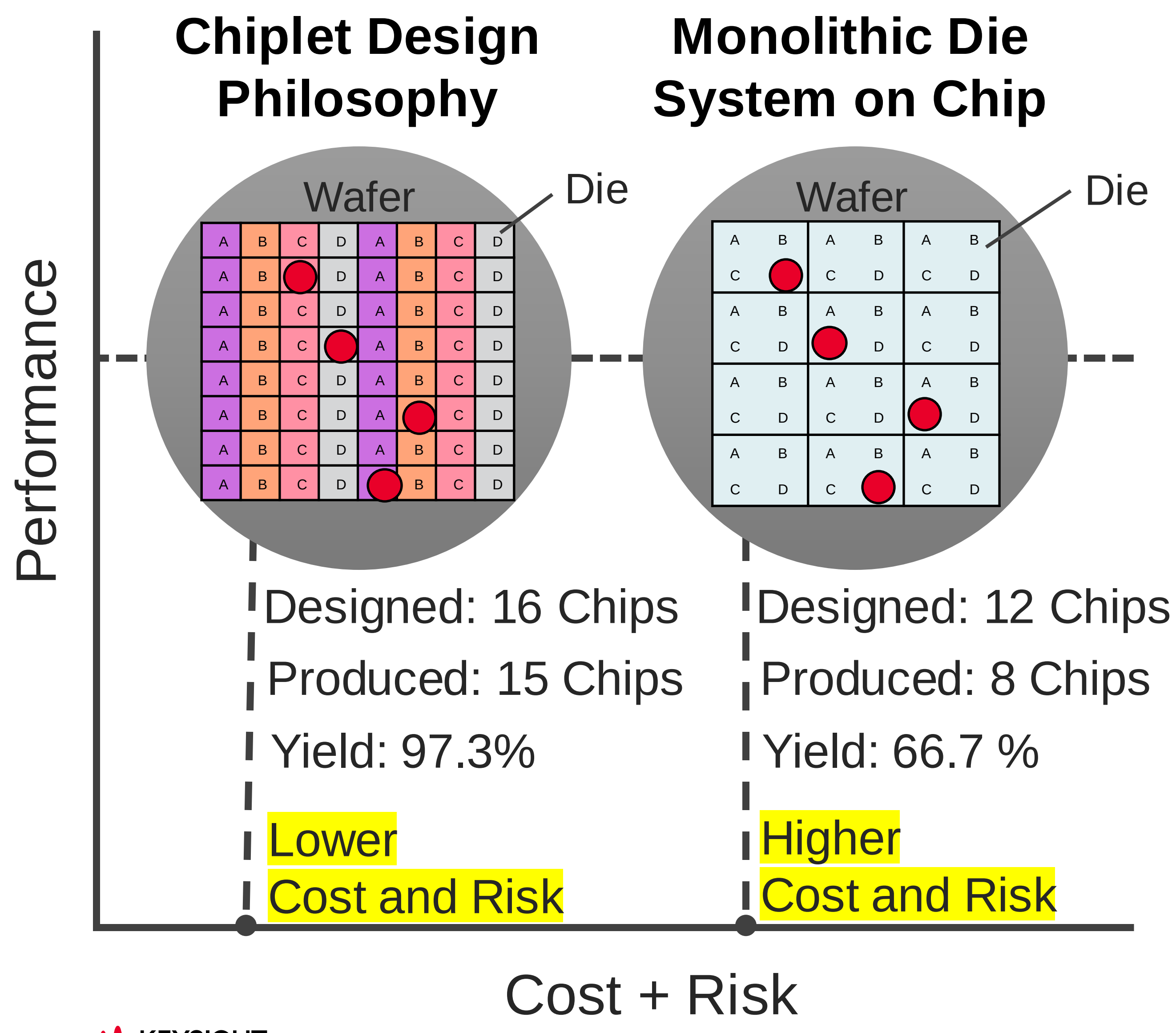


Chiplet Design Philosophy

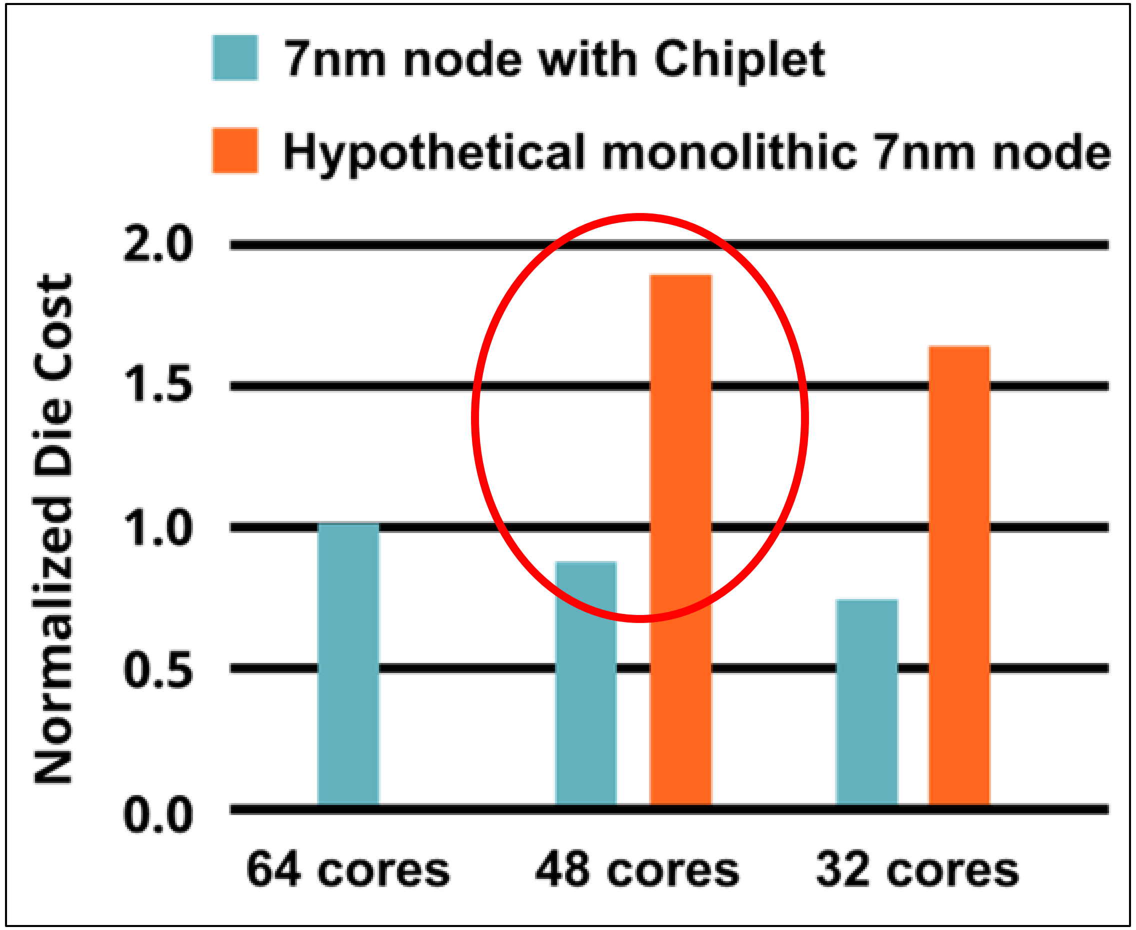
- Maximizes wafer usage
- Has a higher yield
- Has a lower cost
- Easy to scale!

The chiplet approach reduces cost, risk and improves the scaling ability.

Chiplets Improve the Cost vs. Performance of Chip Production

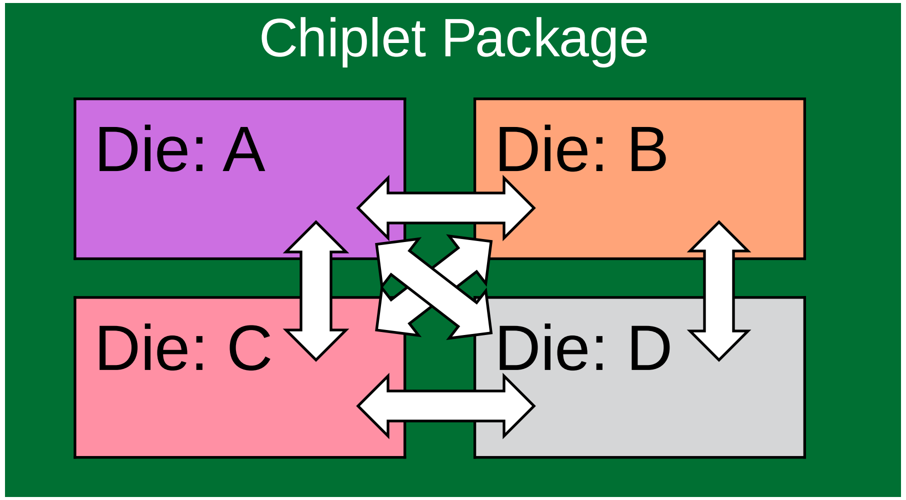


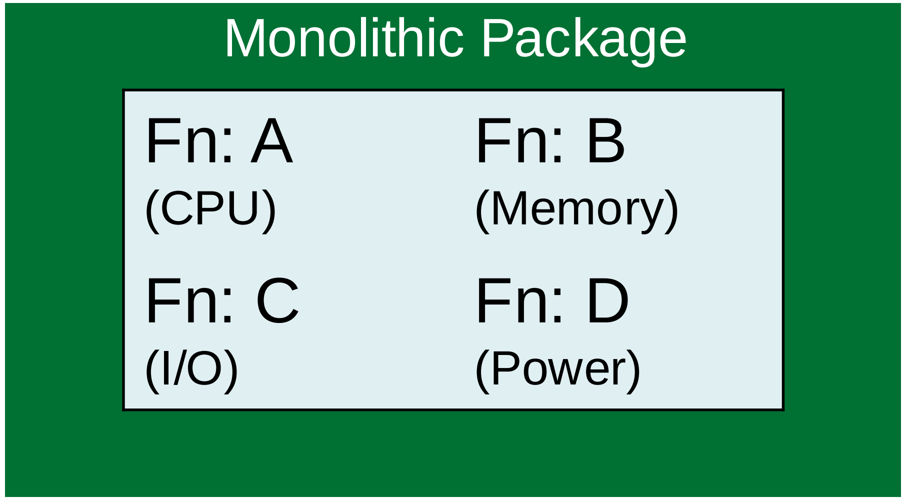
The chiplet approach reduces cost and improves the scaling ability.



Ref [1]

The Catch: Die-to-Die Communication is Important for Chiplets





UCIe™ Universal Chiplet Interconnect Express

BoW

OPEN Compute Project

The standards for the die-to-die interface between chiplets

- **UCIe (Universal Chiplet Interconnect express)**
- **BoW (Bunch of Wires)**

Comparing UCIe and BoW Standards

UCIe vs. BoW: One-word Review Comparison

Interoperability

Cost-efficiency

UCIe vs. BoW: Top Level Features Comparison

Category	UCIe Universal Chiplet Interconnect Express	BoW
Signal mapping priority	Bump map	Wire order
Data transmission	Serial – adjacent	Parallel
Basic design unit	Module	Slice
Directionality	Unidirectional	Can be bi-directional

UCIe vs. BoW: Key Attributes Comparisons for Applications

Ease of implementation

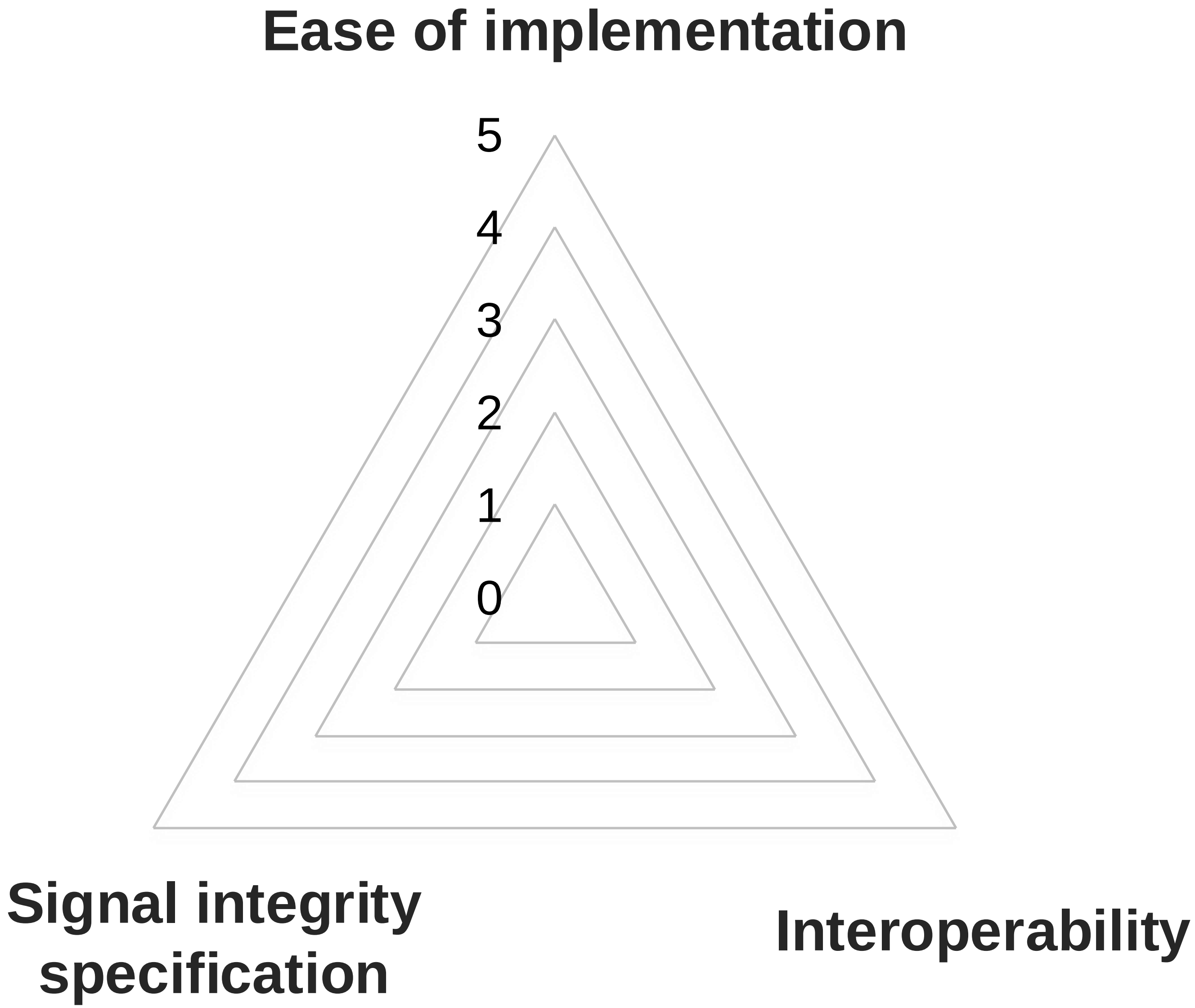
A higher score means it is easier to implement.

Signal integrity specification

A higher score means there are more ways to verify signal integrity.

Interoperability

A higher score means the current design is more likely to work with future ones.



KEYSIGHT

UCIe vs. BoW: Key Attributes Comparisons for Applications

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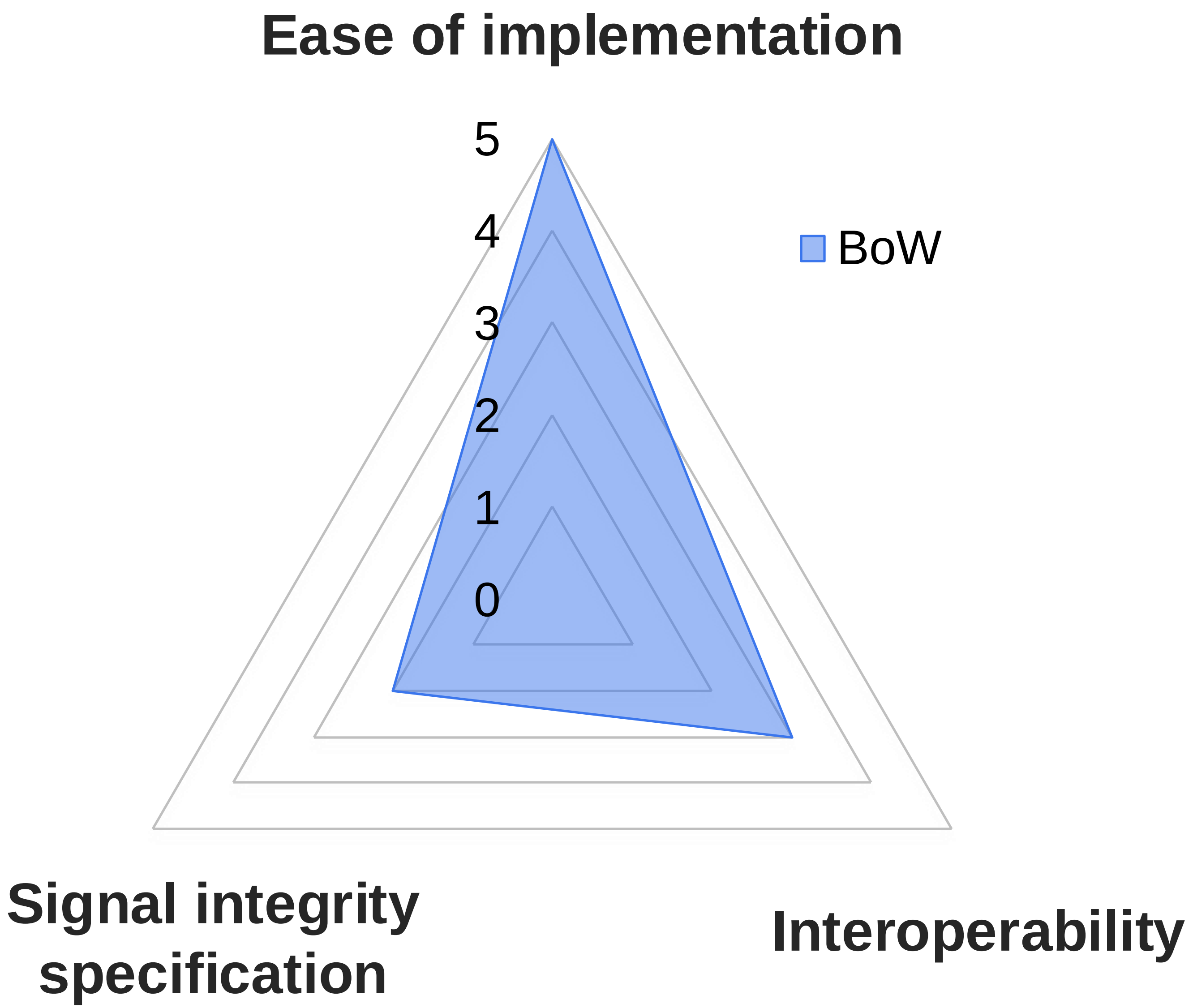

UCIe vs. BoW: Key Attributes Comparisons for Applications

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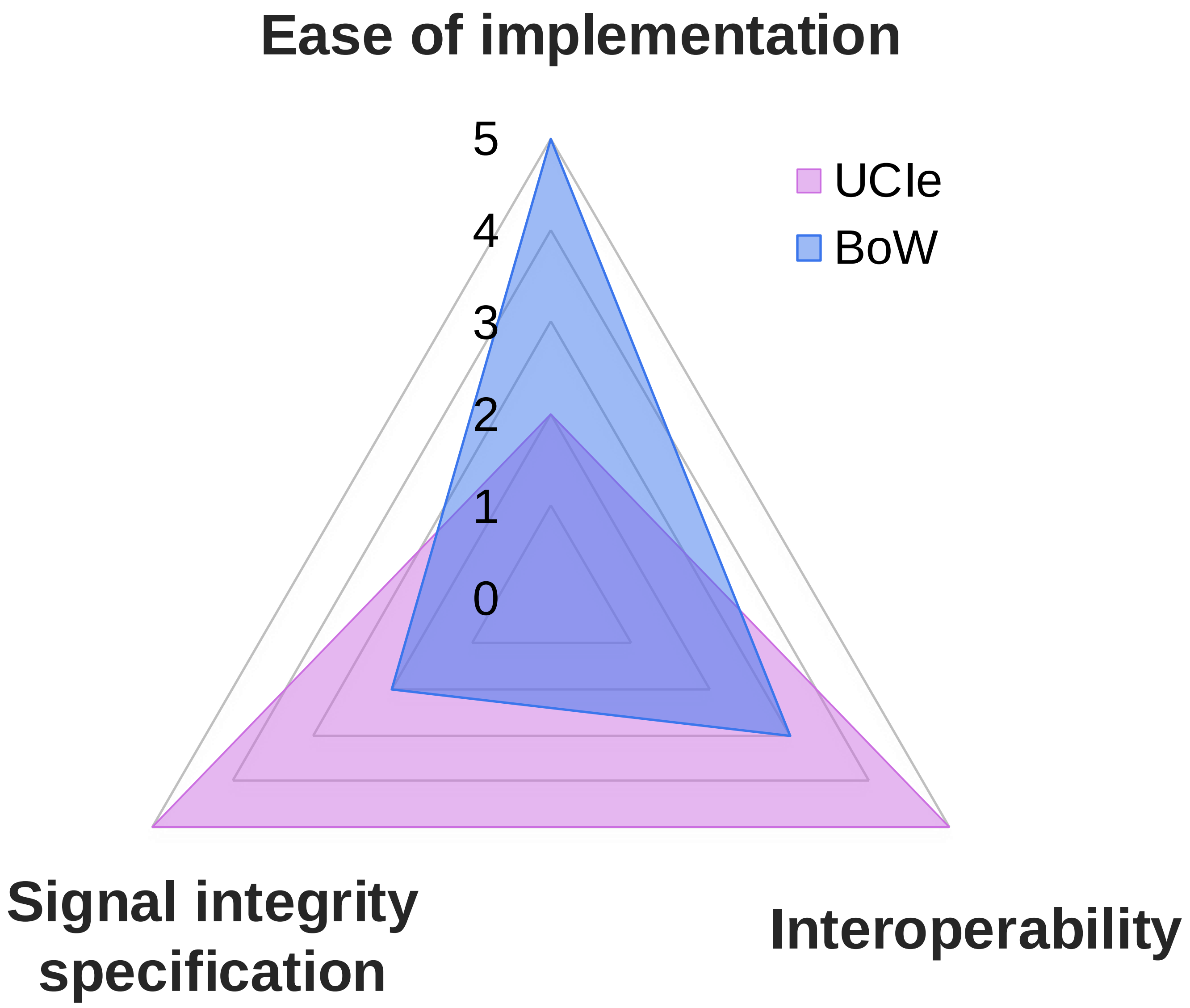
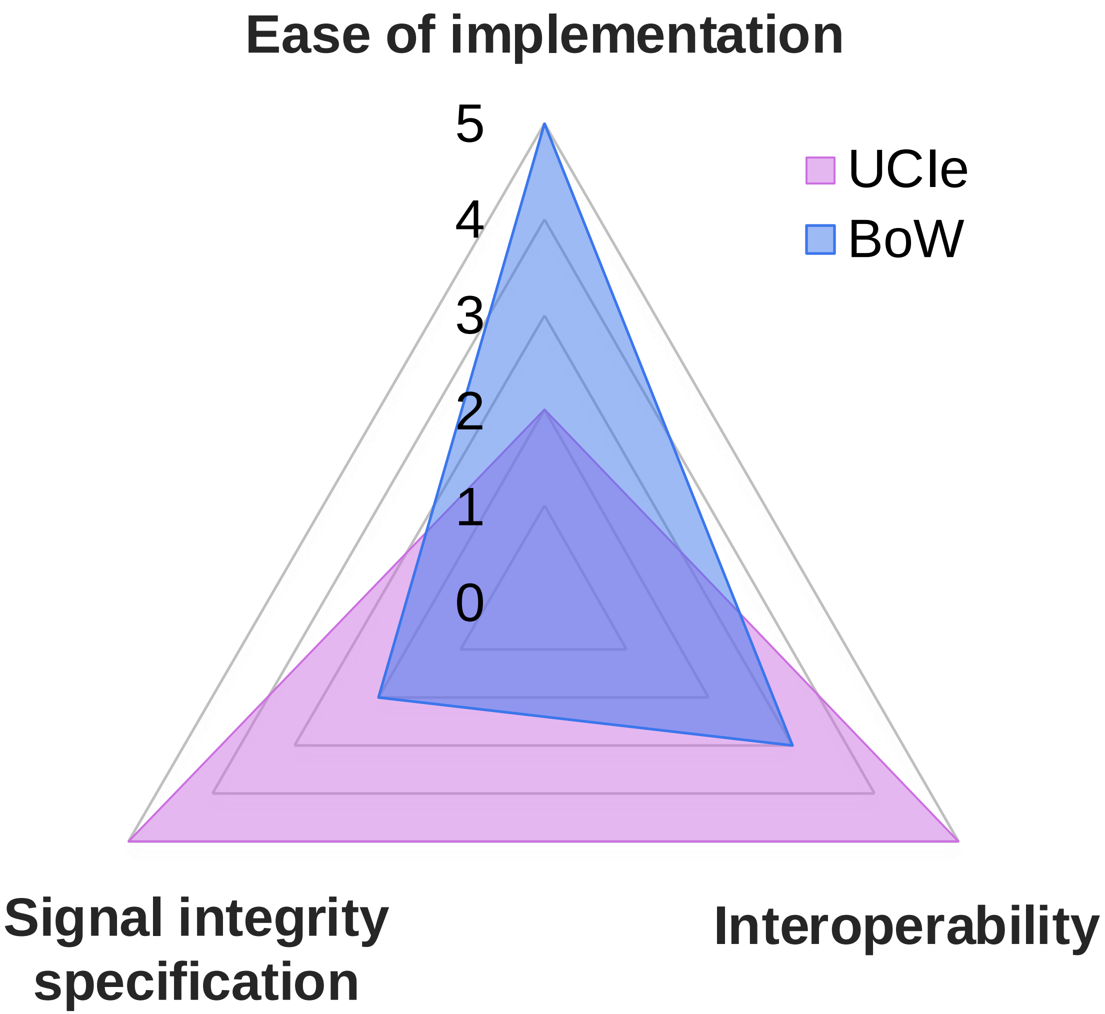


UCIe vs. BoW: Application Implementation Selection



UCIe Universal Chiplet Interconnect Express

Create ultimate Plug-and-Play applications

BoW OPEN Compute Project

Create low-cost applications with implementation flexibility

What Would the Standard Say (WWSS) to justify the radar chart

What Would the Standard Say?

Comparing UCIe and BoW Standard with an Example Channel

UCIe vs. BoW: Technical Comparison with a Case Study

Example channel

UCIe data rates [2]:

4 GT/s 12 GT/s 24 GT/s

8 GT/s 16 GT/s 32 GT/s

BoW wire bit rates [3]:

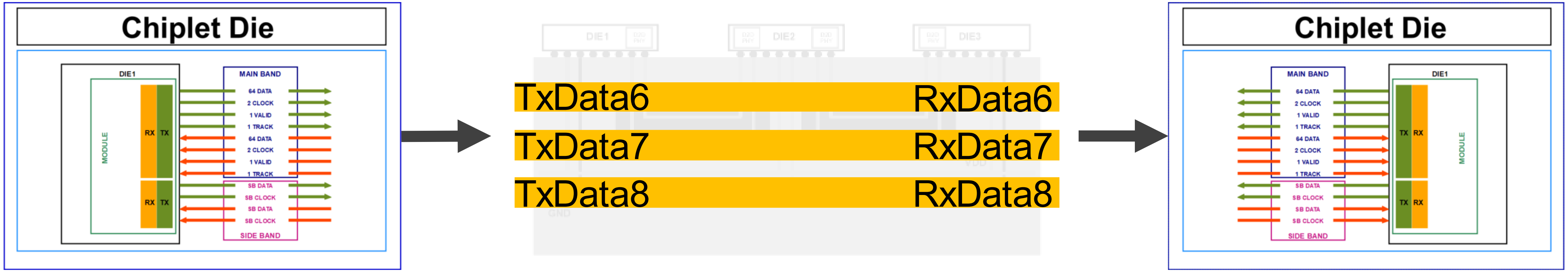
2 Gb/s 8 Gb/s 24 Gb/s

4 Gb/s 16 Gb/s 32 Gb/s

BoW Mode:
BoW-384

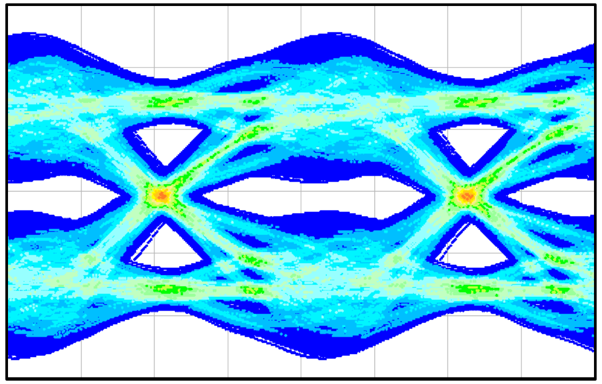
BoW has 2 Gb/s but not UCIe

What Would the Standard Say: a Comparative Case Study



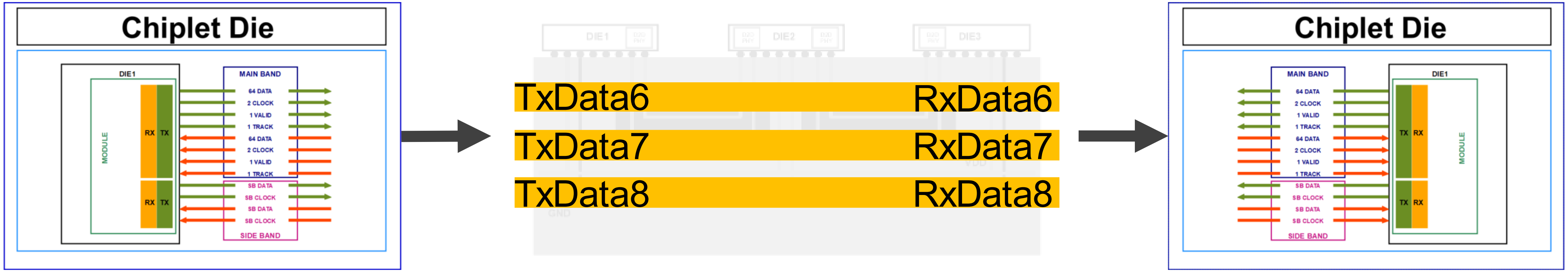
What Would the Standards Say:

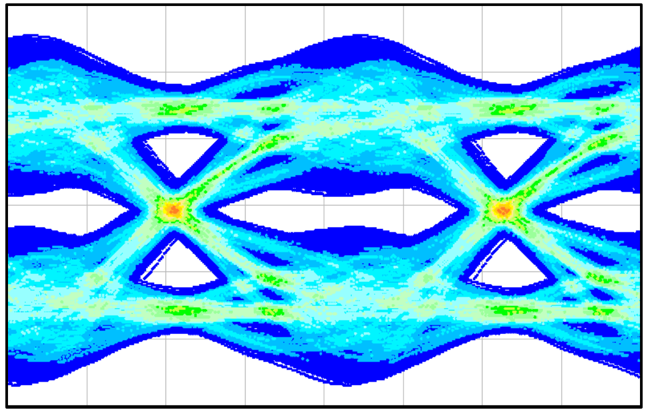
- Voltage and timing margins
- Loss, and crosstalk level



A Comparative Case Study to Gain Signal Integrity Insights

Standard package





The impact on the eye diagram from

- Reflection
- Crosstalk
- Frequency-dependent loss

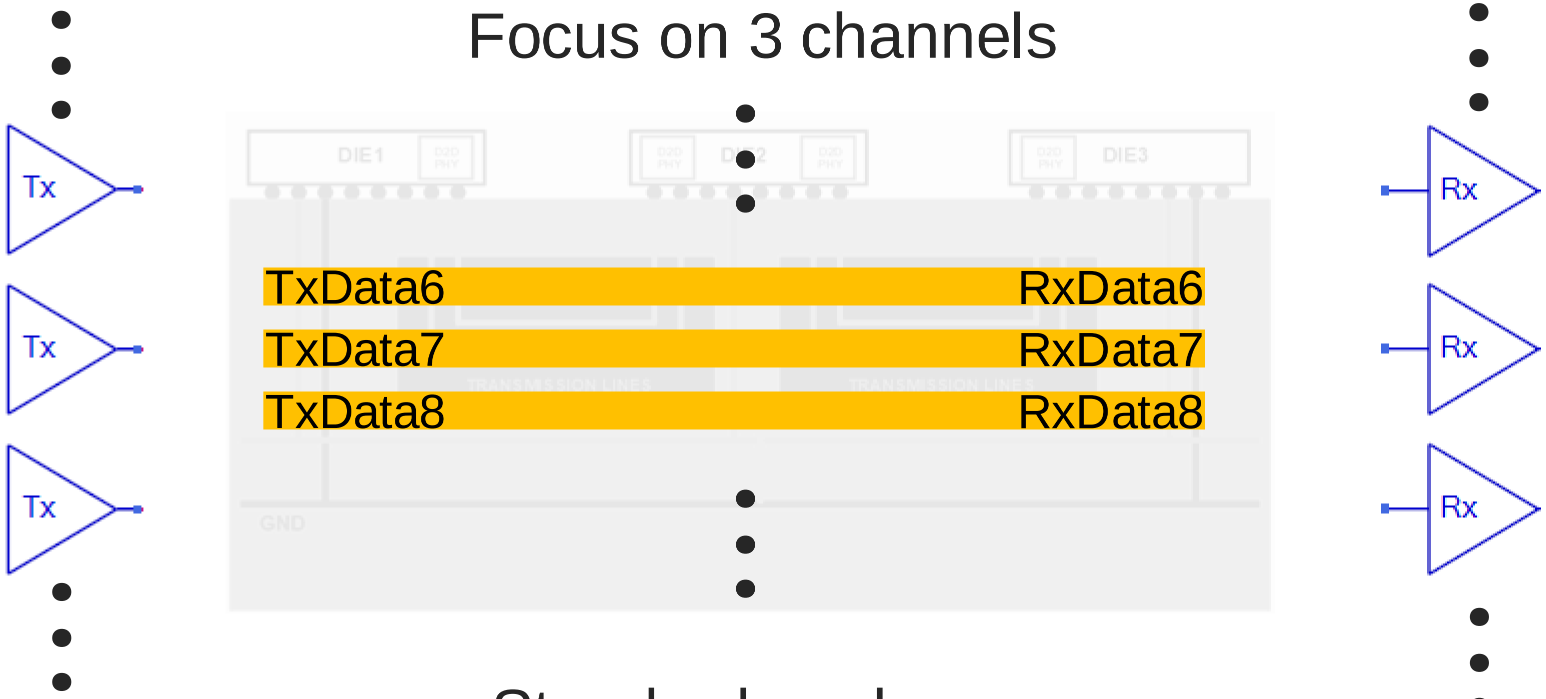
KEYSIGHT

Focus on 3 Channels, 24 GT/s and Standard Package

Focus on 3 channels

3 Transmitters

24 GT/s



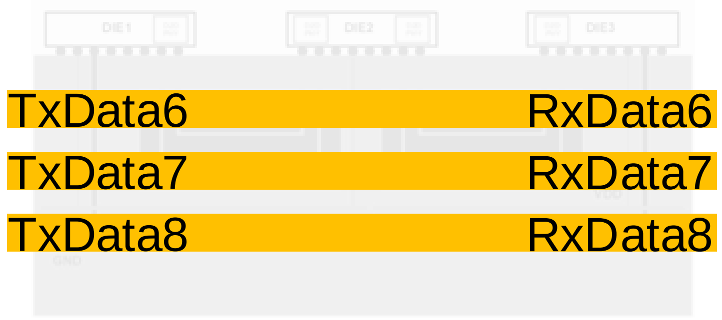
3 Receivers

Standard package

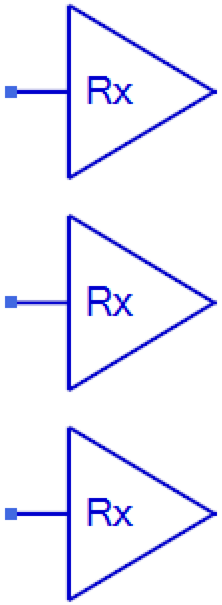
This study focuses on what would the standard say about the three channels in the middle of 16 data lines running at 24 GT/s.

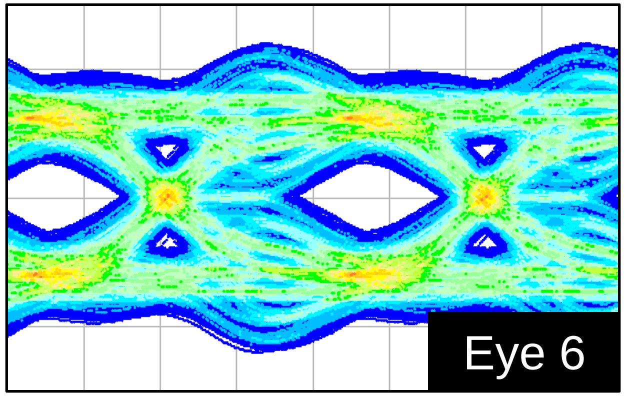
Qualitative Assessment of the Eye Diagram Is Not Positive

3 Transmitters
Standard package
24 GT/s

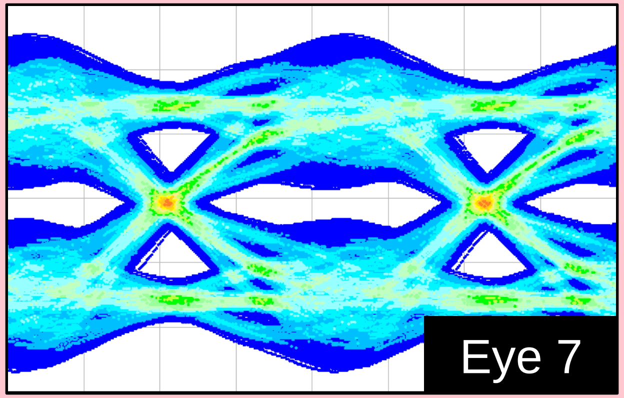


3 Receivers
No EQ
Terminated



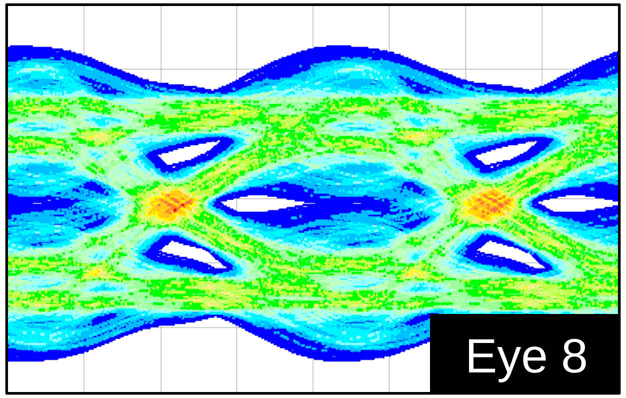


Not good



Bad

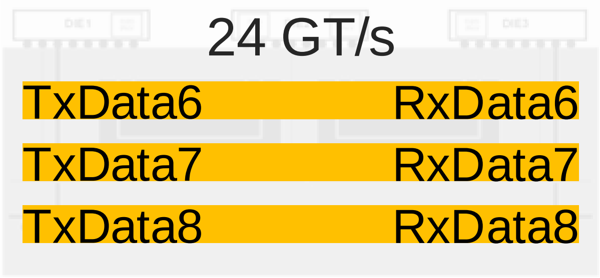
Let’s ask the standards



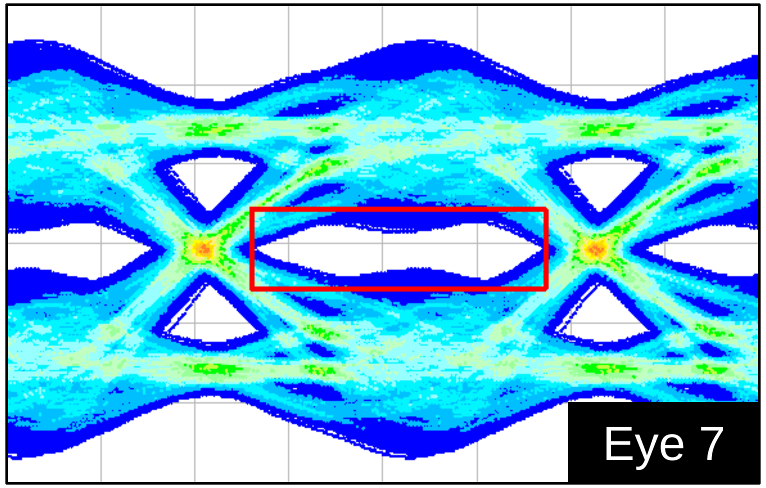
Very bad

WWSS-Eye: Standards with Different Descriptions of the Eye

UCIe™ Universal Chiplet Interconnect Express



Standard package

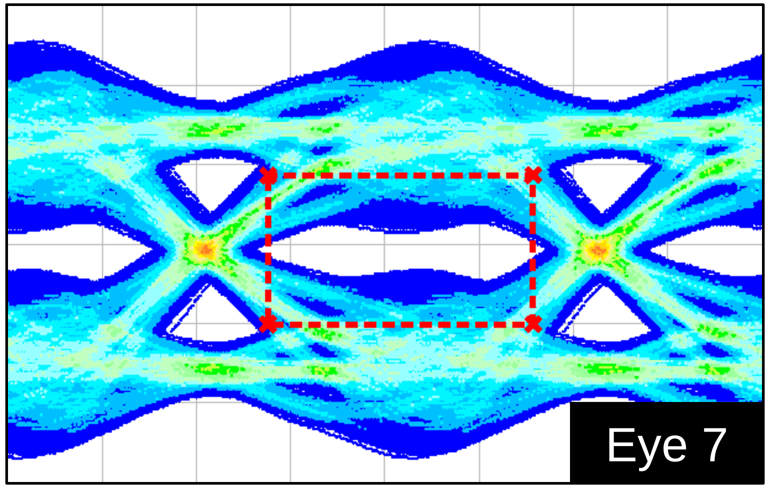


Data Rate (GT/s)	Eye Height (mV)	Eye Width (UI)
4, 8, 12, 16[1, 3]	40	0.75
24, 32[1,2,3]	40	0.65

[2] Table 5-10

1. Rectangular mask.
2. With equalization enabled.
3. Based on minimum Tx swing specification.

BoW OPEN Compute Project



BoW Mode	$V_{err, tot, RX}$ (mV)	$t_{err, tot, RX}$ (T_{bit})
BoW-384	75	32.5%

[3] Table 15

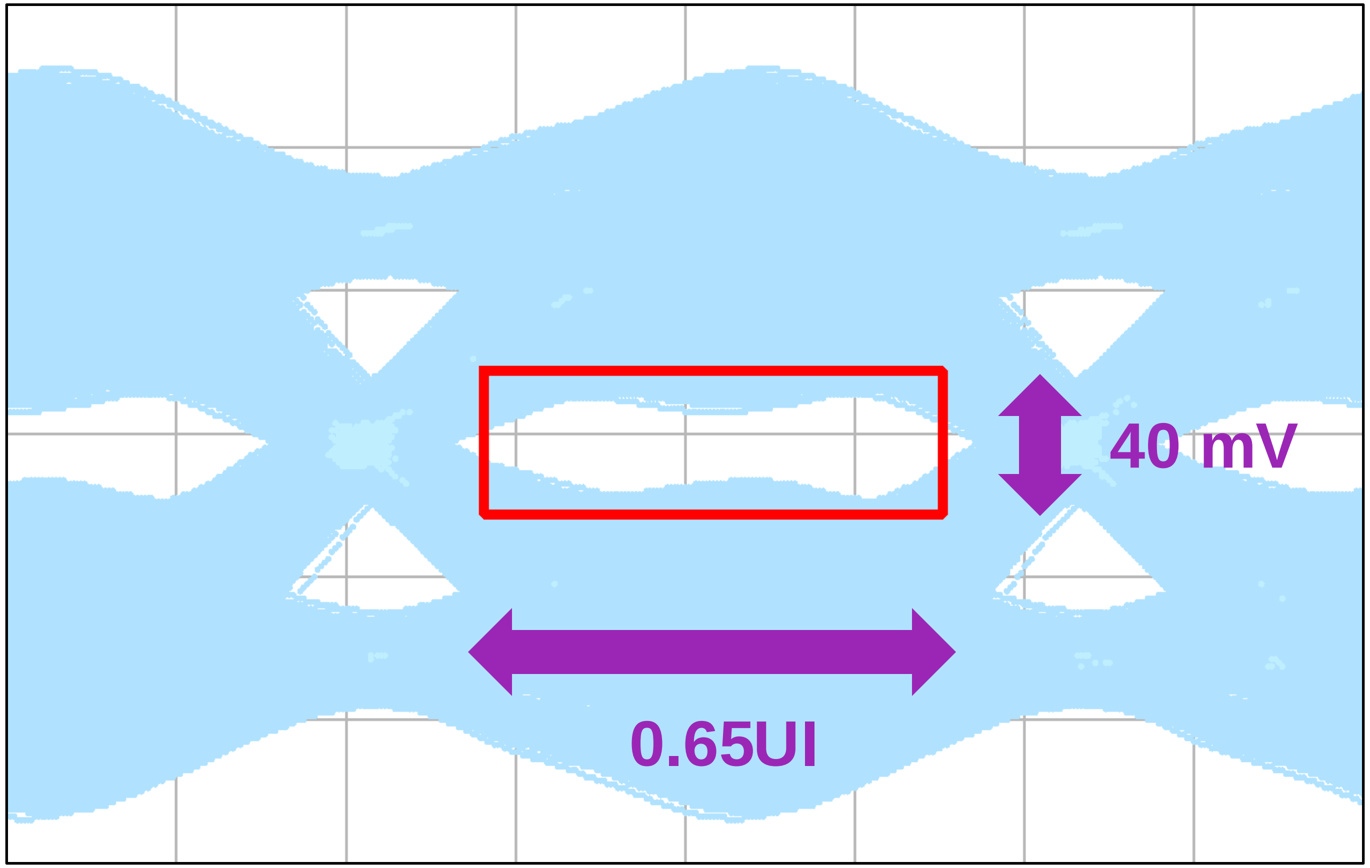
$V_{err, tot, RX}$:
Maximum total required Rx voltage margin

$t_{err, tot, RX}$:
Maximum total Rx timing error

It was easier to find the eye height and width from UCIe.

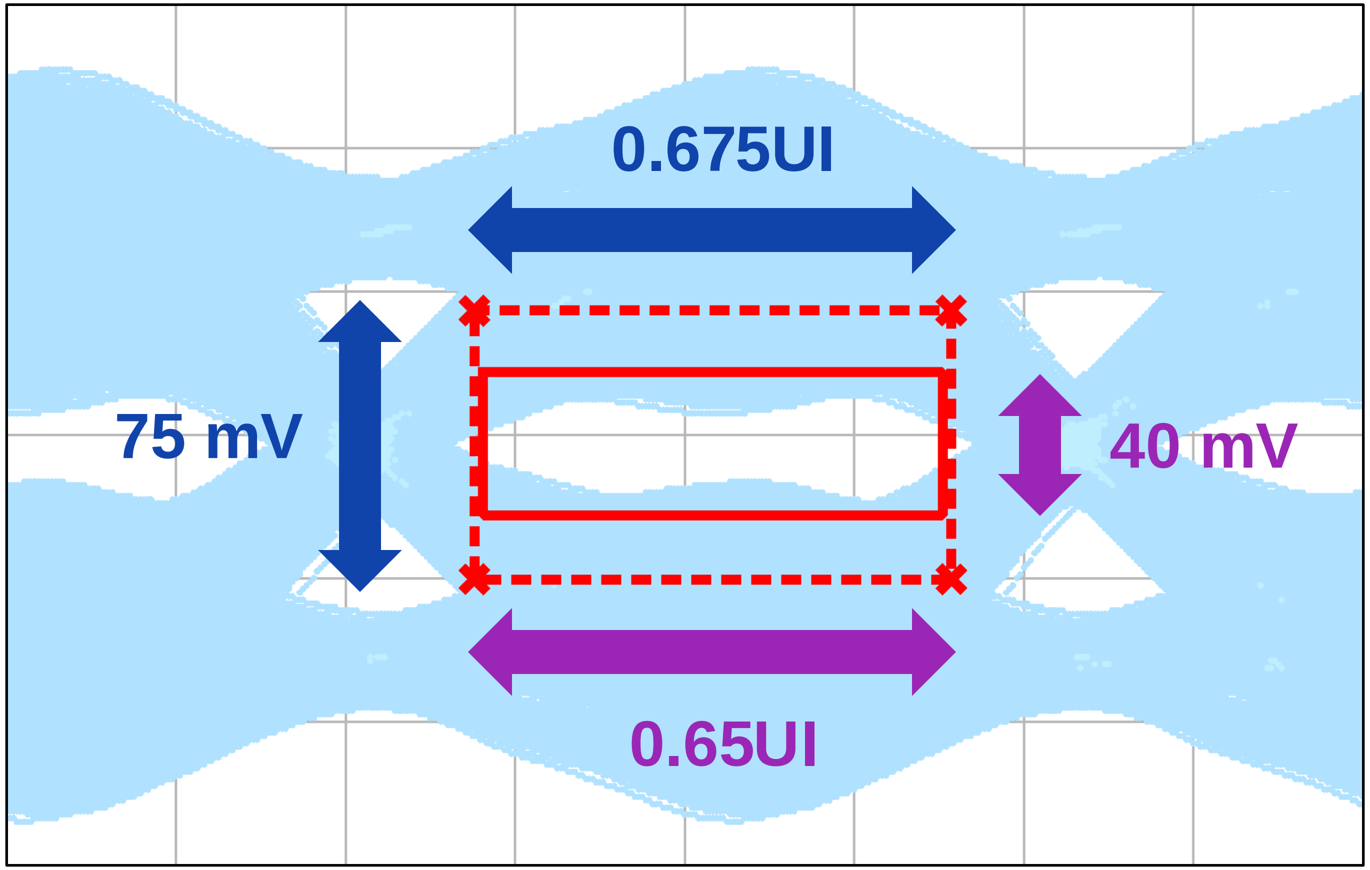
KEYSIGHT

WWSS-Eye: UCIe and Bow Have Different Margin Requirements



Standard package
24 GT/s

WWSS-Eye: UCIe and Bow Have Different Margin Requirements



UCIe™
Universal Chiplet Interconnect Express

BoW
OPEN Compute Project

Standard package
24 GT/s

BoW requires more voltage margins and slightly more timing margin.

WWSS-Loss: Evaluate Your Channel's Loss with the Standards

[2] Section 5.7.1

24 GT/s

TxData6 RxData6
TxData7 RxData7
TxData8 RxData8

Standard package

Data Rate (GT/s)	4, 8	12, 16	24, 32
VTF Loss (dB)	L(0) > -4.5 $L(f_N)$ > -7.5	L(0) > -4.5 $L(f_N)$ > -6.5	L(0) > -4.5 $L(f_N)$ > -7.5

- f_N= Nyquist frequency
- Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF)
- Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF)
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)

---

[3] Section 12

24 GT/s

TxData6 RxData6
TxData7 RxData7
TxData8 RxData8

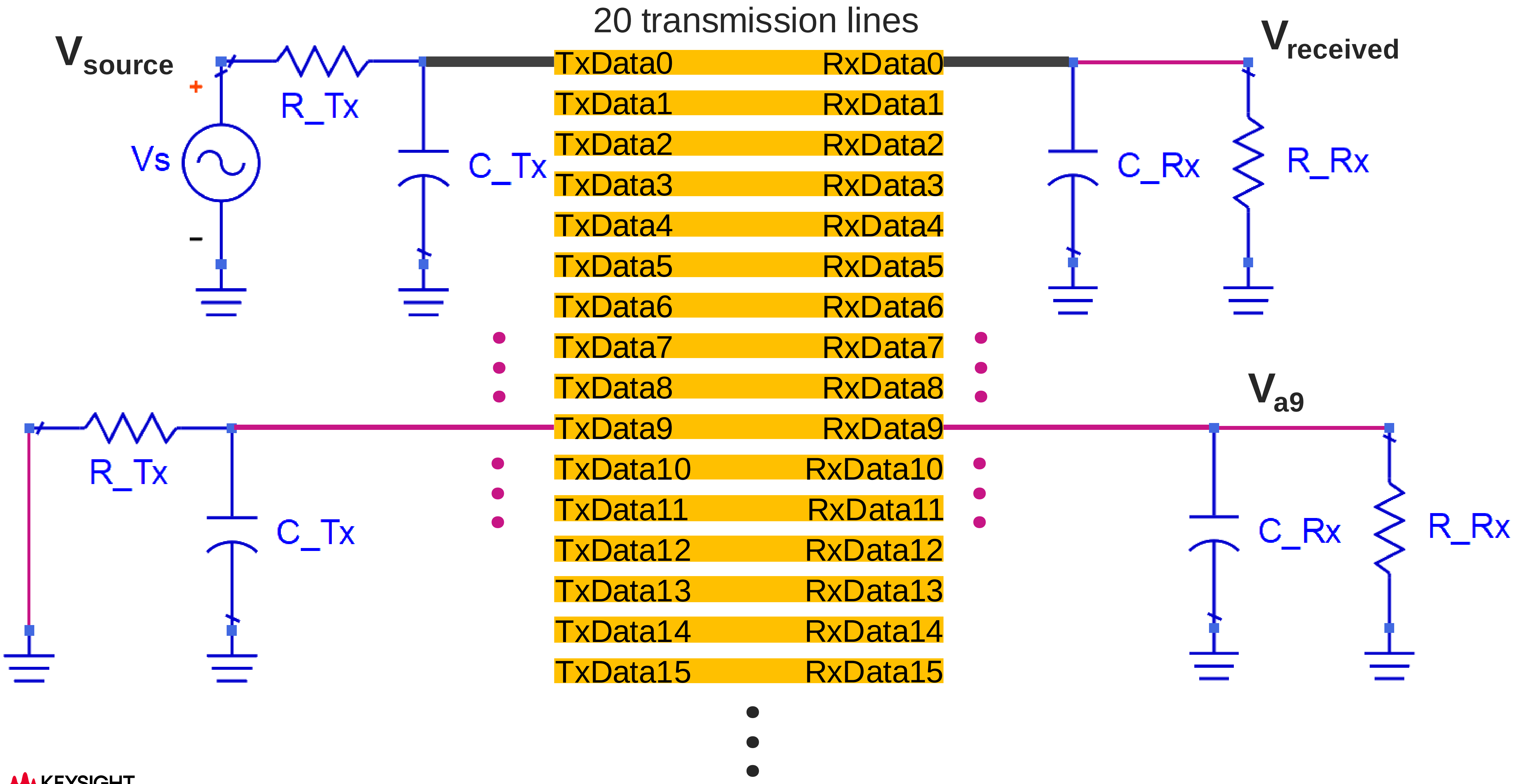
Standard package

BoW does not place any direct requirements on characteristics such as channel loss or crosstalk.

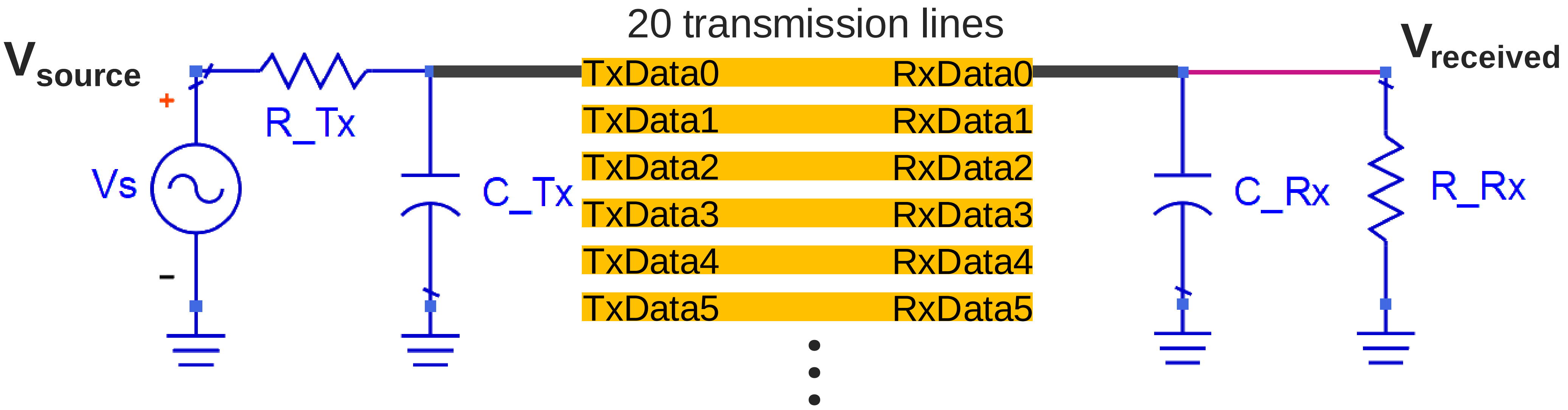
12.3. Example BoW Channel for Doubly-Terminated Links

We expect both loss evaluations to fail because the eye mask was violated.

Voltage Transfer Function in the UCIe Standard



VTF Loss Definition in the UCIe Standard



Given $C_{Tx}, R_{Tx}, C_{Rx}, R_{Rx}$ for different data rates

$$L(f) = 20\ log\left(\left|\frac{V_{received}(f)}{V_{source}(f)}\right|\right)$$

$$L(0) = 20\ log\left(\frac{R_{Rx}}{R_{Tx} + R_{channel} + R_{Rx}}\right)$$

👆 For terminated channel. L(0) = 0 for unterminated channels

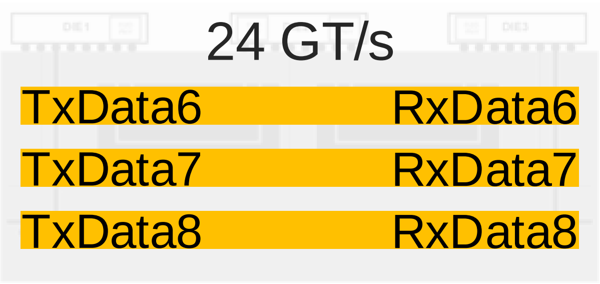
Standard package (f_N= Nyquist frequency)

Data Rate (GT/s)	4, 8	12, 16	24, 32
VTF Loss (dB)	L(0) > -4.5 L(f_N) > -7.5	L(0) > -4.5 L(f_N) > -6.5	L(0) > -4.5 L(f_N) > -7.5

- Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF)
- Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF)
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)

UCIe's VTF Loss Limit Line and Passing Criteria

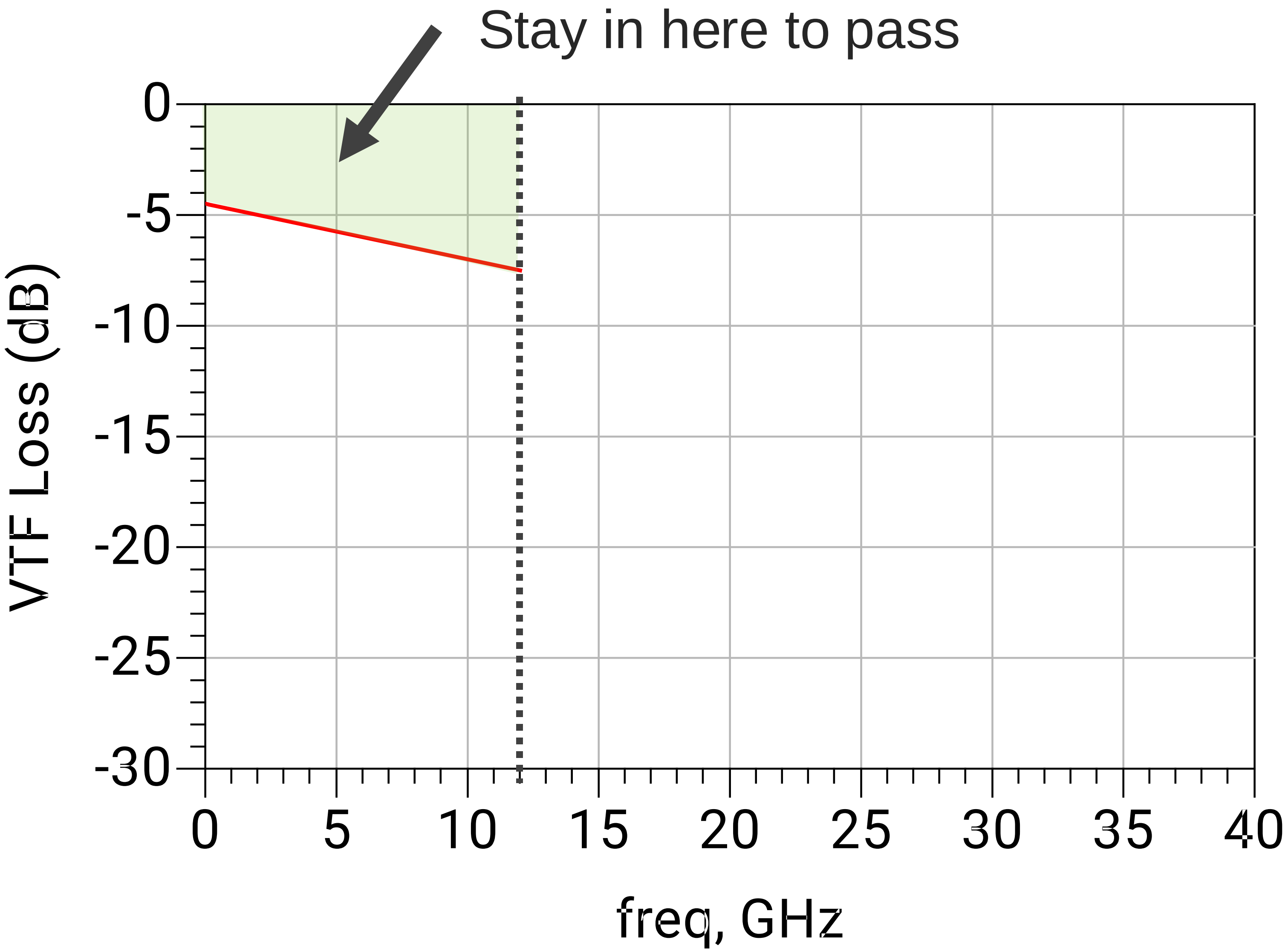
Universal Chiplet Interconnect Express



Standard package

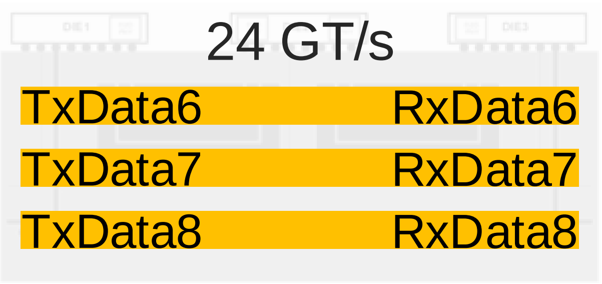
Data Rate (GT/s)	24, 32
VTF Loss (dB)	L(0) > -4.5 L(f_N) > -7.5

- f_N= Nyquist frequency
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)
- [2] Section 5.7.1



UCIe's VTF Loss Evaluation Indicates a Failing Channel

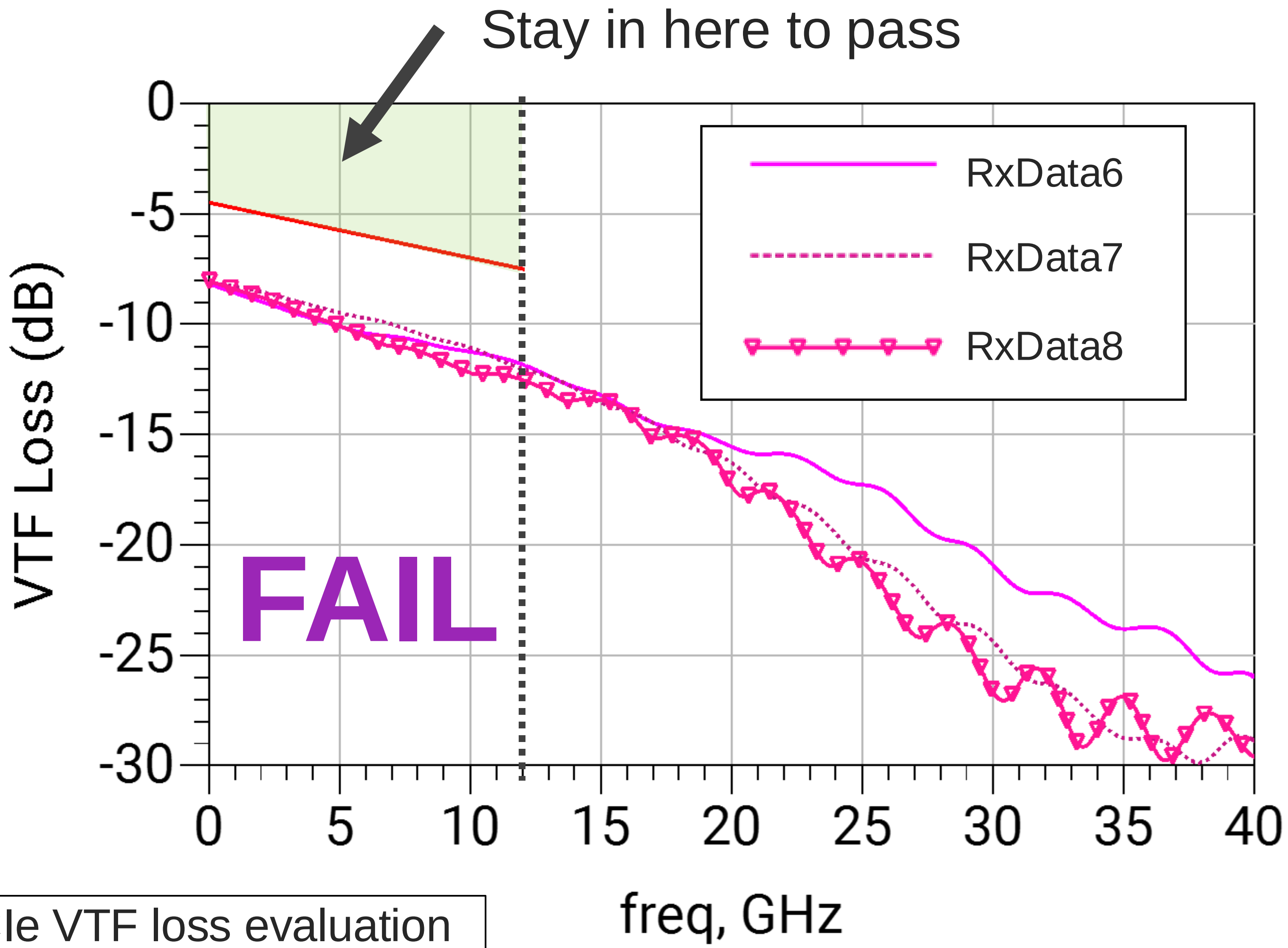
UCIe™
Universal Chiplet
Interconnect Express



Standard package

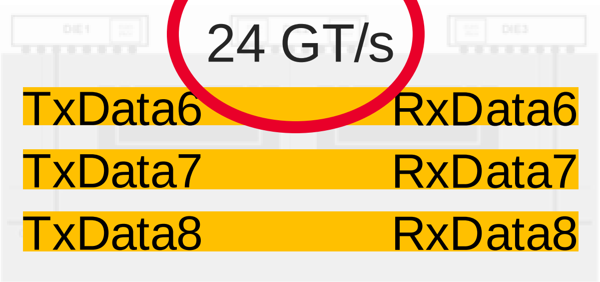
Data Rate (GT/s)	24, 32
VTF Loss (dB)	$L(0) > -4.5$ $L(f_N) > -7.5$

- f_N= Nyquist frequency
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)
- [2] Section 5.7.1



UCIe VTF loss evaluation fails as expected.

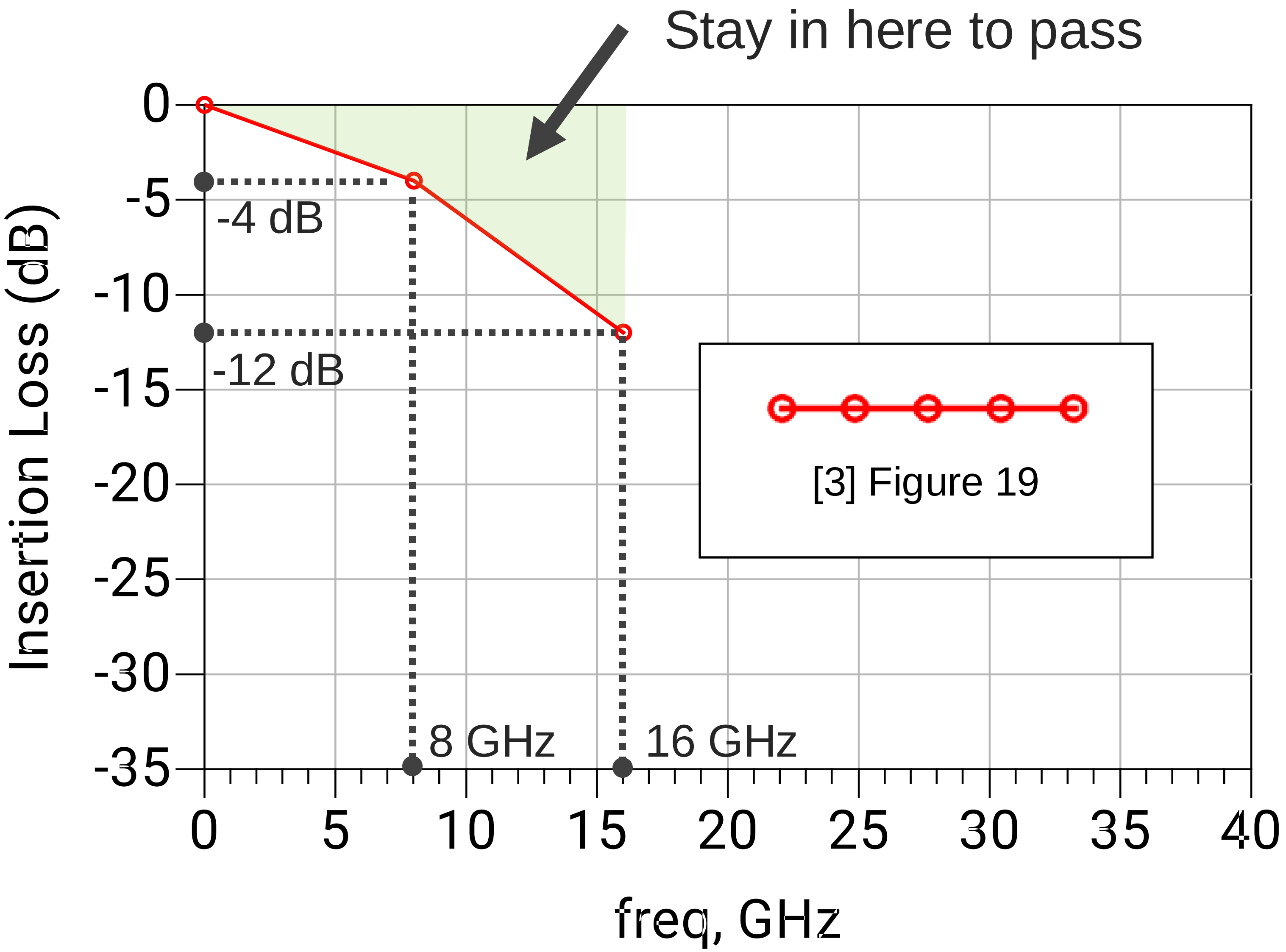
Examination of BoW's Example Channel from 12.3



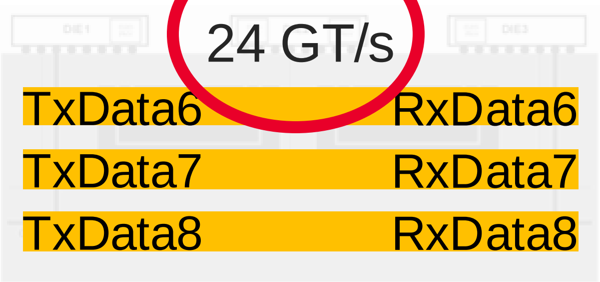
Standard package

BoW Mode	BoW-256 (16 Gbps)
Insertion Loss (dB)	$IL(f_N) > -4$ $IL(2*f_N) > -12$

[3] Figure 19

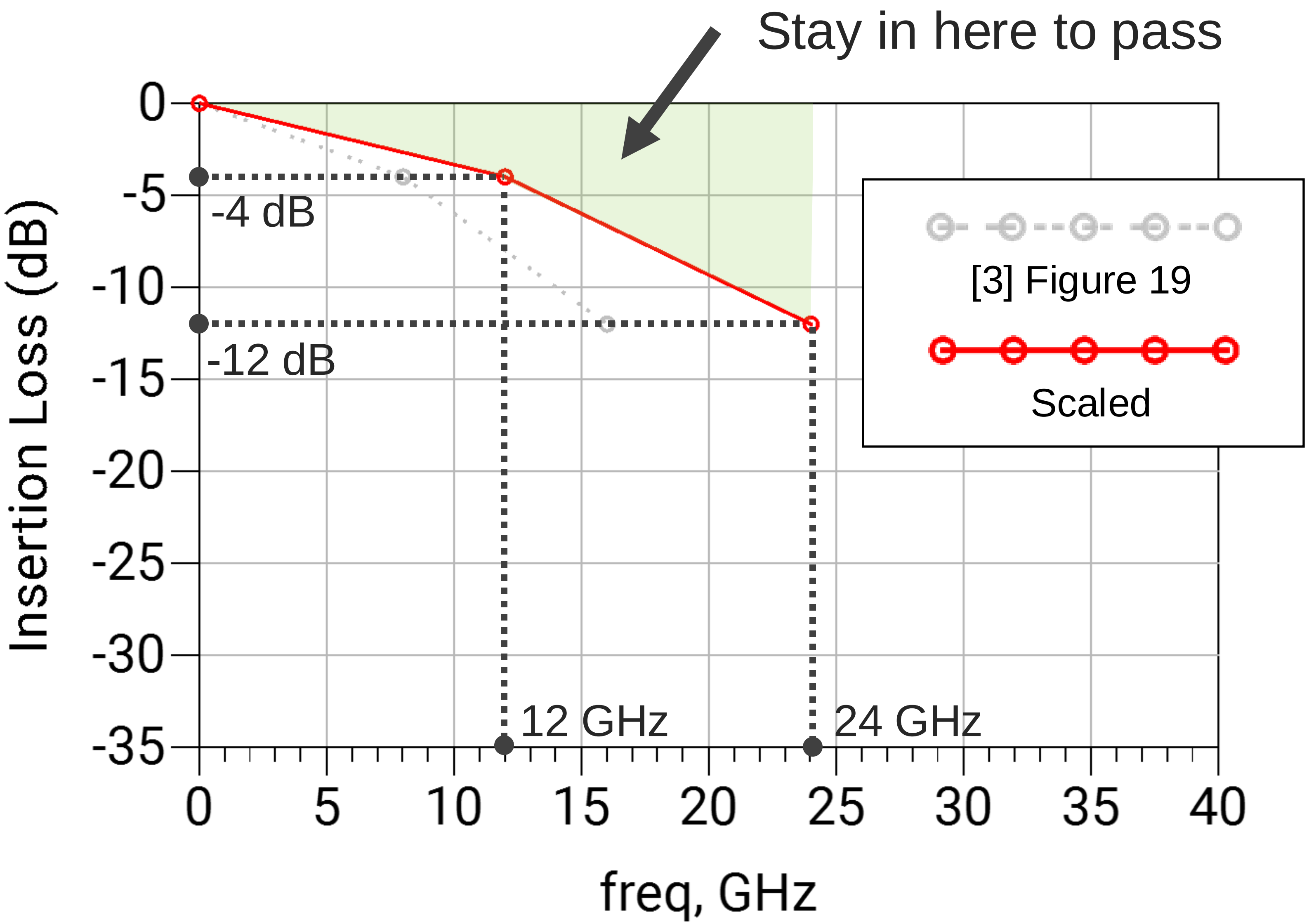


Scale BoW's Example to Create the Right Limit Line



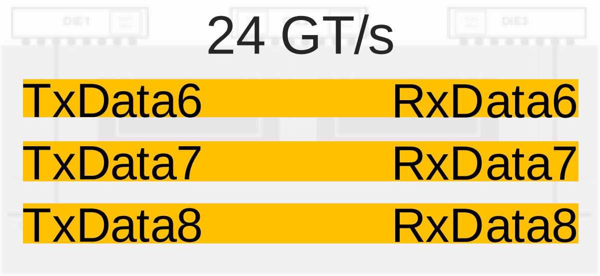
Standard package

BoW Mode	BoW-384 (24 Gbps)
Insertion Loss (dB)	$IL(f_N) > -4$ $IL(2*f_N) > -12$



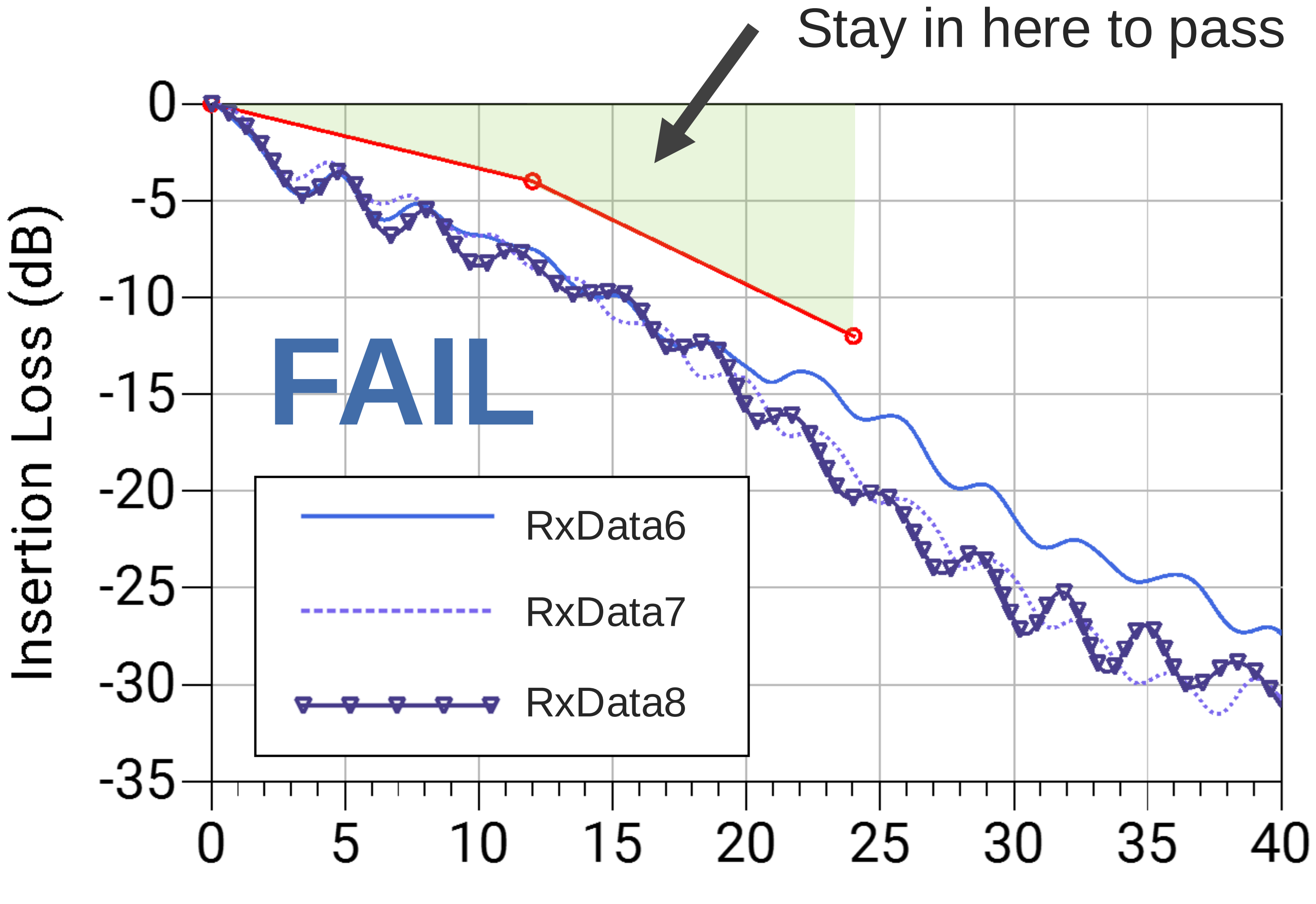
BoW's Evaluation Indicates a Failing Channel

BoW
OPEN Compute Project



Standard package

BoW Mode	BoW-384 (24 Gbps)
Insertion Loss (dB)	$IL(f_N) > -4$ $IL(2*f_N) > -12$



BoW loss evaluation fails as expected.

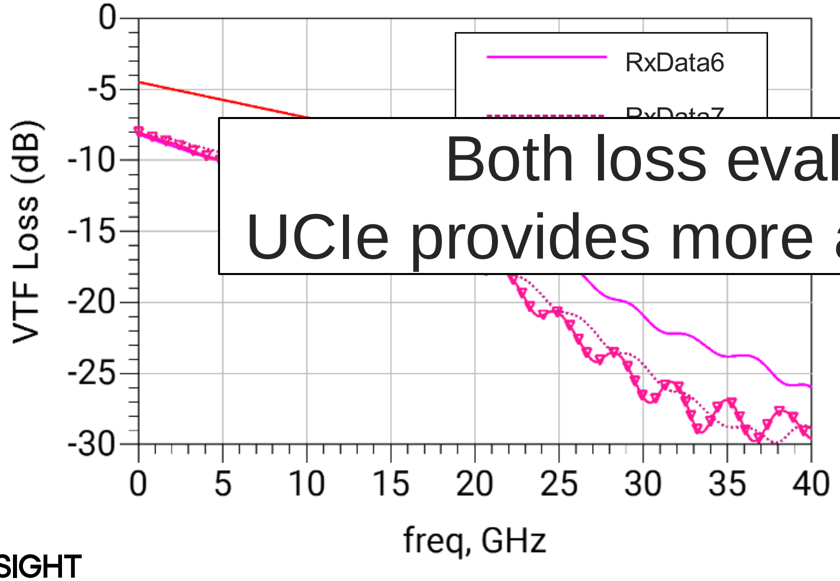
UCIe Provides More Accessible Loss Metrics Than BoW

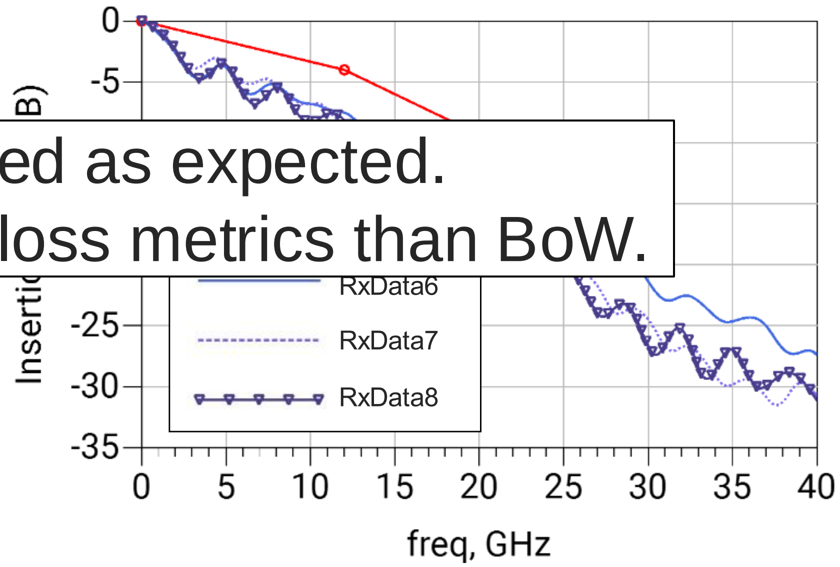
Data Rate (GT/s)	24, 32
VTF Loss (dB)	L(0) > -4.5 L(f_N) > -7.5

- f_N= Nyquist frequency
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)
- [2] Section 5.7.1

BoW Mode	BoW-384 (24 Gbps)
Insertion Loss (dB)	IL(f_N) > -4 IL(2*f_N) > -12

Open-source software evaluating signal integrity […] will be provided at a future date [3].



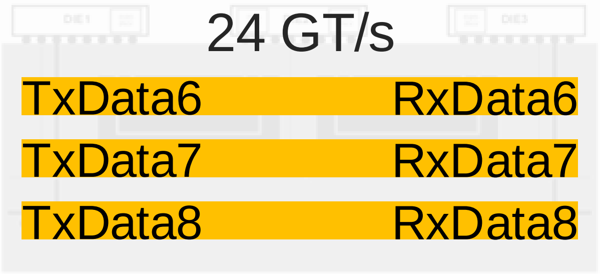


Both loss evaluations failed as expected.
UCIe provides more accessible loss metrics than BoW.

WWSS-Crosstalk: Evaluate Your Channel's Crosstalk

Universal Chiplet Interconnect Express

24 GT/s



Standard package

[2] Section 5.7.1

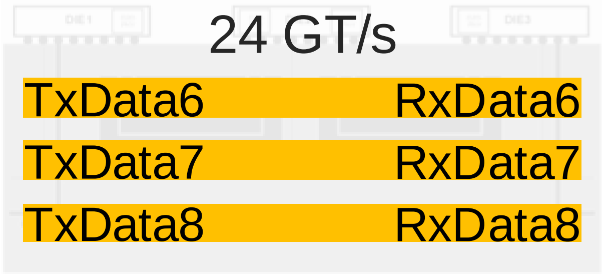
Data Rate (GT/s)	12, 16	24, 32
VTF Xtalk (dB)	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

- f_N= Nyquist frequency
- Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF)
- Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF)
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)

BoW

OPEN Compute Project

24 GT/s



Standard package

[3] Section 12

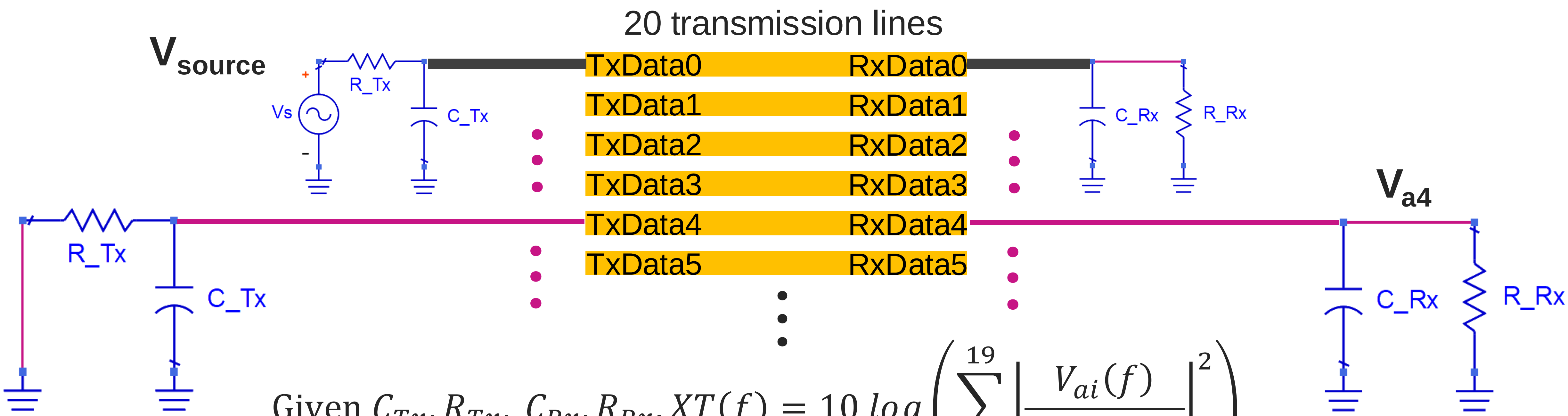
BoW does not place any direct requirements on characteristics such as channel loss or crosstalk.

12.3.2 Crosstalk

We expect both crosstalk evaluations to fail because the eye mask was violated.

KEYSIGHT

VTF Crosstalk Definition in the UCIe Standard



$$\text{Given } C_{Tx}, R_{Tx}, C_{Rx}, R_{Rx}, XT(f) = 10\ log\left(\sum_{i=1}^{19}\left|\frac{V_{ai}(f)}{V_{source}(f)}\right|^2\right)$$

Standard package (f_N= Nyquist frequency)

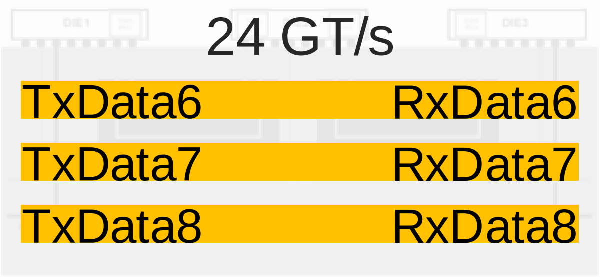
Data Rate (GT/s)	4, 8	12, 16	24, 32
VTF Xtalk (dB)	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 3 * L(f_N) - 11.5$ and $XT(f_N) < -25$	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

- Voltage Transfer Function for 4 GT/s and 8 GT/s (Tx: 30 ohm / 0.3pF; Rx: 50 ohm / 0.3pF)
- Voltage Transfer Function for 12 GT/s and 16 GT/s (Tx: 30 ohm / 0.2pF; Rx: 50 ohm / 0.2pF)
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)

KEYSIGHT

UCIe's VTF Crosstalk Limit Line and Passing Criteria

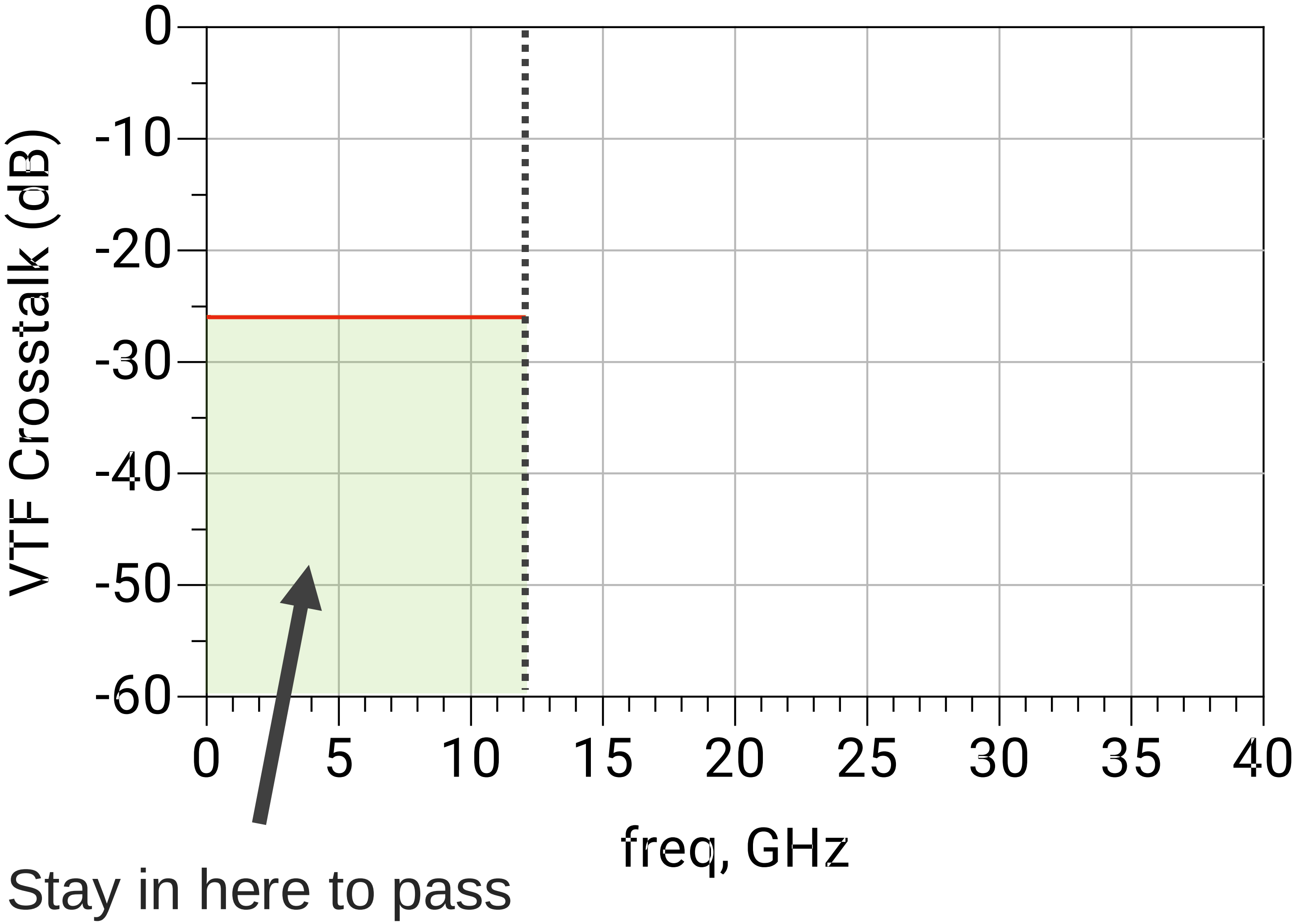
UCIe
Universal Chiplet
Interconnect Express



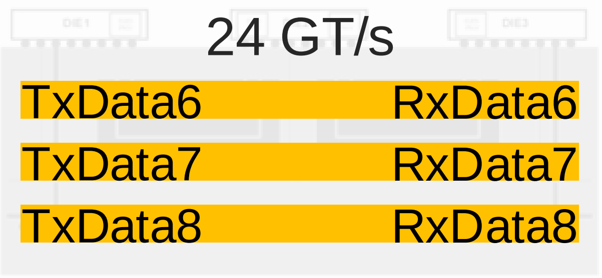
Standard package

Data Rate (GT/s)	24, 32
VTF Xtalk (dB)	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

- f_N= Nyquist frequency
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)
- [2] Section 5.7.1



UCIe's VTF Crosstalk Evaluation Indicates a Failing Channel

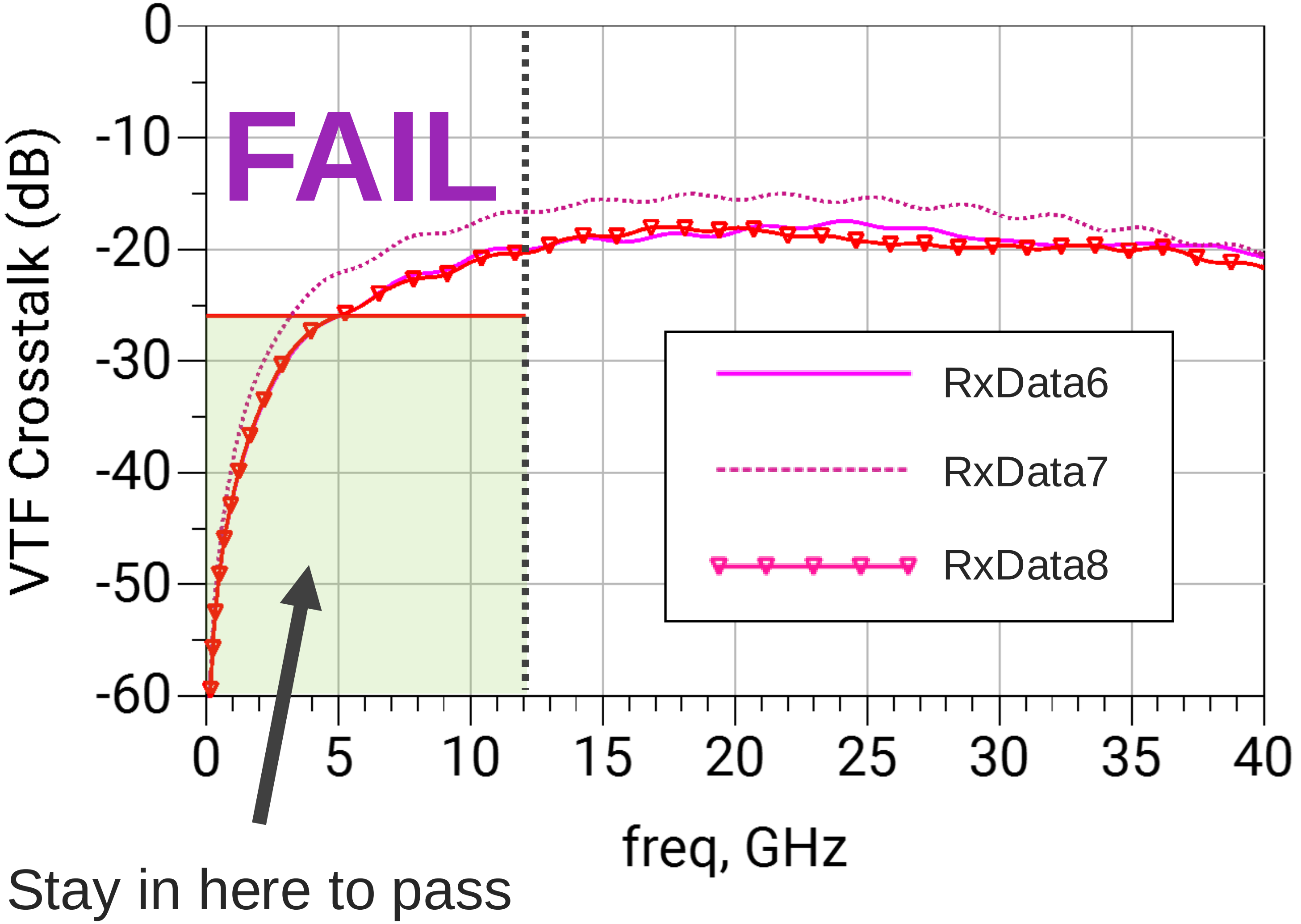


Standard package

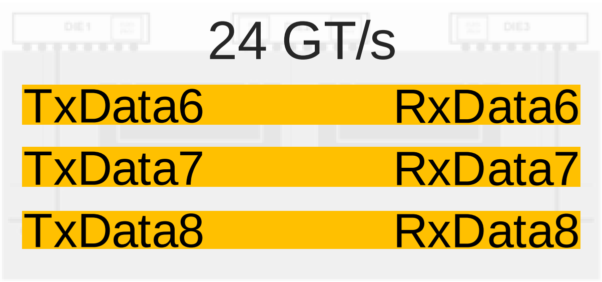
Data Rate (GT/s)	24, 32
VTF Xtalk (dB)	$XT(f_N) < 2.5 * L(f_N) - 10$ and $XT(f_N) < -26$

- f_N= Nyquist frequency
- Voltage Transfer Function for 24 GT/s and 32 GT/s (Tx: 30 ohm / 0.125pF; Rx: 50 ohm / 0.125pF)
- [2] Section 5.7.1

UCIe VTF crosstalk evaluation fails as expected.

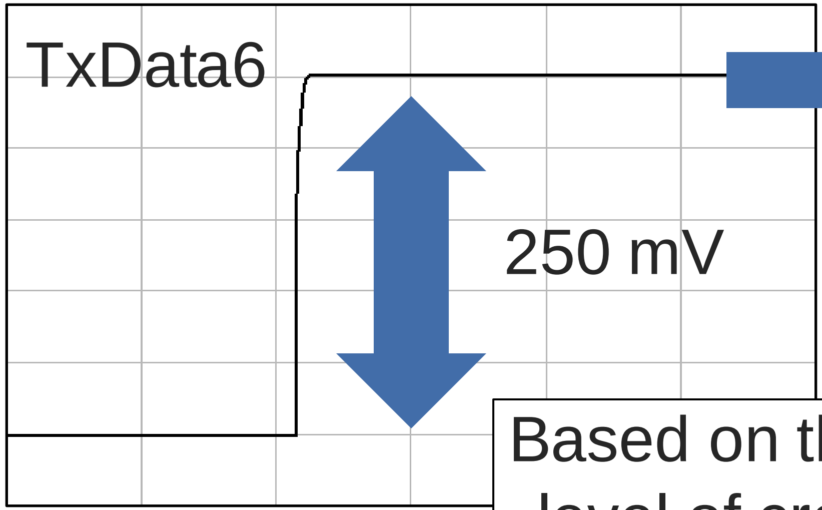


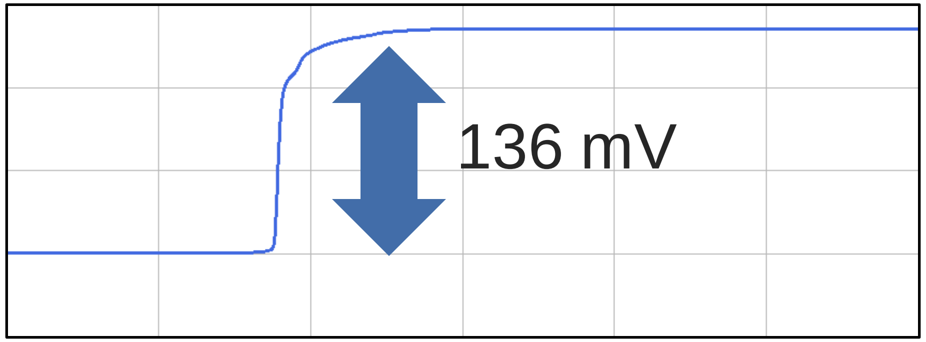
BoW's Crosstalk Criteria: Less Than 35% of Voltage Swing

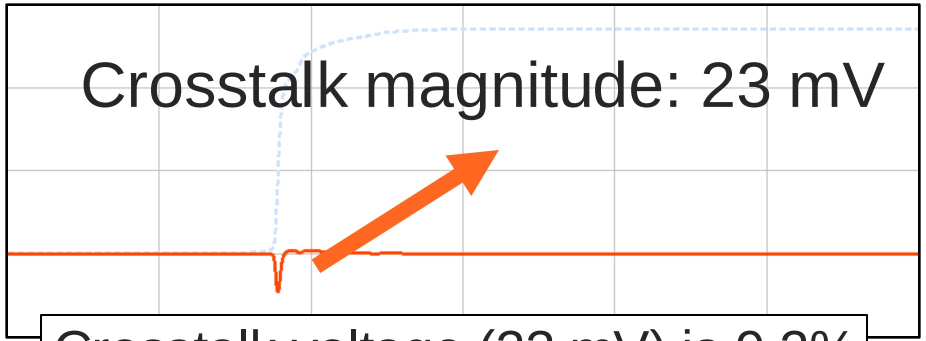


Standard package

12.3.2 Crosstalk [3]
The total crosstalk observed on an individual signal within a BoW-256 channel should typically be less than ~35% of the signal swing.





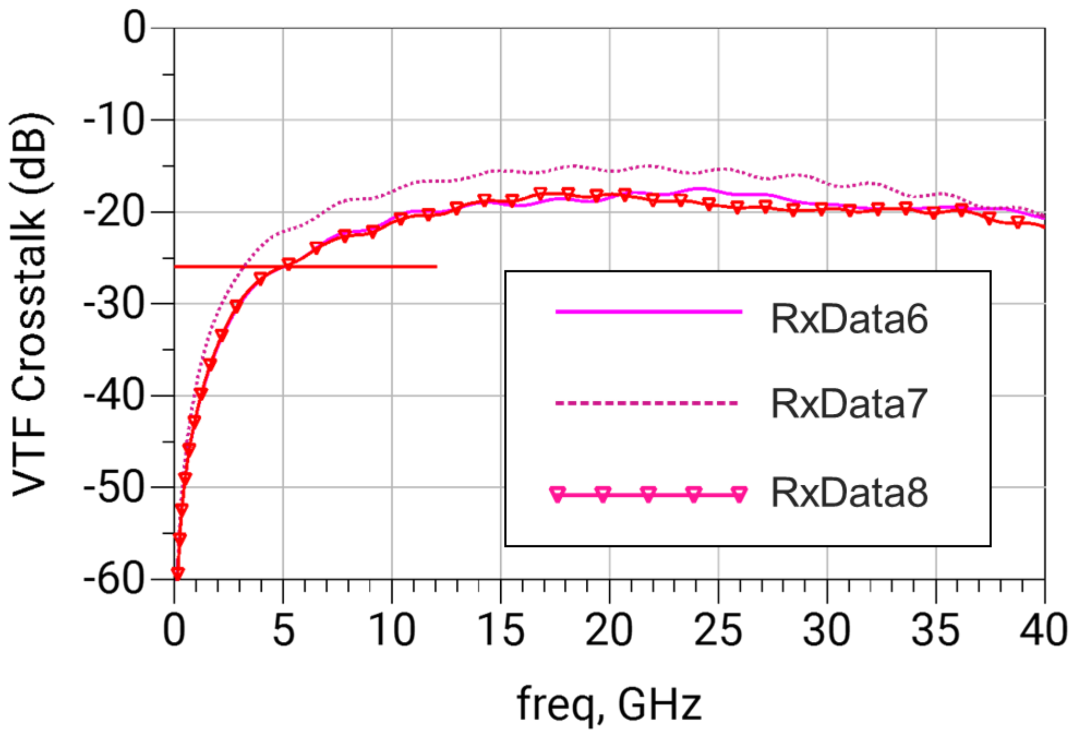


Based on the crosstalk criteria, the level of crosstalk seems fine, but we know the eye is closed and we expect it to fail.

Crosstalk voltage (23 mV) is 9.2% of the swing (250 mV).

KEYSIGHT

UCIe Provides More Consistent Crosstalk Metrics Than BoW

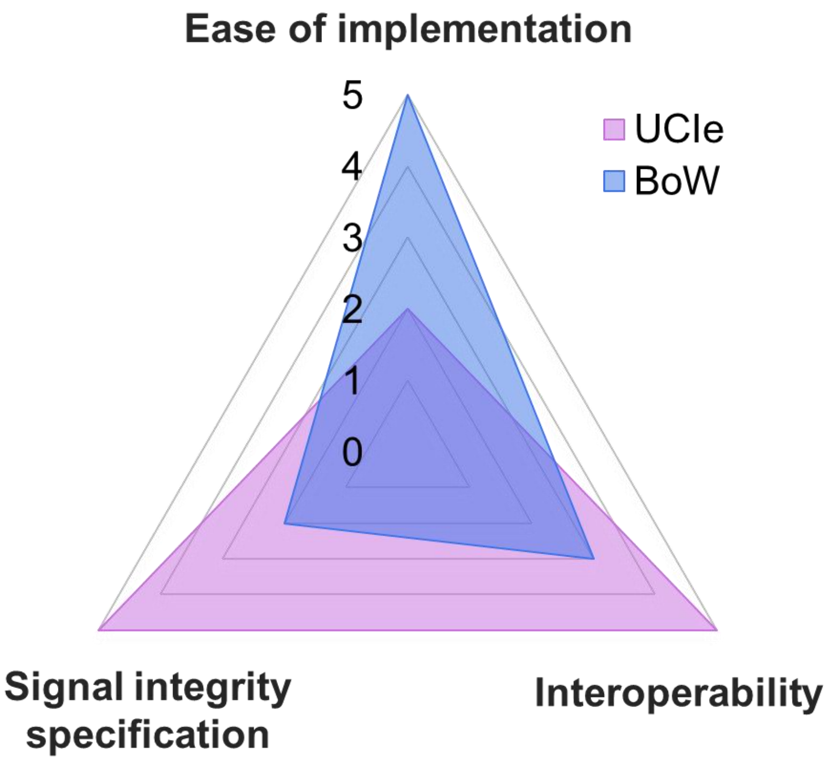


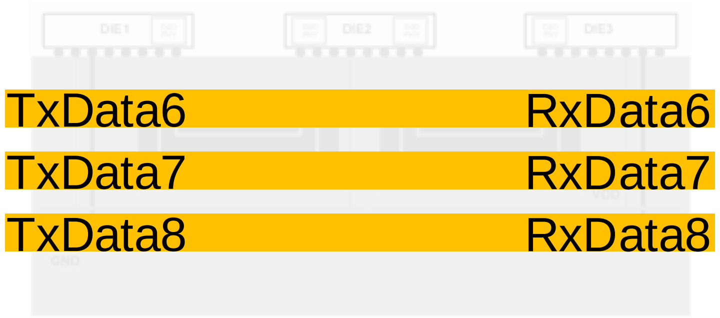
BoW does not place any direct requirements on characteristics such as channel loss or crosstalk.

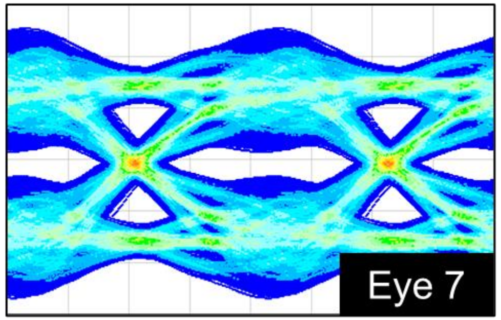
12.3.2 Crosstalk
The total crosstalk observed on an individual signal within a BoW-256 channel should typically be less than ~35% of the signal swing.

We failed UCIe crosstalk evaluations failed as expected.
However, BoW provides us with an evaluation inconsistent with our expectation.

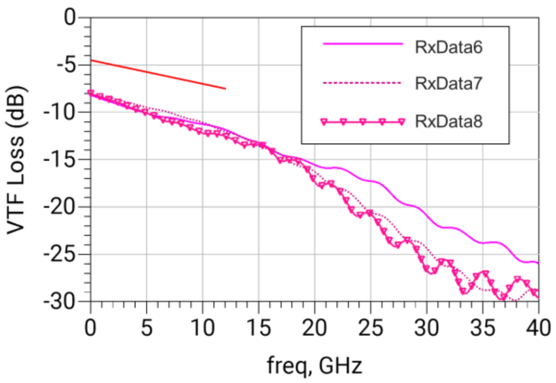
UCIe vs. BoW: Overall UCIe Is More SI-Friendly

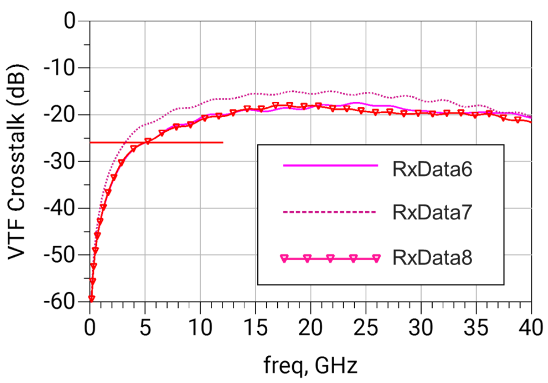






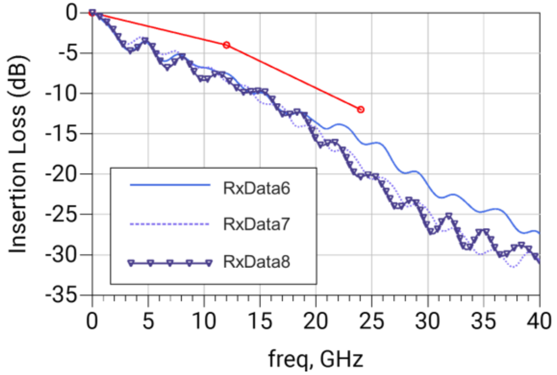
UCIe™
Universal Chiplet
Interconnect Express





A channel case study showed that UCIe provides more SI metrics.

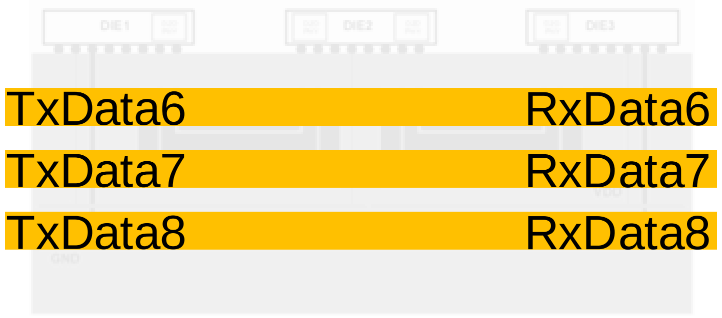
BoW
OPEN
Compute Project



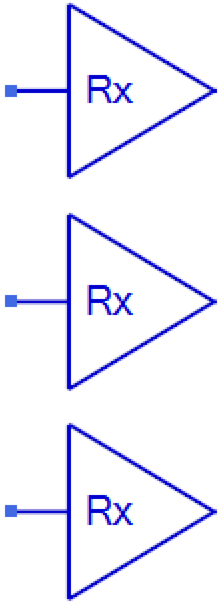
Gain SI Insights from the Broken Channel

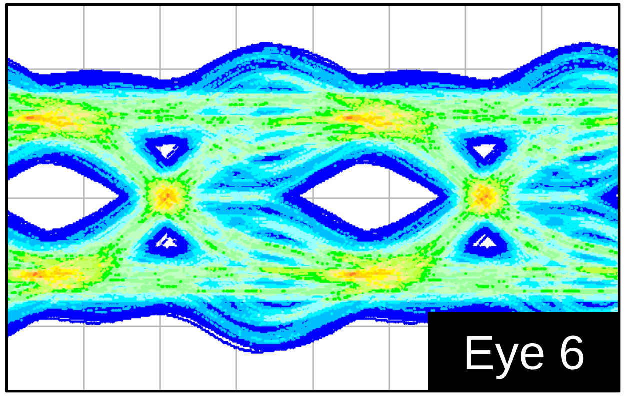
Qualitative Assessment of the Eye Diagram Is Not Positive

3 Transmitters
Standard package
24 GT/s

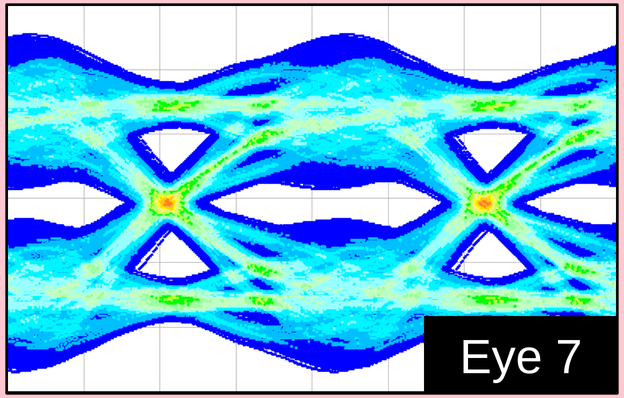


3 Receivers
No EQ
Terminated

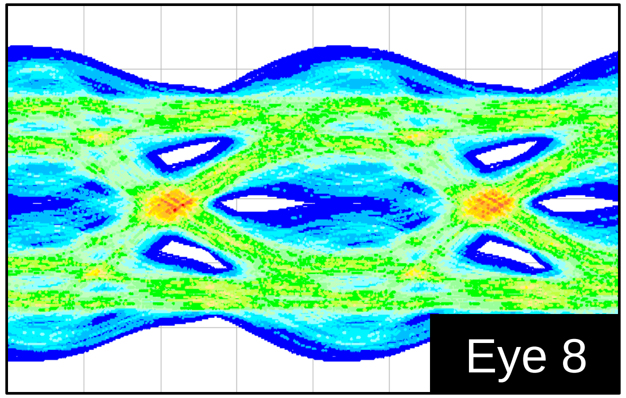




Not good



Bad

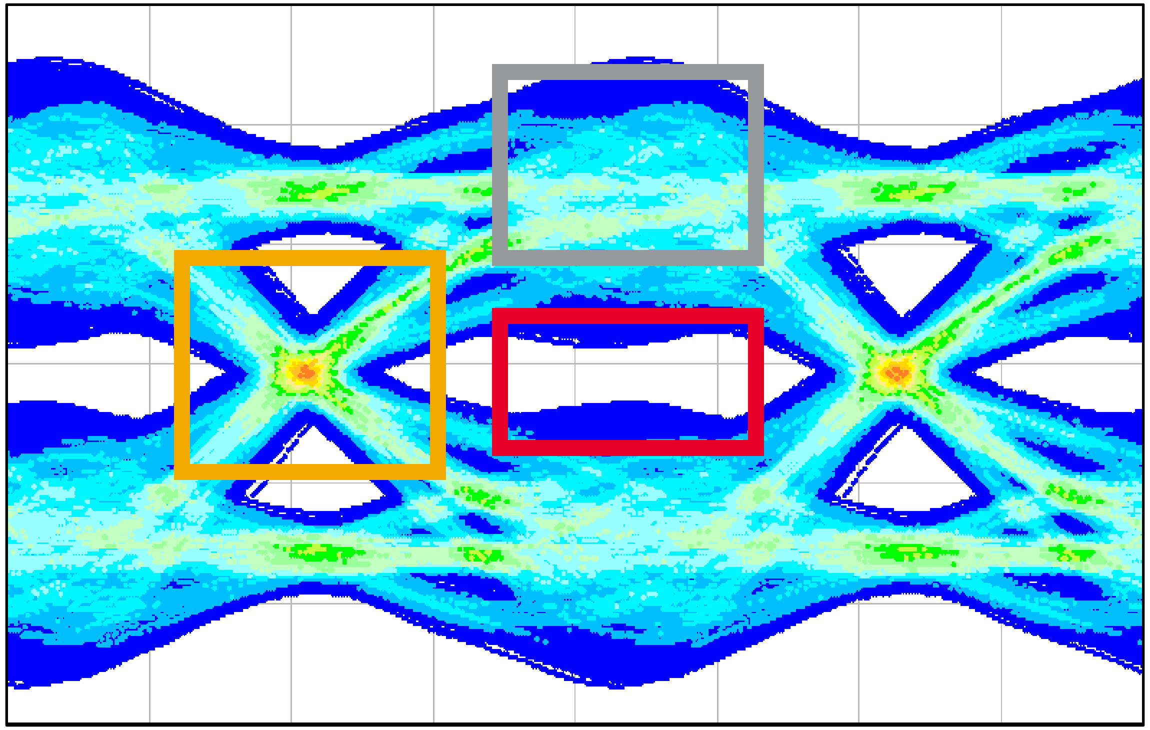


Very bad

KEYSIGHT

Eye Shows Reflection, Crosstalk, and Considerable Loss

Received eye at RxData7 without equalization

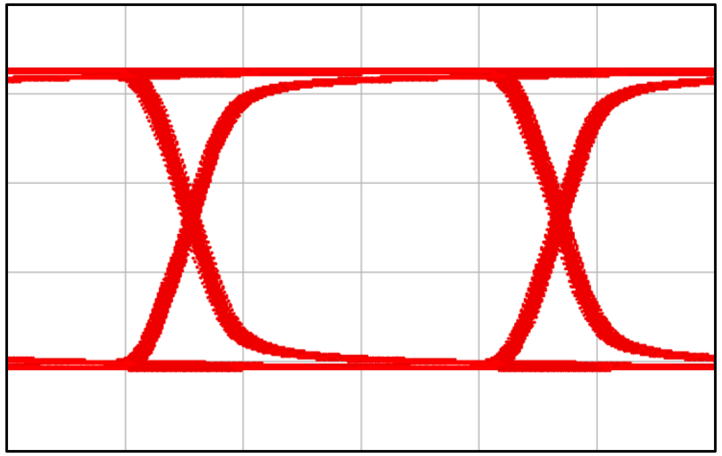


1. Signs of reflection
2. Signs of crosstalk
3. Signs of frequency-dependent loss

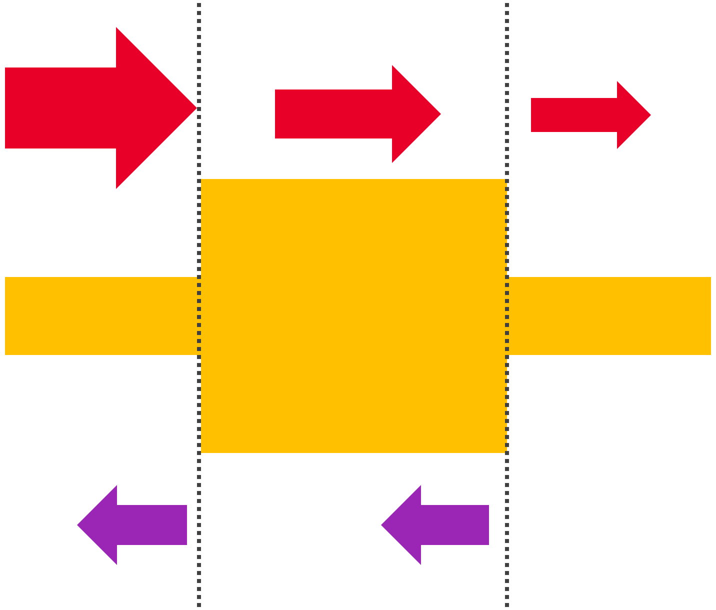
Rule Number 9: Anticipate Before You Measure or Simulate [4]

Reflection Degrades the Amplitude of the Transmitted Signal

Moderate loss channel
With no discontinuities



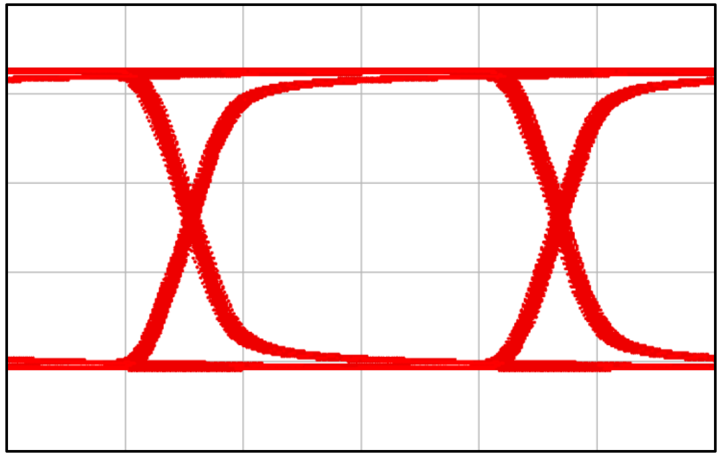
Moderate loss channel
With impedance discontinuities



One expects the received amplitude to be smaller than intended because part of the transmitted amplitude is reflected.

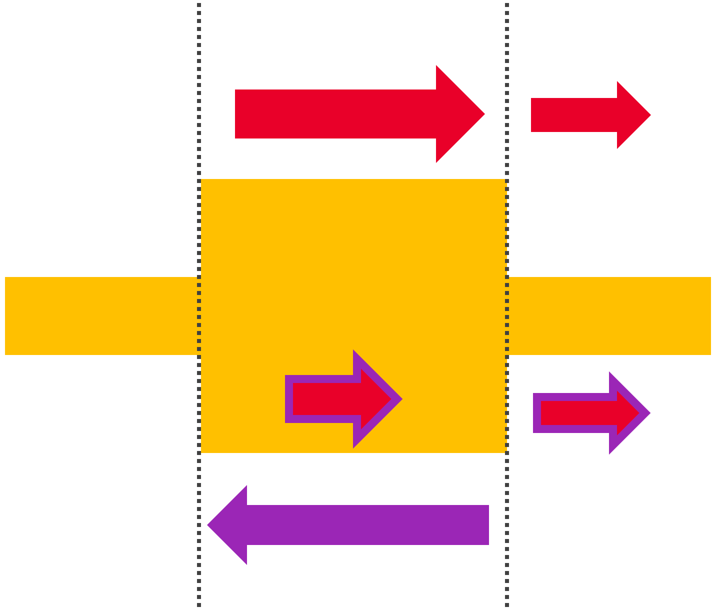
Reflections in the System Deform the Received Eye Shape

Moderate loss channel
With no discontinuities



Moderate loss channel

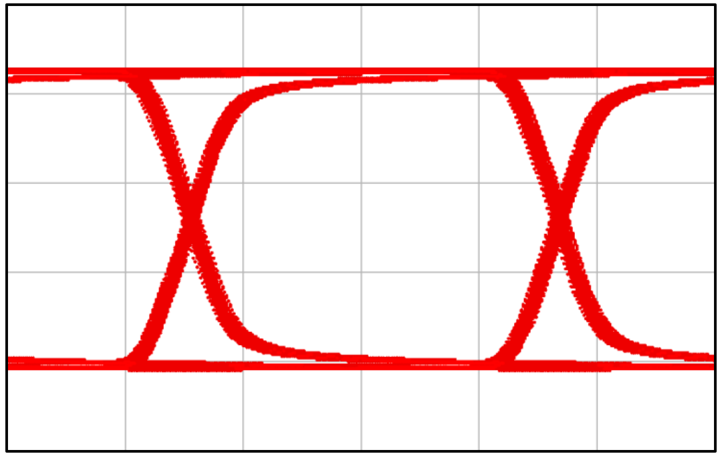
With impedance discontinuities



One expects the received eye shape to be deformed by the multiple reflections in the system.

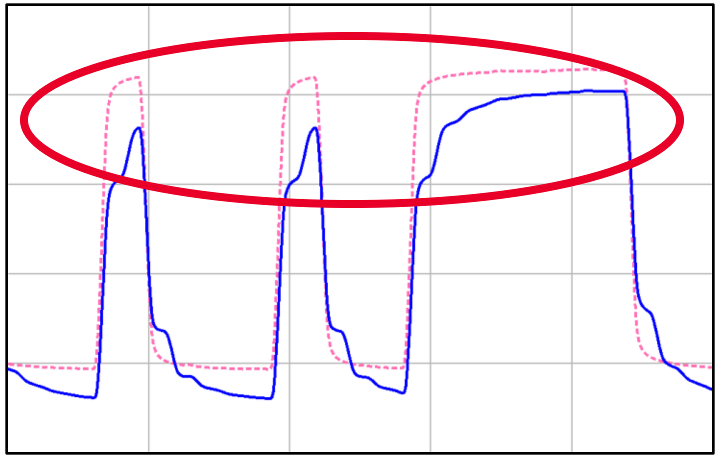
Reflections in the System Deform the Received Eye Shape

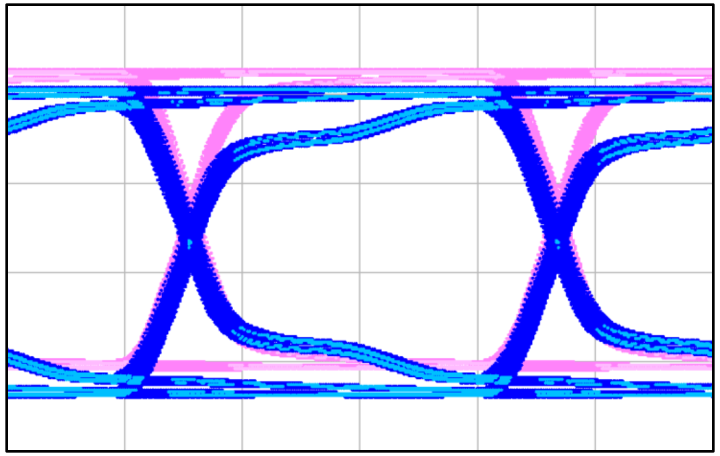
Moderate loss channel
With no discontinuities



Moderate loss channel

With impedance discontinuities



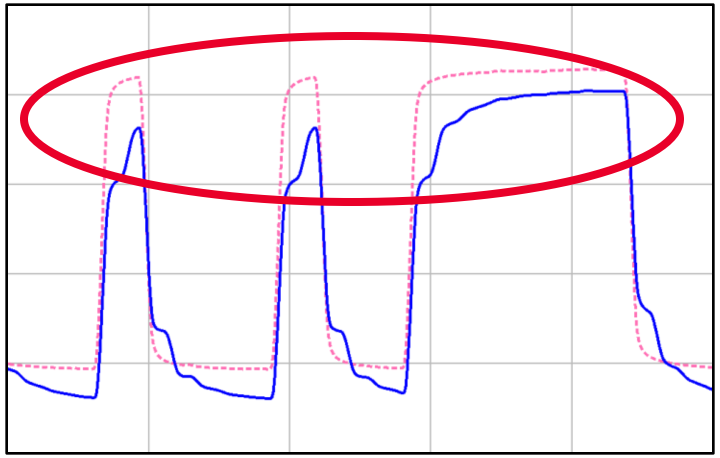


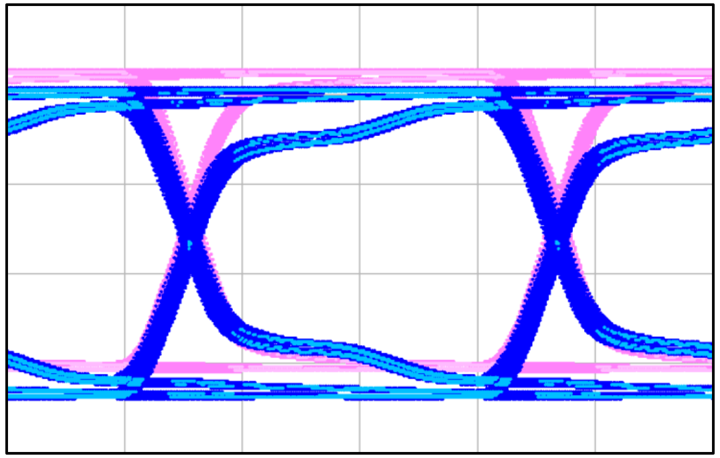
As expected, impedance discontinuity degrades both the eye amplitude and shape.

Fix Eye Closure by Removing Impedance Discontinuities

Moderate loss channel

With impedance discontinuities

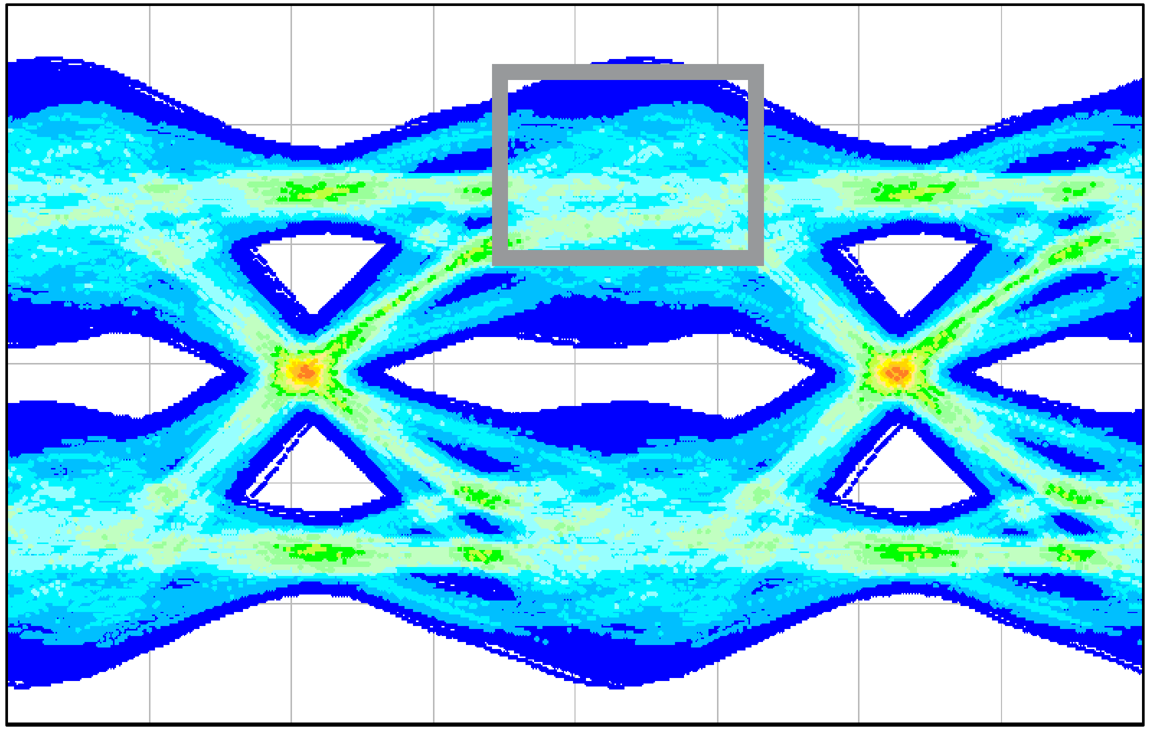




Signs in the Eye	Root cause	Fixes
• Deformed eye shape • Reduced eye amplitude	Impedance discontinuities	• Locate impedance discontinuity and match it with channel impedance

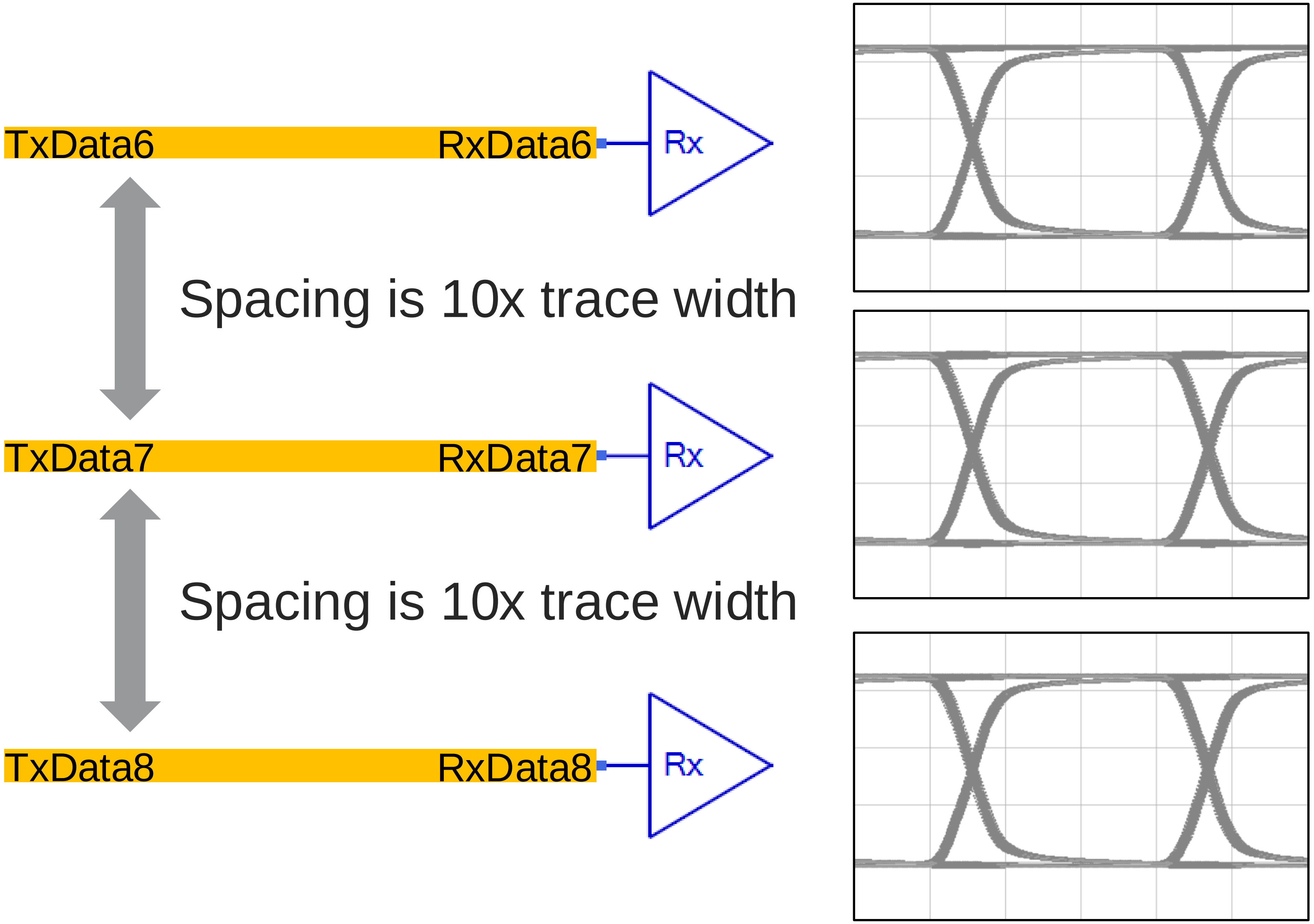
Eye Shows Reflection, Crosstalk, and Considerable Loss

Received eye at RxData7 without equalization



2. Signs of crosstalk

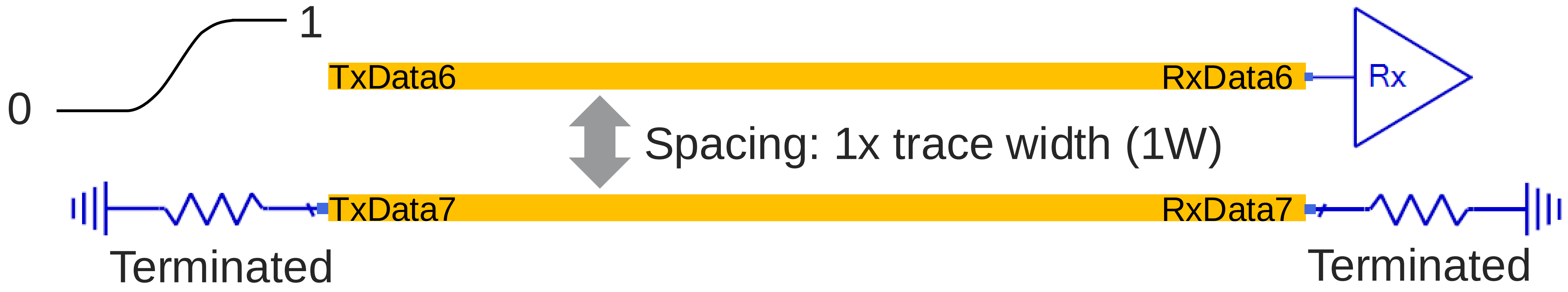
Eyes Are Open When the Channel Are 10 Trace-width Apart

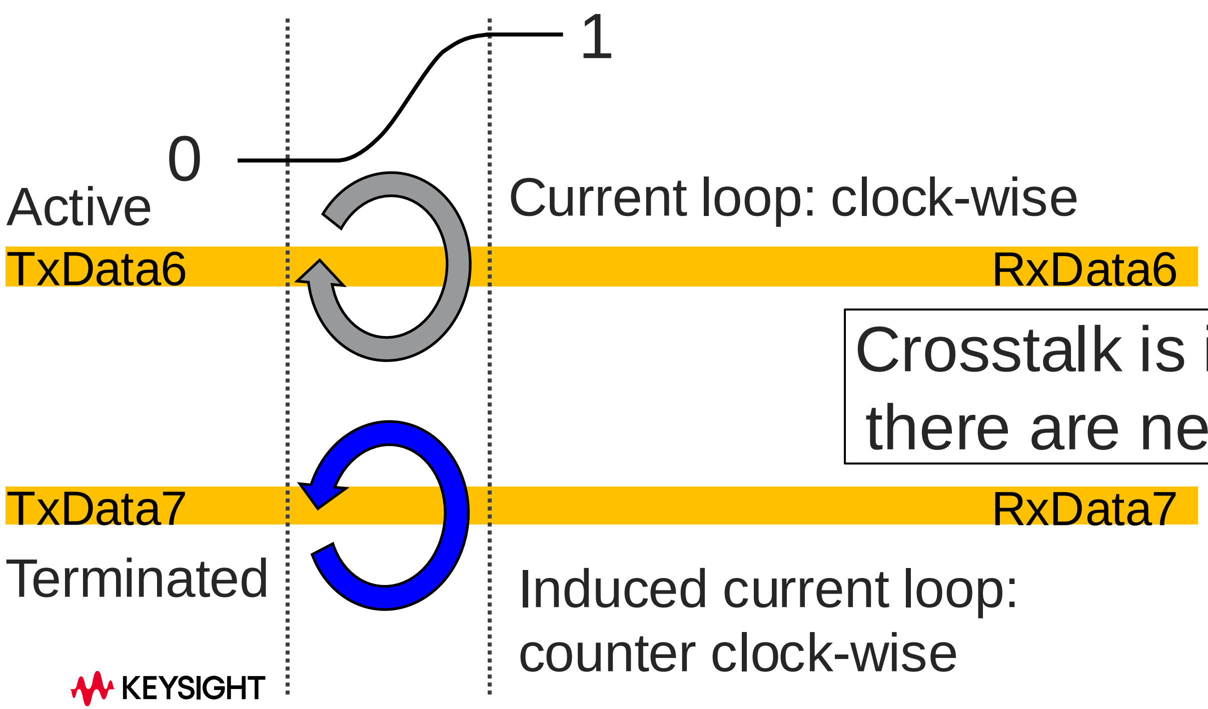


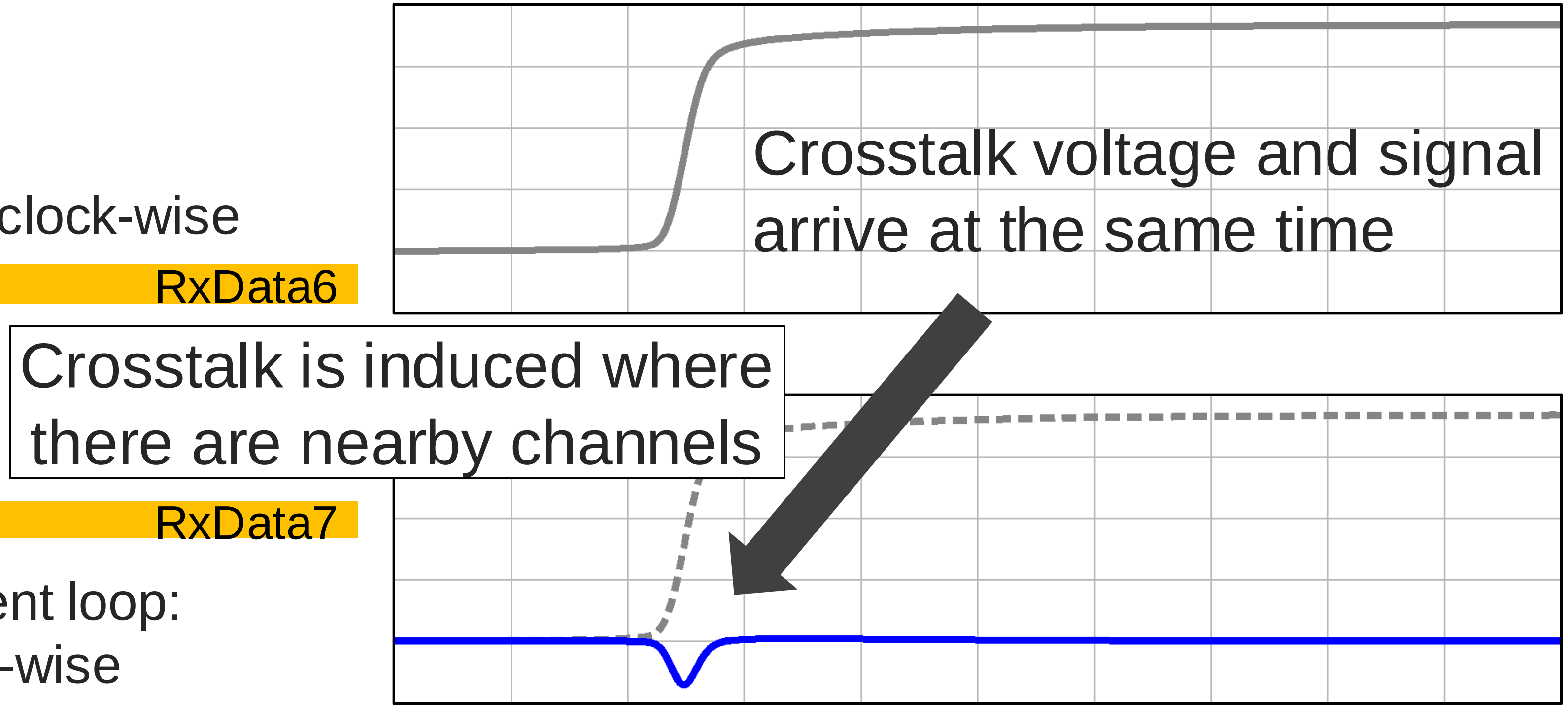
Eyes are open when the channels are 10 trace width apart.

There is no crosstalk when the channels are far from each other.

Expect Far-end Crosstalk When Channels Are Close

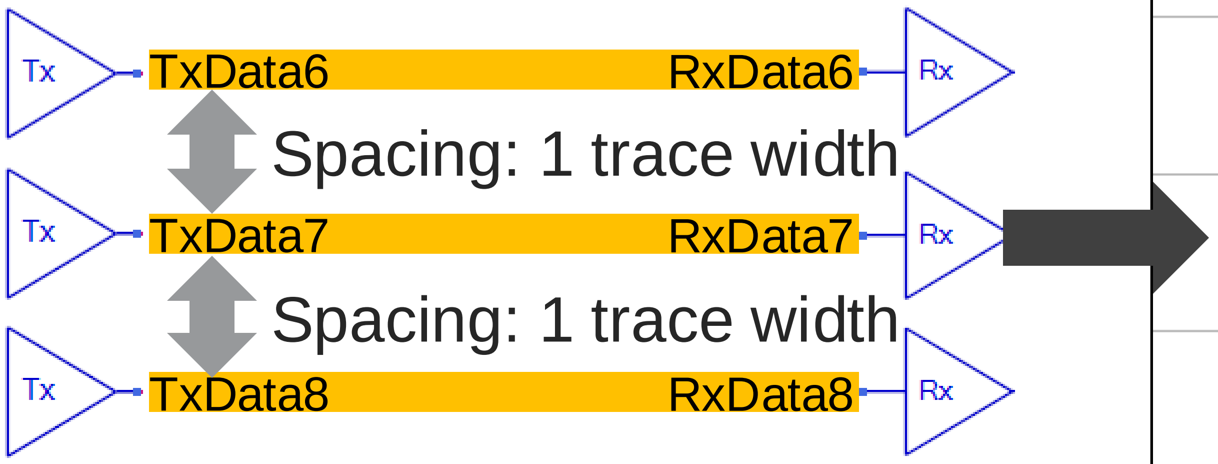




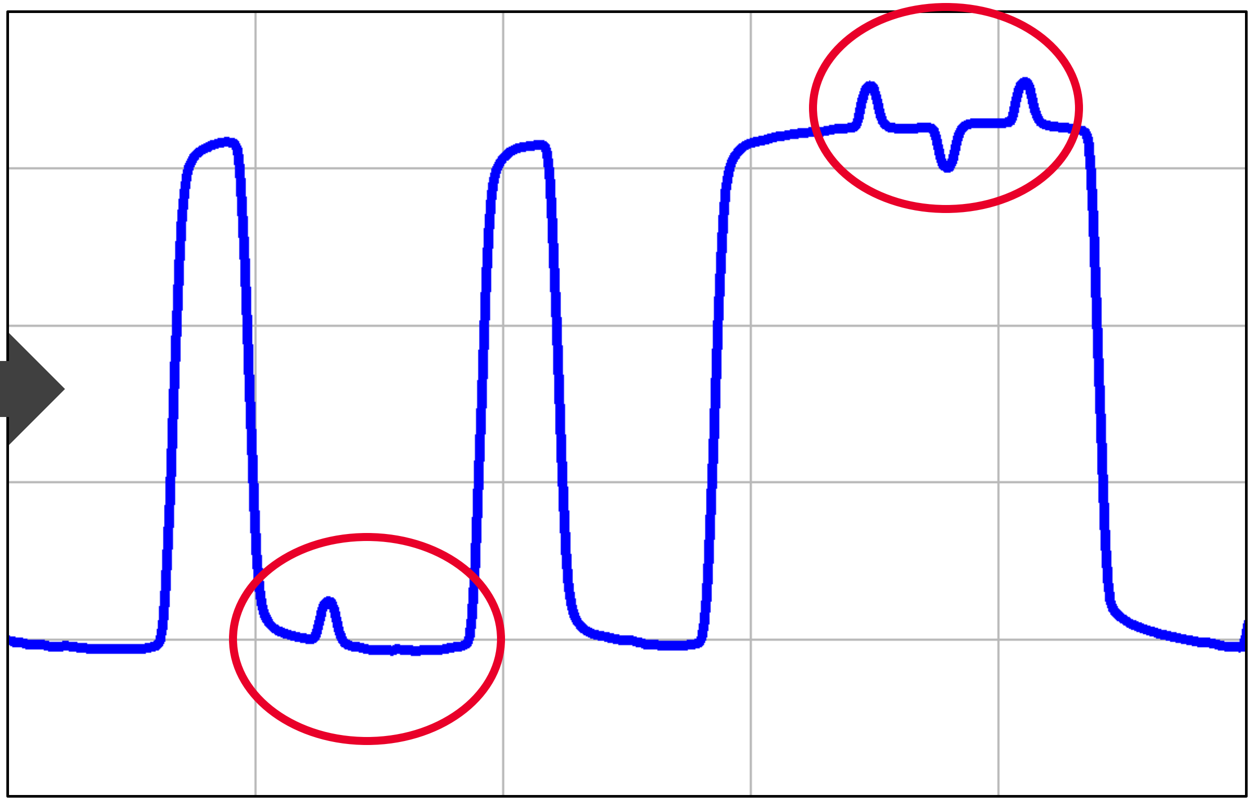


Far-end Crosstalk Signatures in the Waveform

Channels are close and they are all active



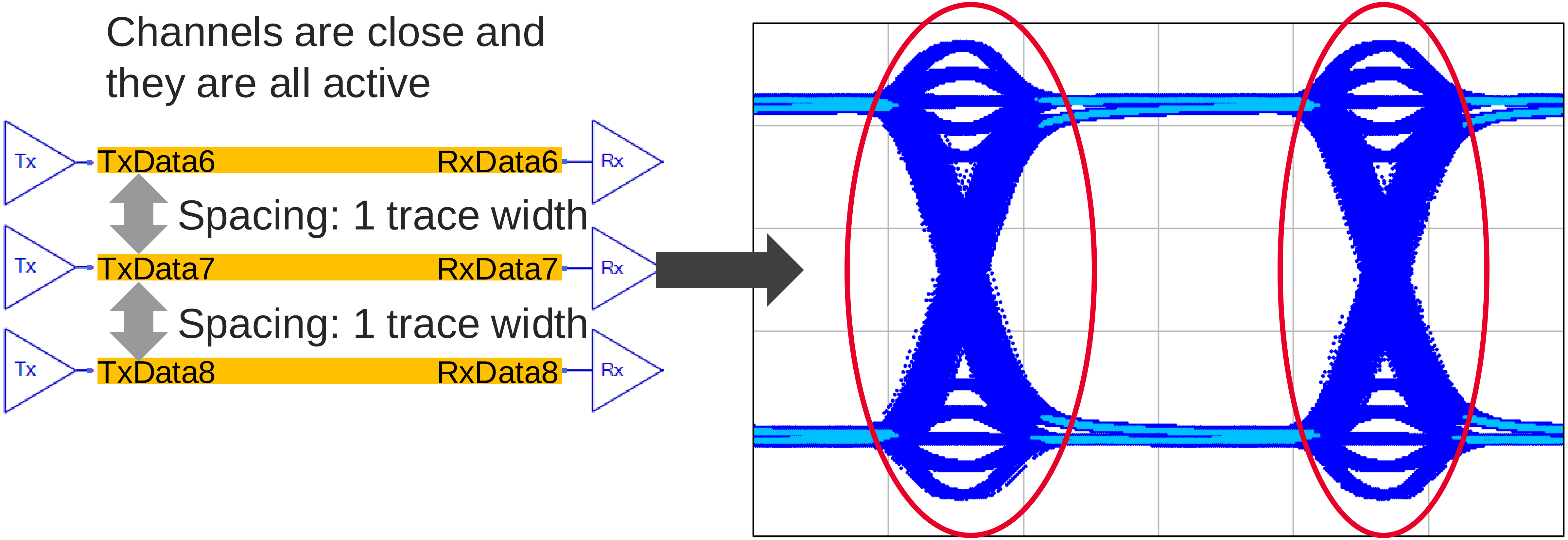
Crosstalk voltage signature in RxData7's waveforms



Far-end Crosstalk Signatures in the Eye

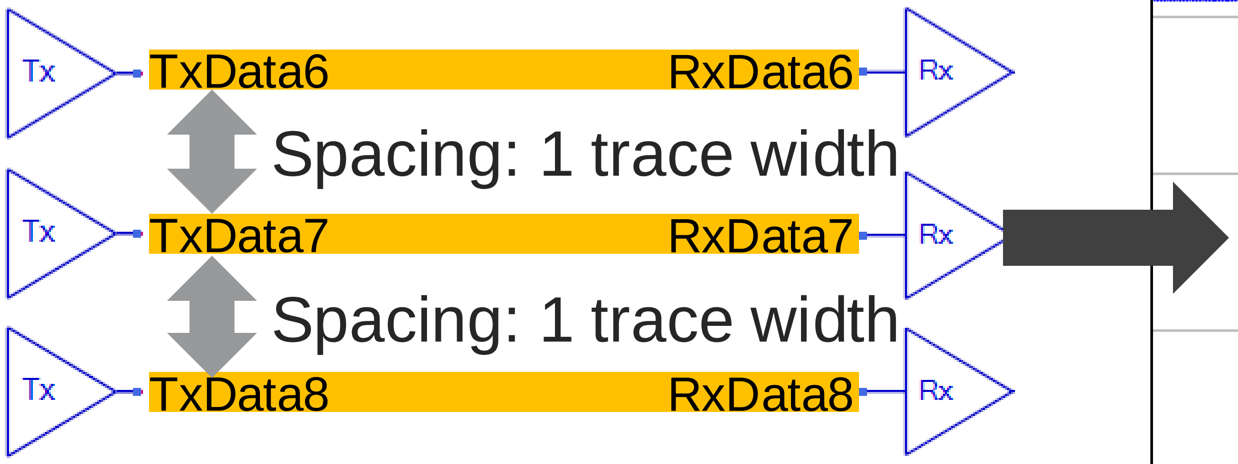
Crosstalk voltage signature in RxData7's waveforms

Channels are close and they are all active

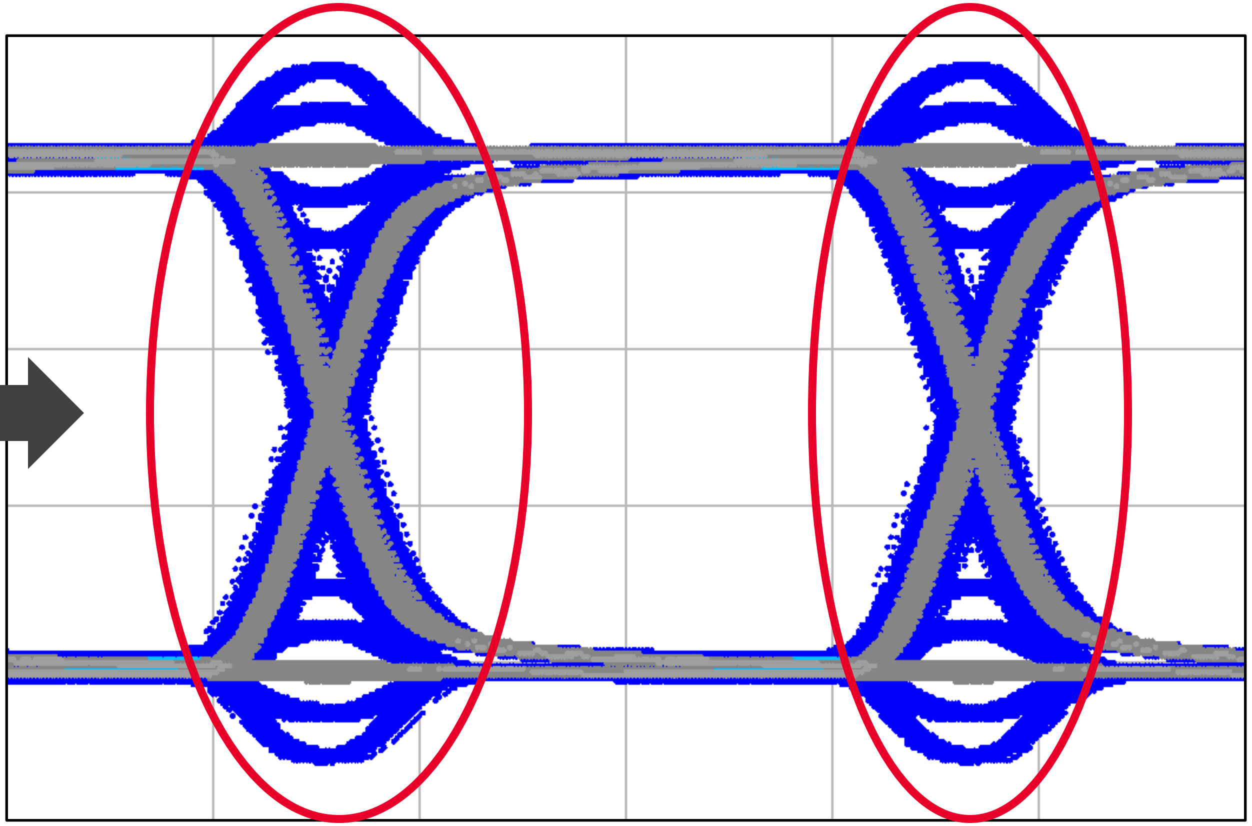


Far-end Crosstalk Signatures in the Eye

Channels are close and they are all active



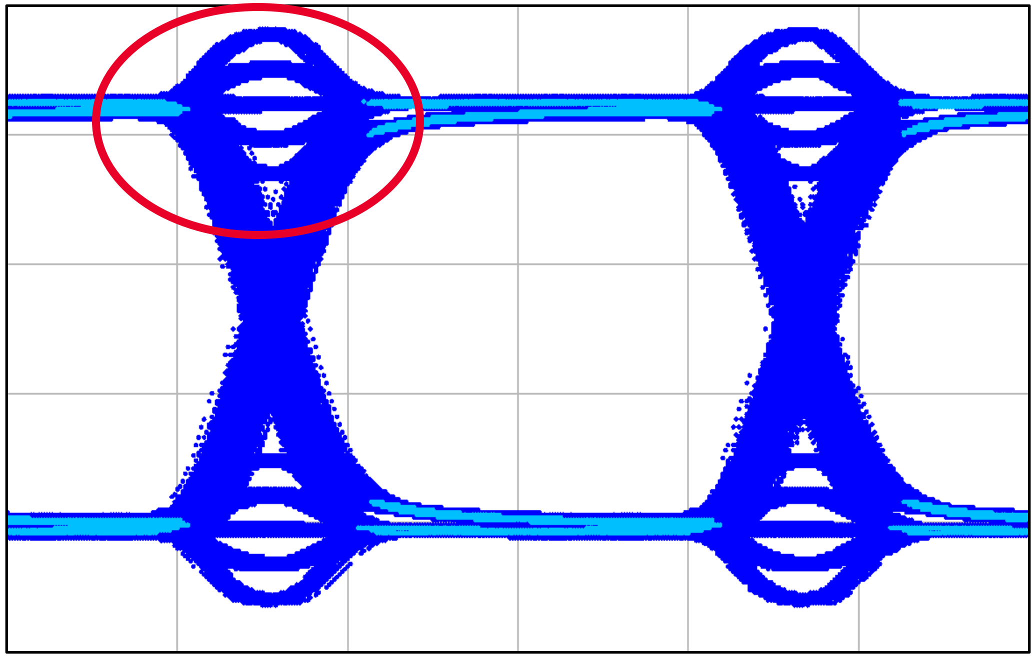
Crosstalk voltage signature in RxData7's waveforms



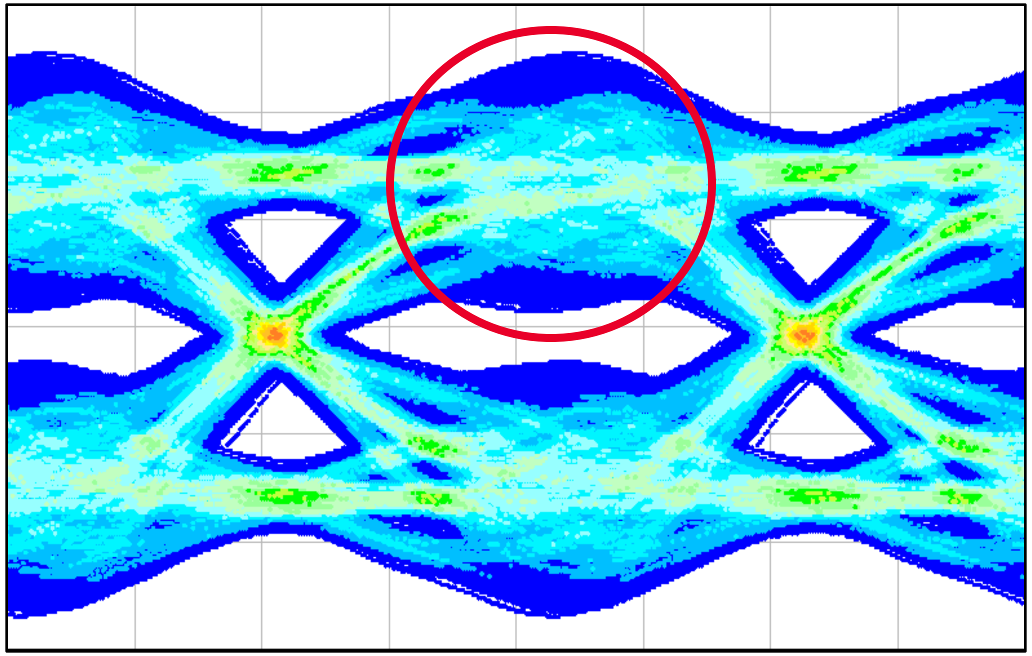
Far-end crosstalk shows up as peaks in the transitions

Far-end Crosstalk Signature Looks Different

Received eye example

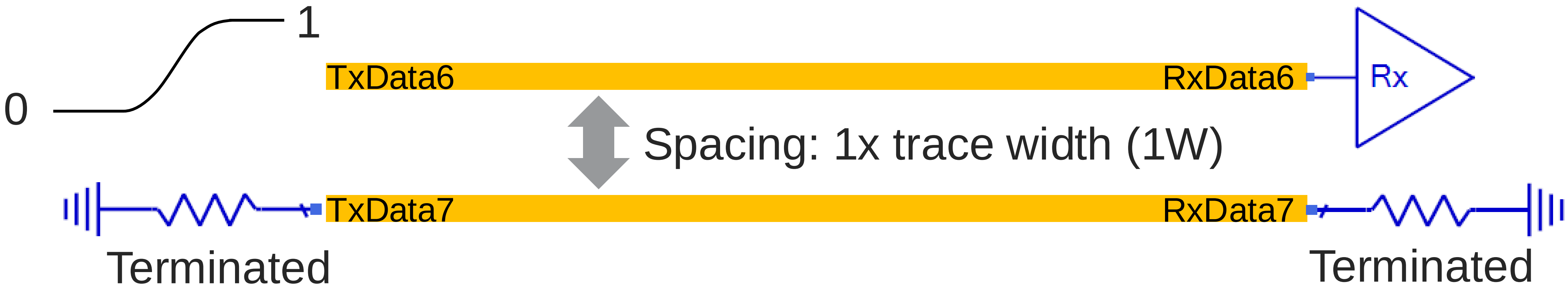


Received eye at RxData7
without equalization

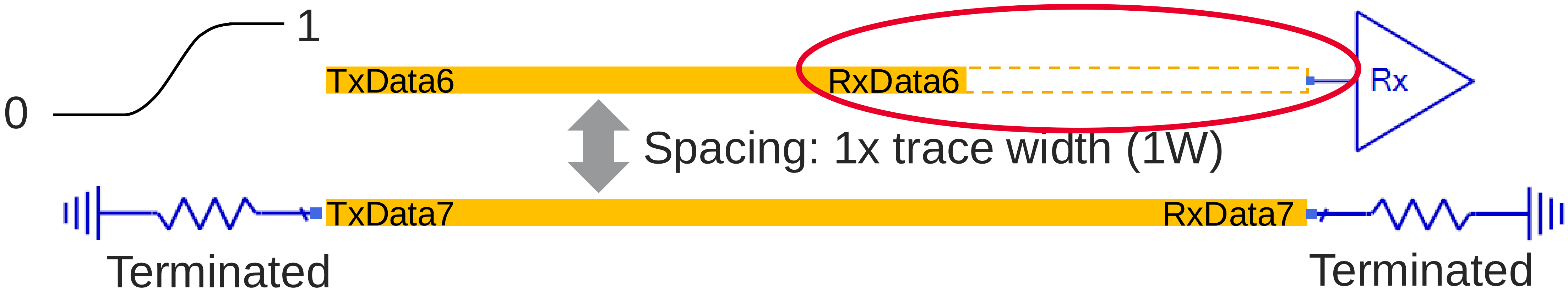


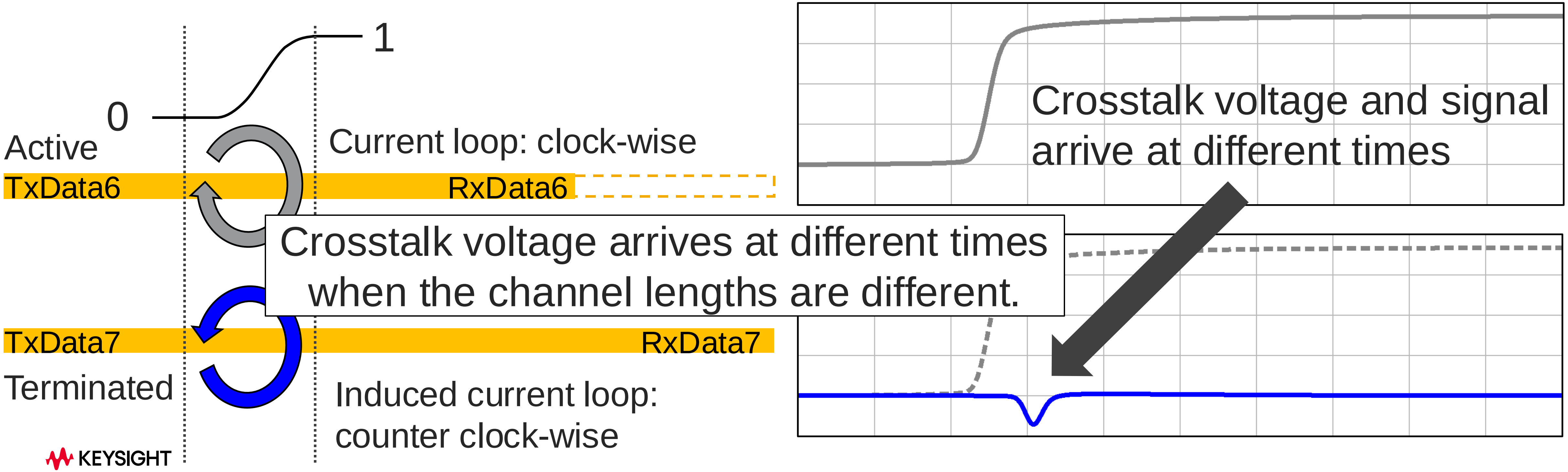
KEYSIGHT

Previous Channels Have the Same Lengths



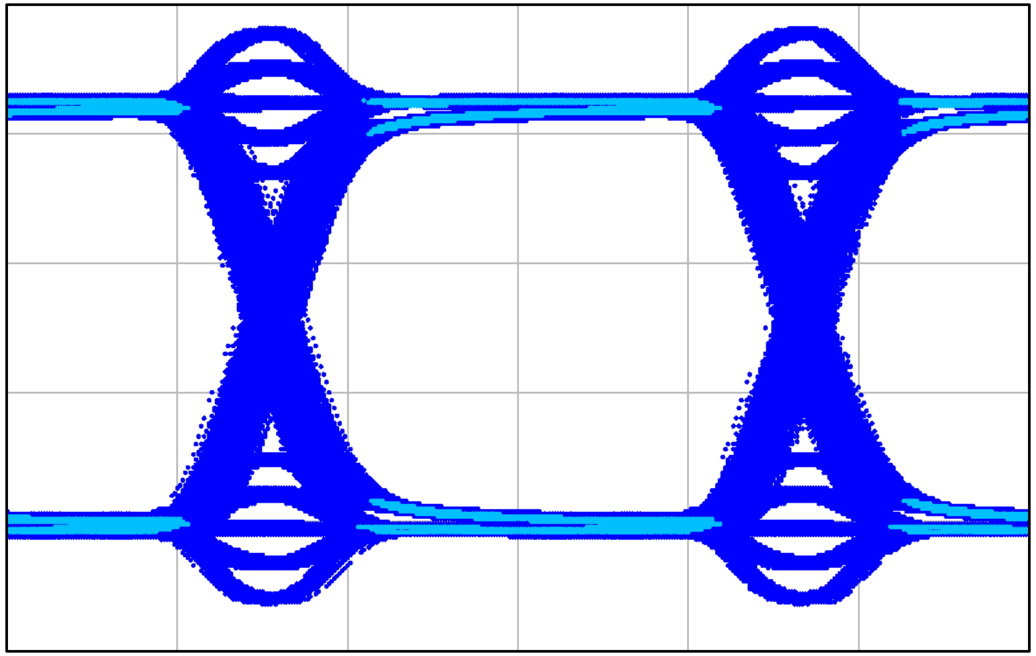
Change the Channel Length to Offset the Timing of Crosstalk



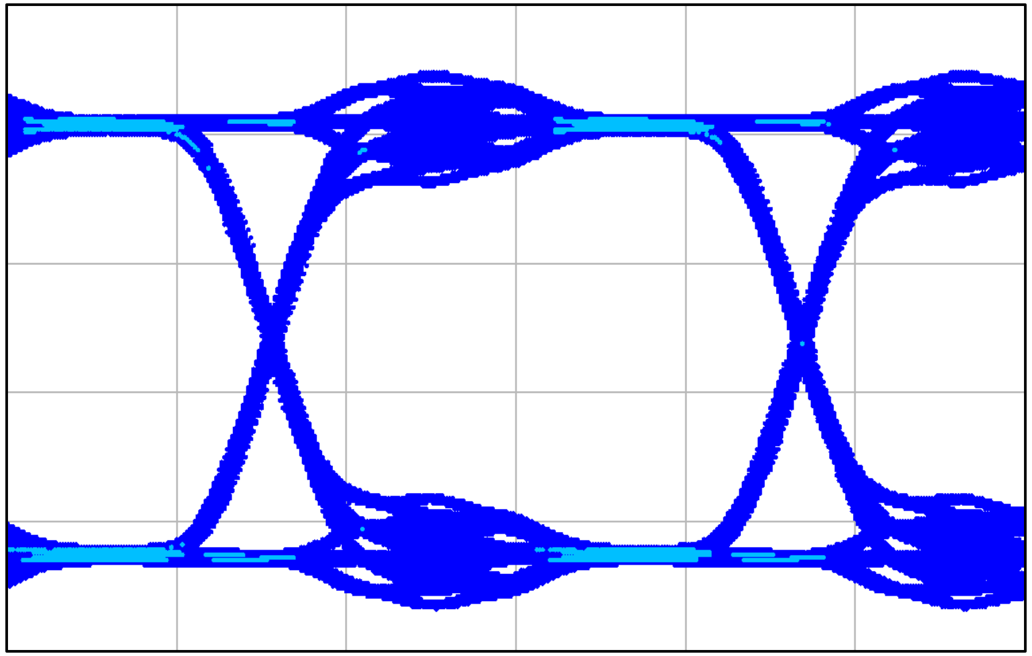


Xtalk and Length Variation Cause Vertical Eye Collapse

Received eye example
With **same channel lengths**



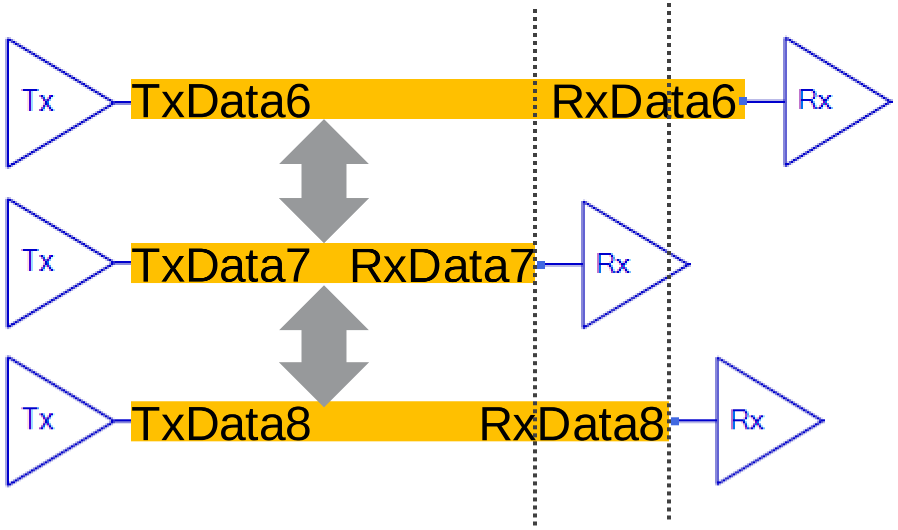
Received eye example
With **different channel lengths**

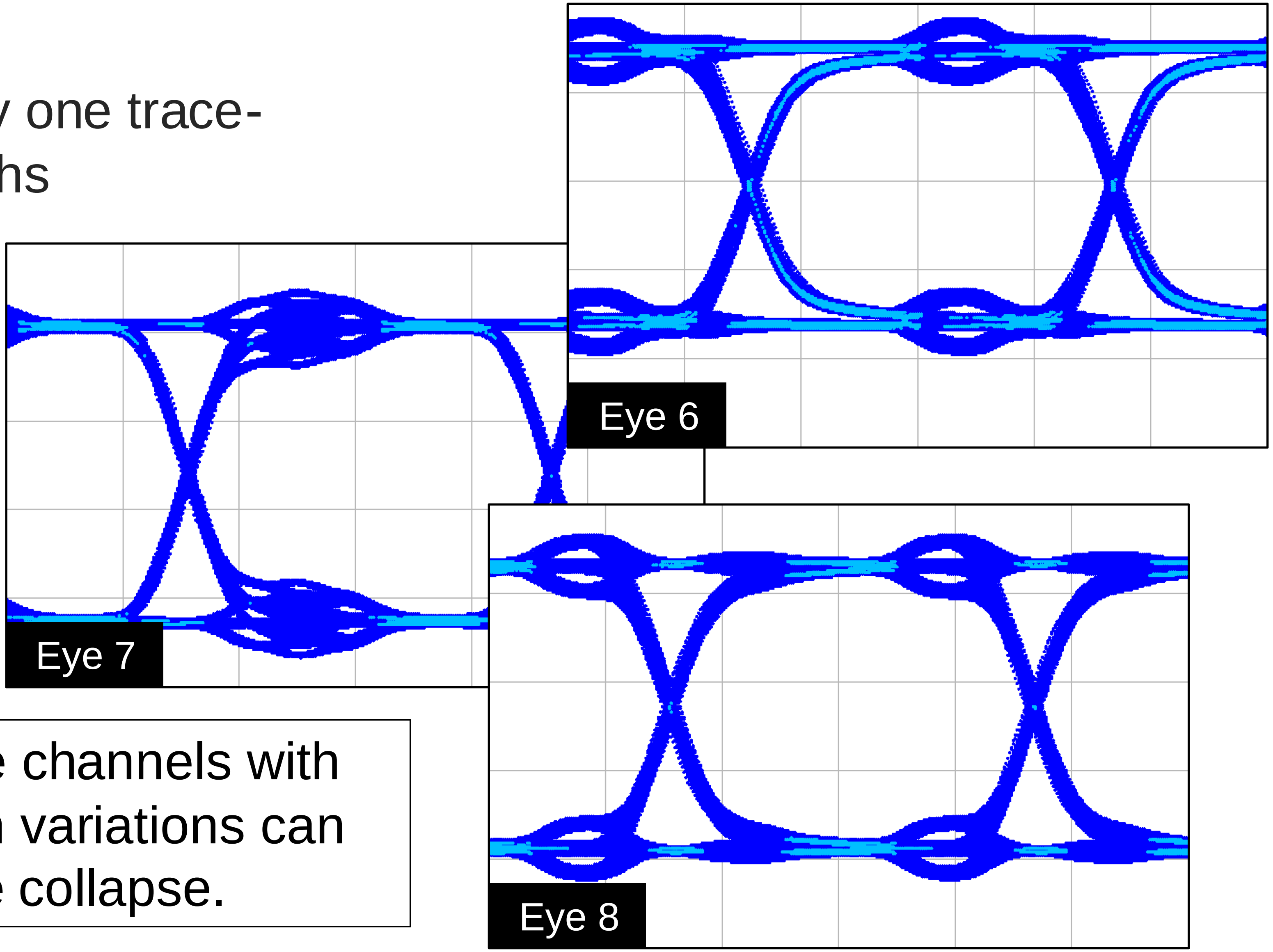


Crosstalk with channel length variations can cause vertical eye collapse!

Xtalk and Length Variation Cause Vertical Eye Collapse

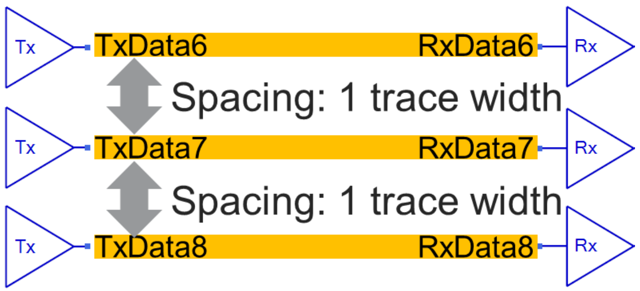
3 nearby channels separated by one trace-width and with all different lengths

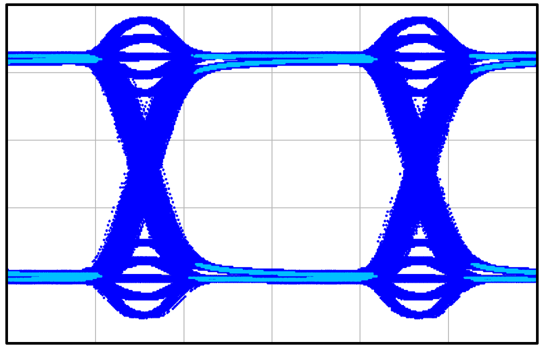


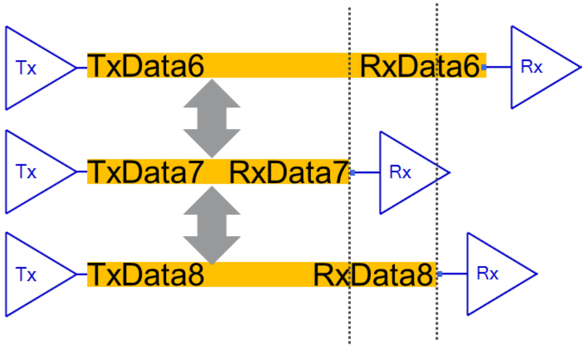


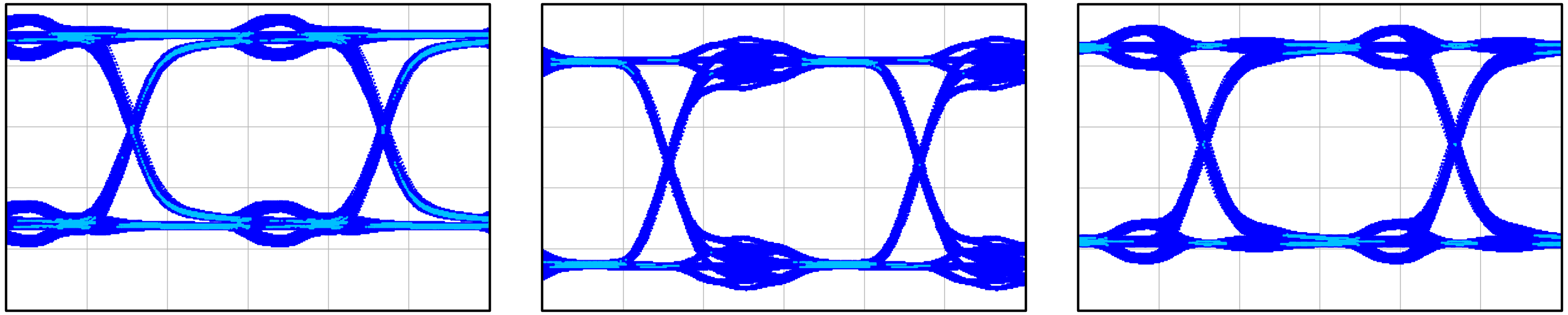
Crosstalk from multiple channels with multiple channel length variations can cause vertical eye collapse.

Fix Vertical Eye Closure by Increasing Channel Spacing







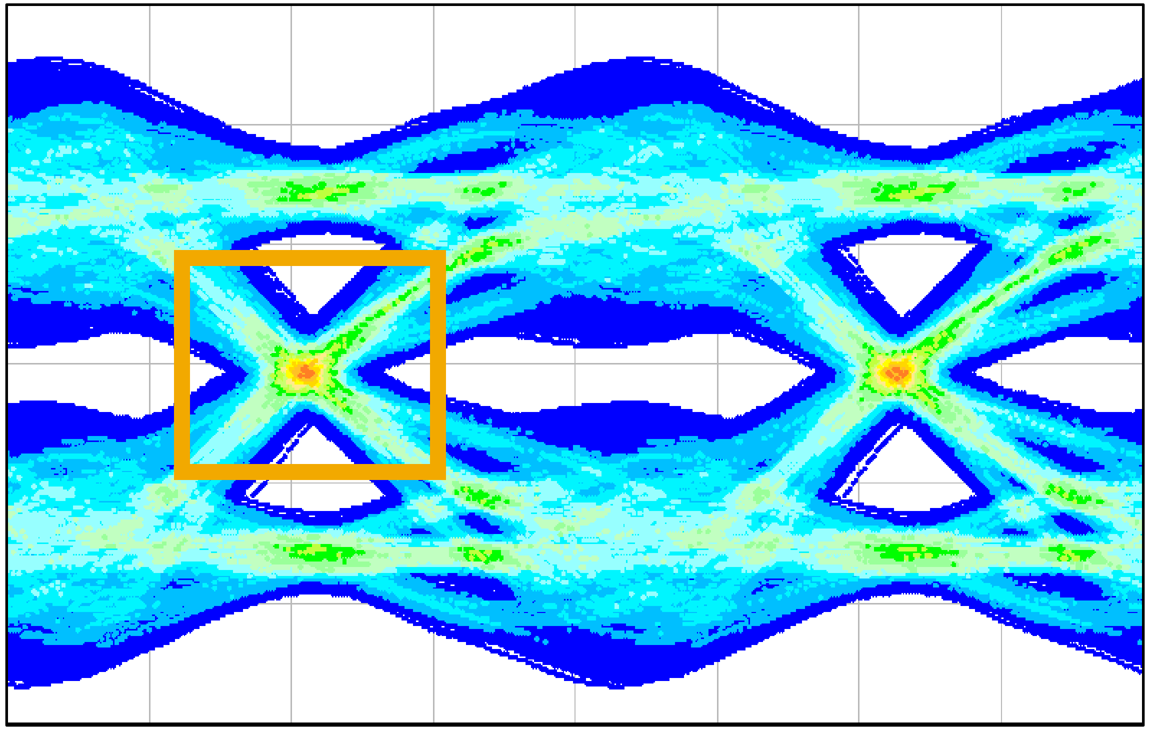


Signs in the Eye	Root cause	Fixes
• Peaks in eye transitions • Lumped peaks in the eyes	Crosstalk from adjacent channels	• Move channels farther apart • Maintain the same channel length

KEYSIGHT

Eye Shows Reflection, Crosstalk, and Considerable Loss

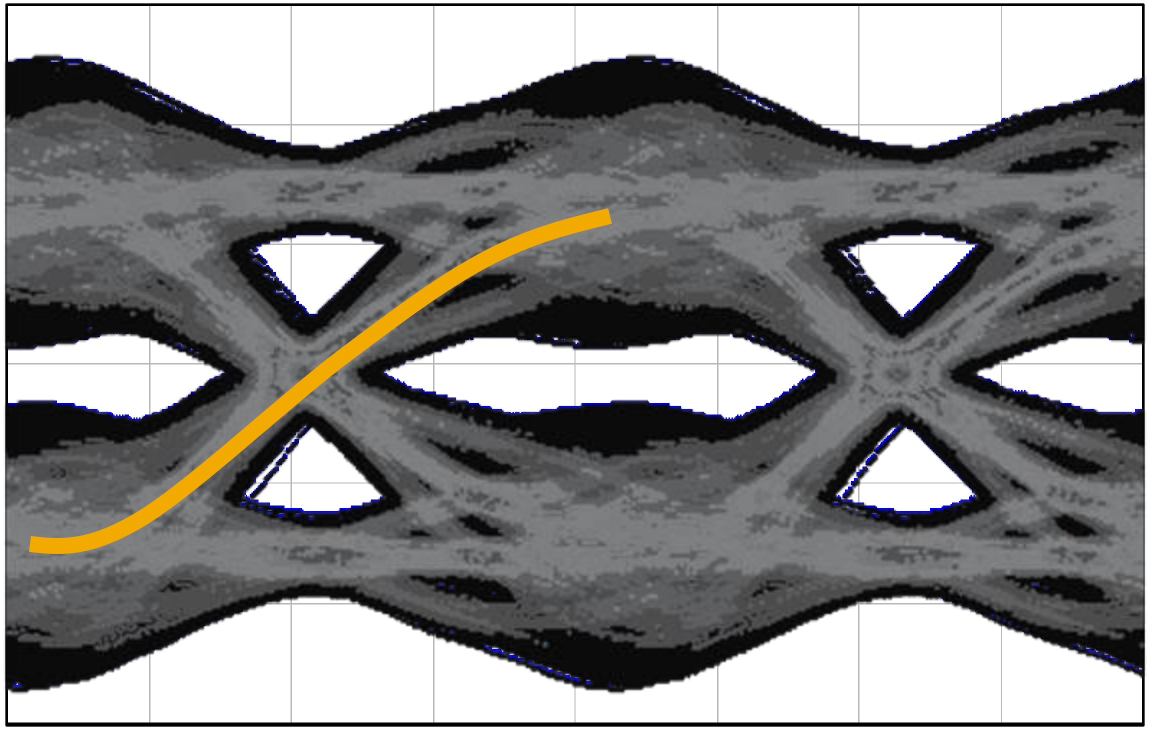
Received eye at RxData7 without equalization



3. Signs of frequency-dependent loss

Rise Time Degradation Indicates Loss in the Channel

Received eye at RxData7 without equalization

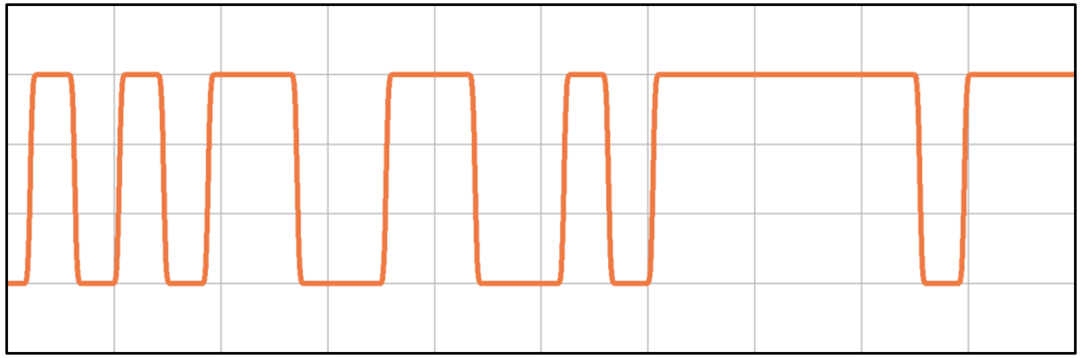


3. Signs of frequency-dependent loss

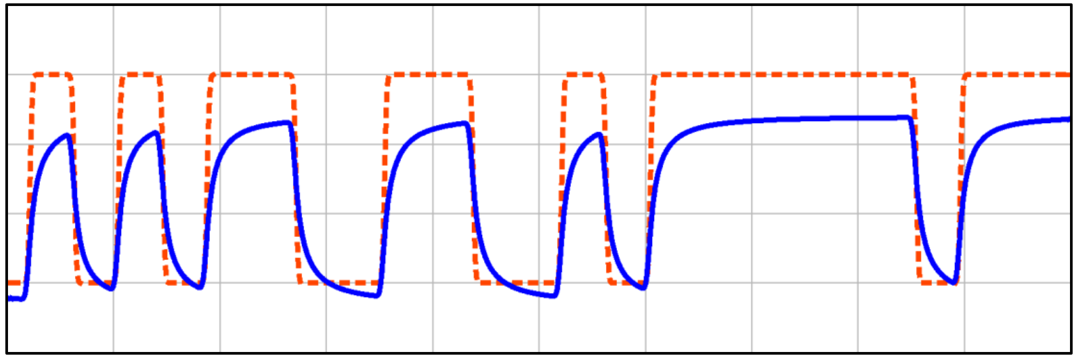
Frequency-dependent loss causes rise time degradation which reduces both timing margin and voltage margin.

Interconnects Attenuate High-frequency Components More

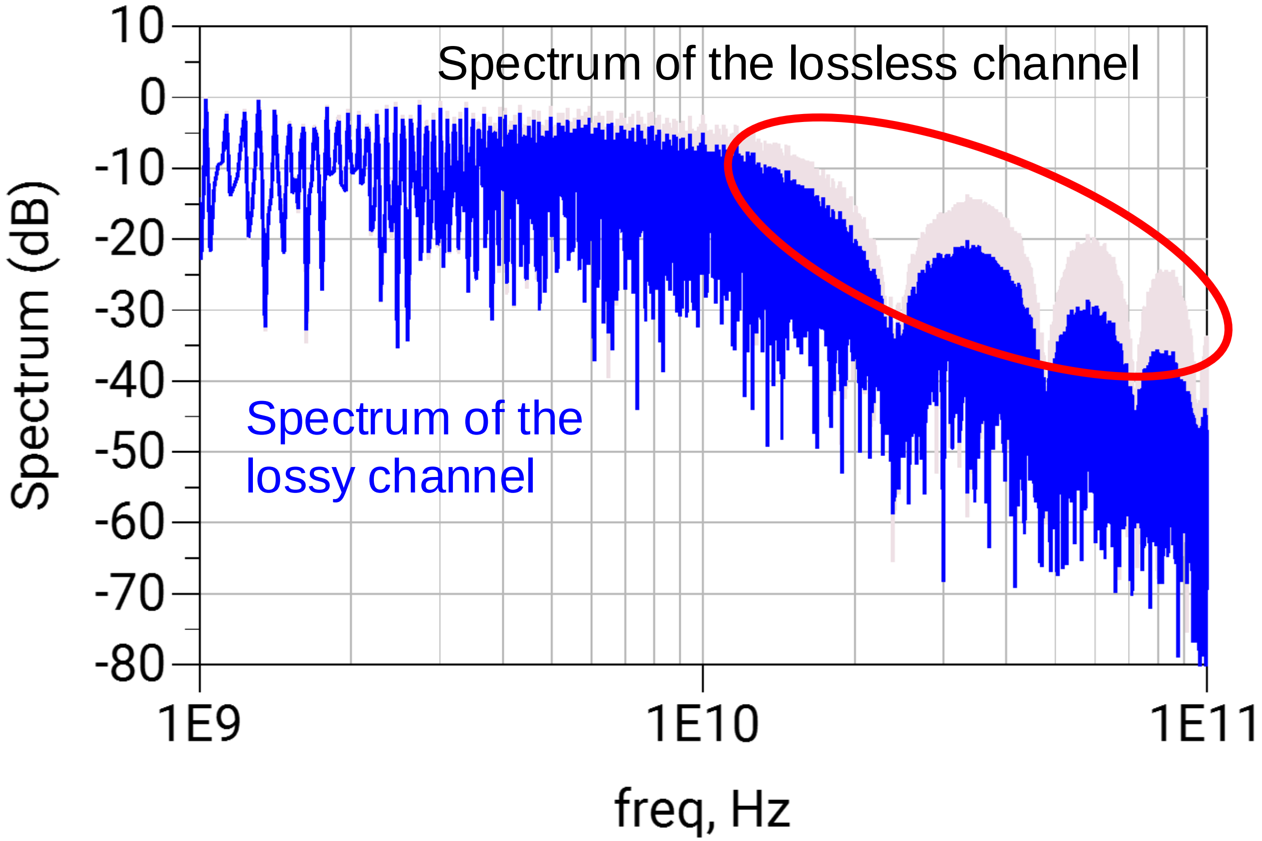
Received waveform after a lossless channel



Received waveform after a lossy channel



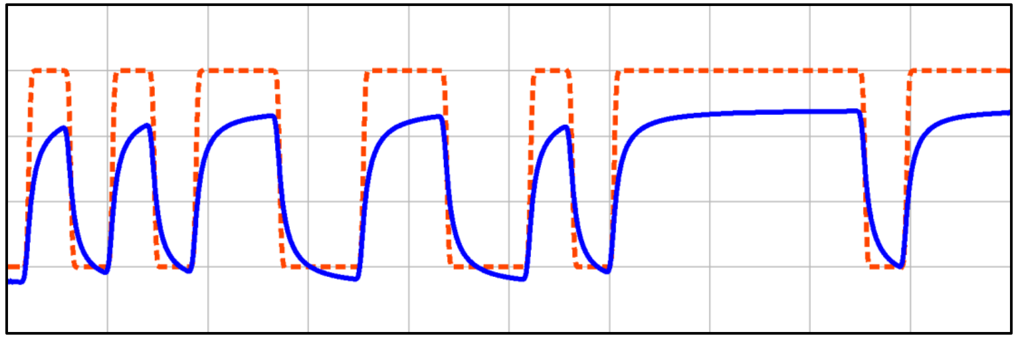
The lossy channel acts as a low-pass filter.

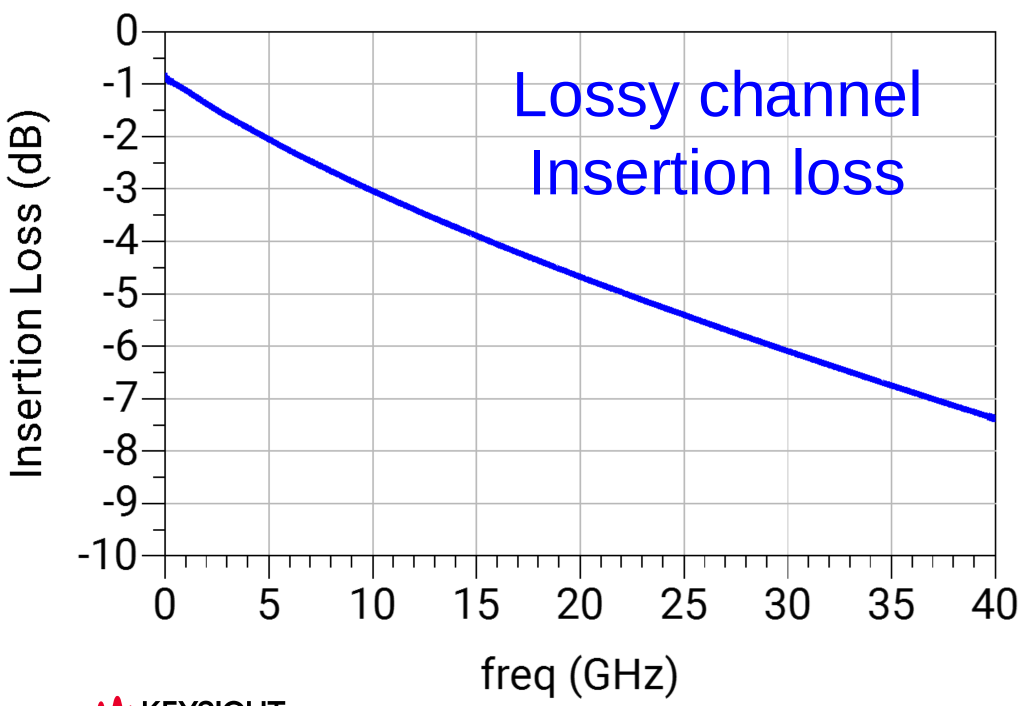


This low-pass filter degrades the fast rise time.

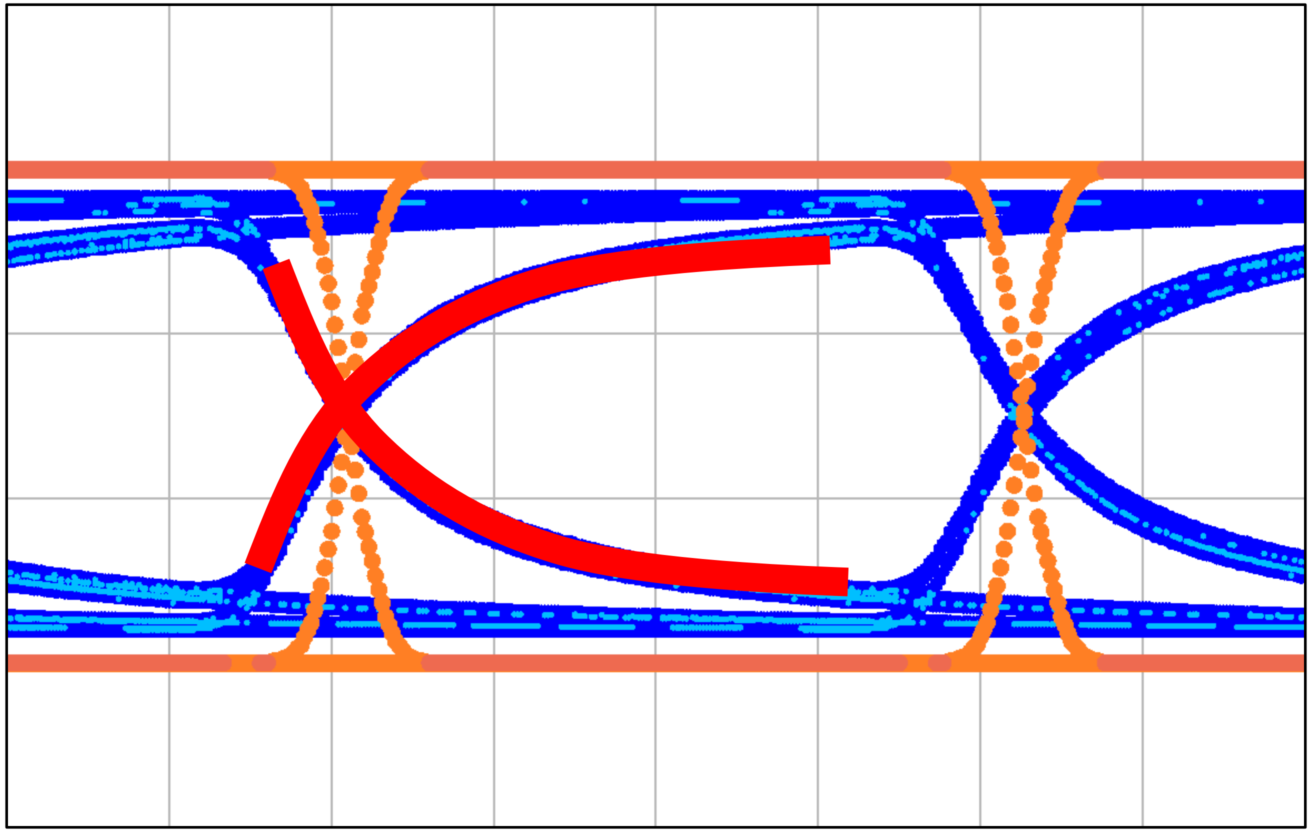
Interconnects Attenuate High-frequency Components More

Received waveform after a lossy channel



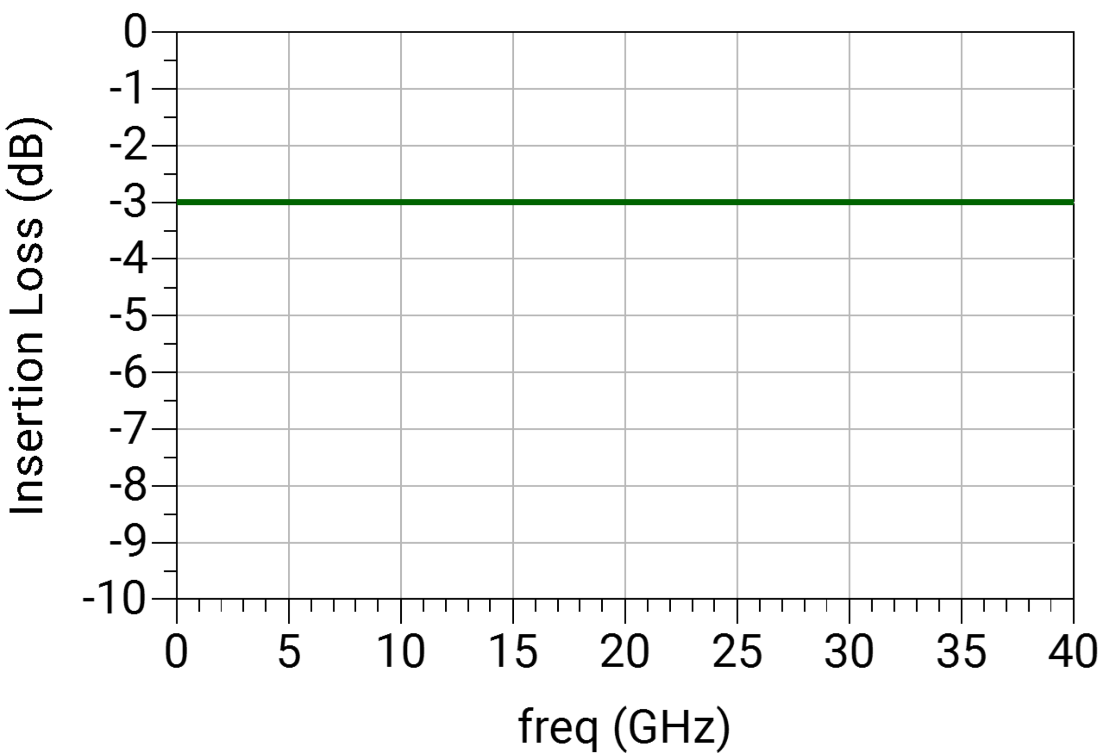


Frequency-dependent loss reduces eye height and width

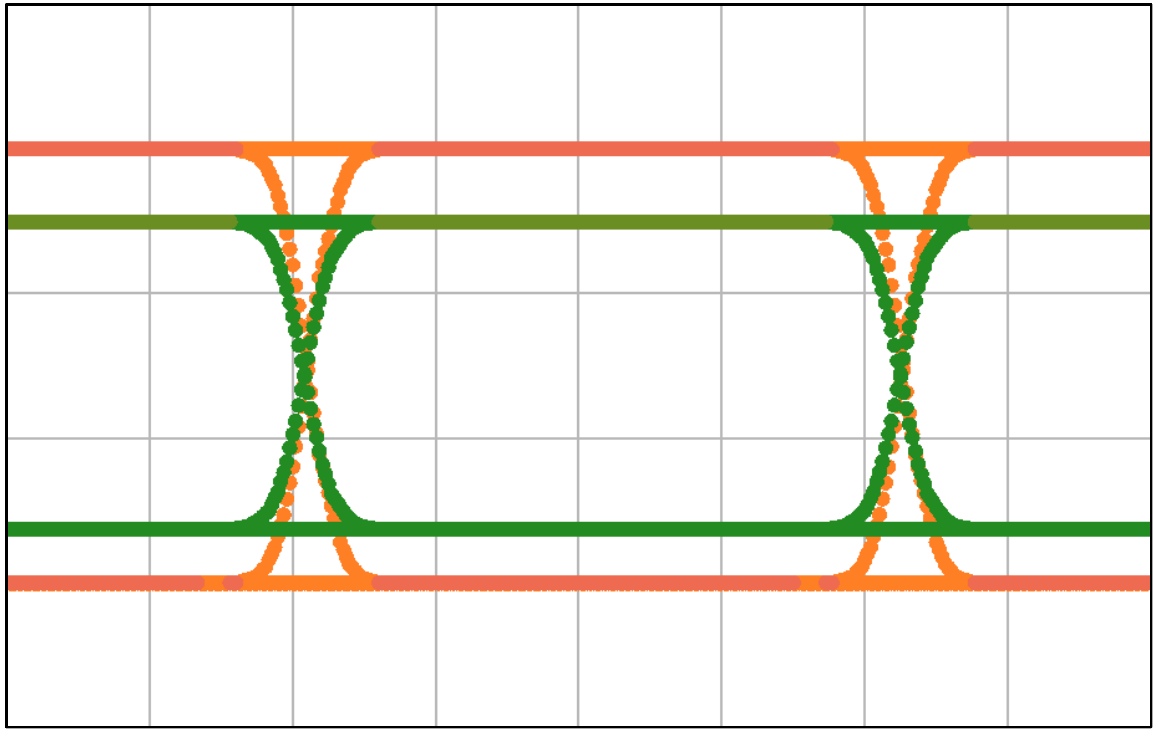


Constant Loss Over Frequency Only Reduces Eye Amplitude

Lossy channel with constant Insertion loss

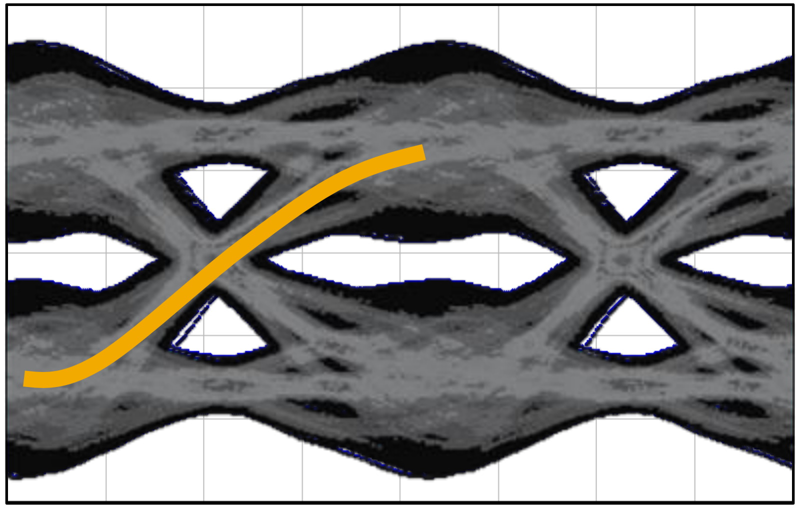


Frequency-independent loss does not degrade rise time

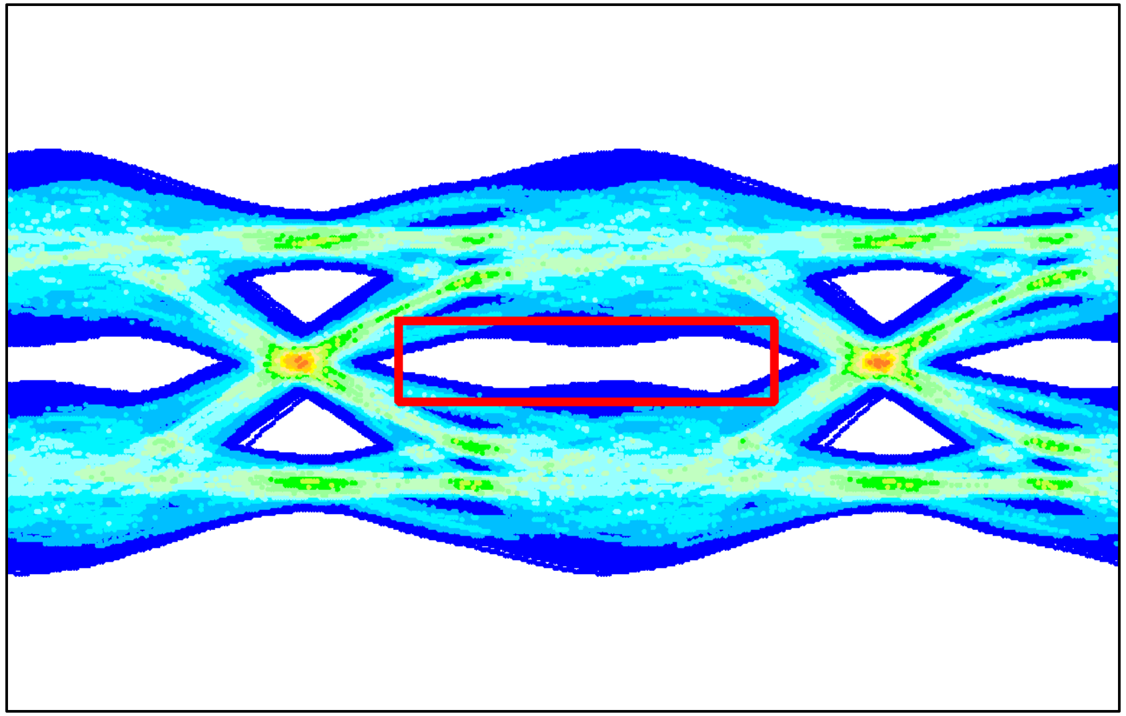


Reduces Loss by Reducing Channel Length

Received eye at RxData7 without equalization



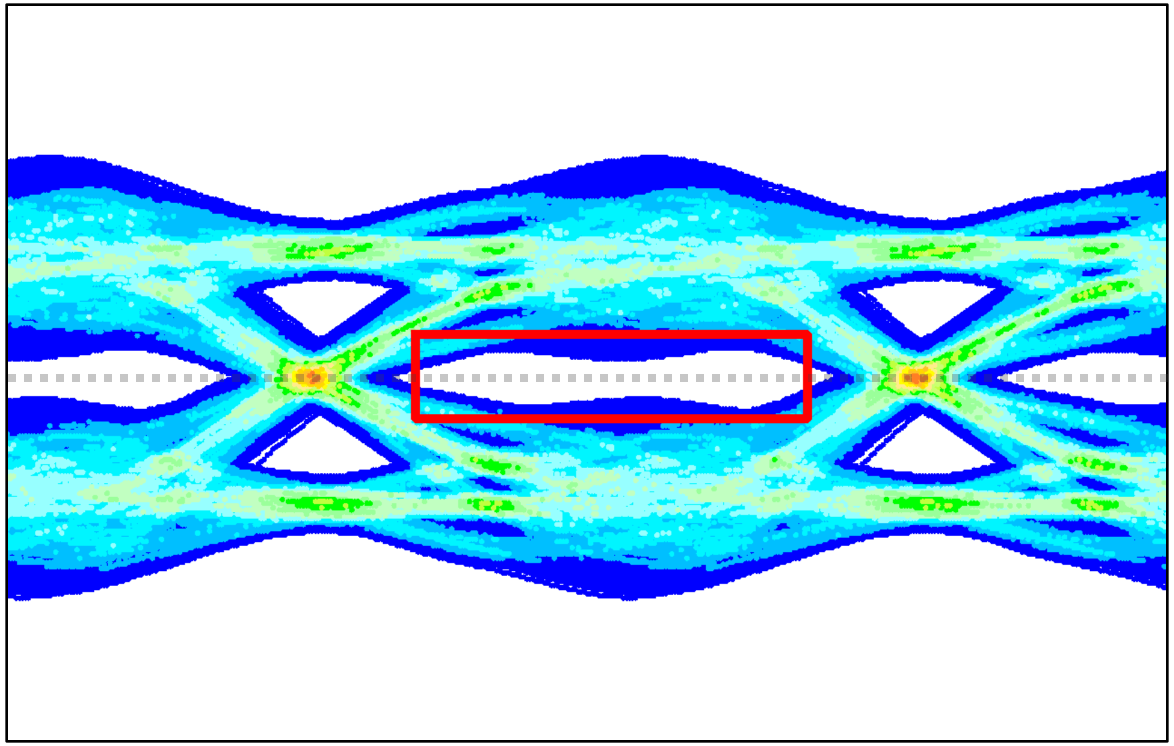
Use an eye mask as a reference as the channel length reduces



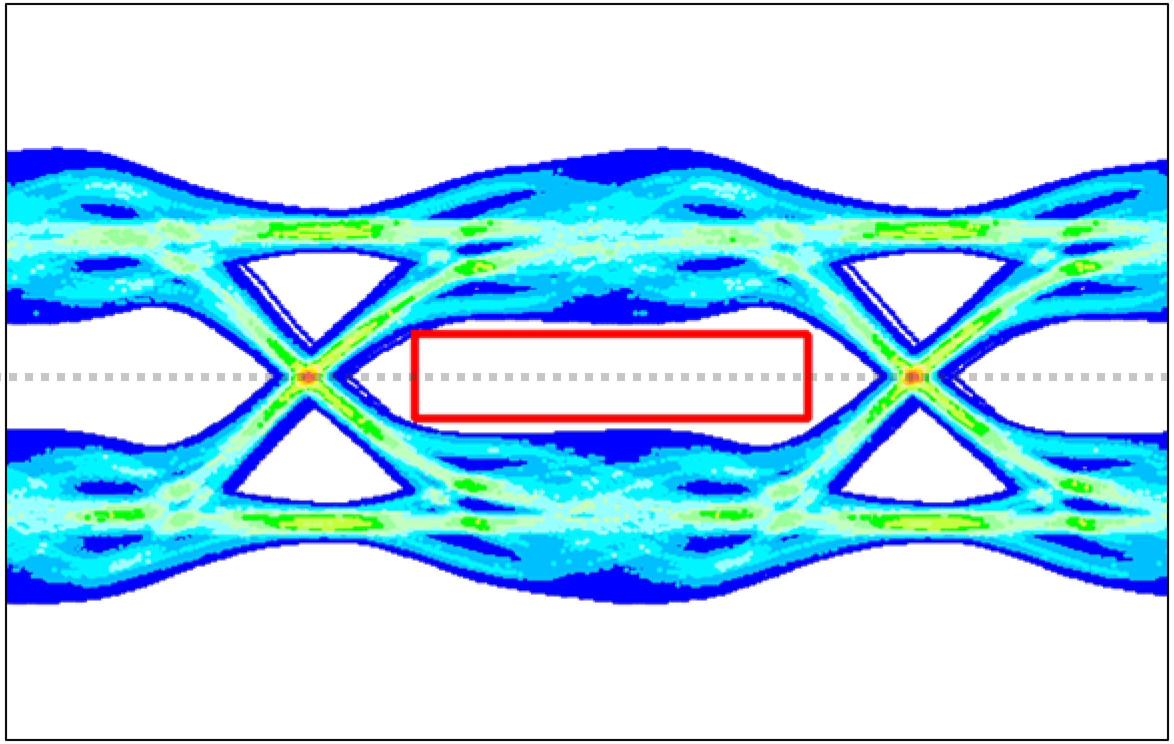
Expect a larger eye-opening as channel length decreases.

Eye Opens Up as Channel Length Decreases

Channel length 25 mm



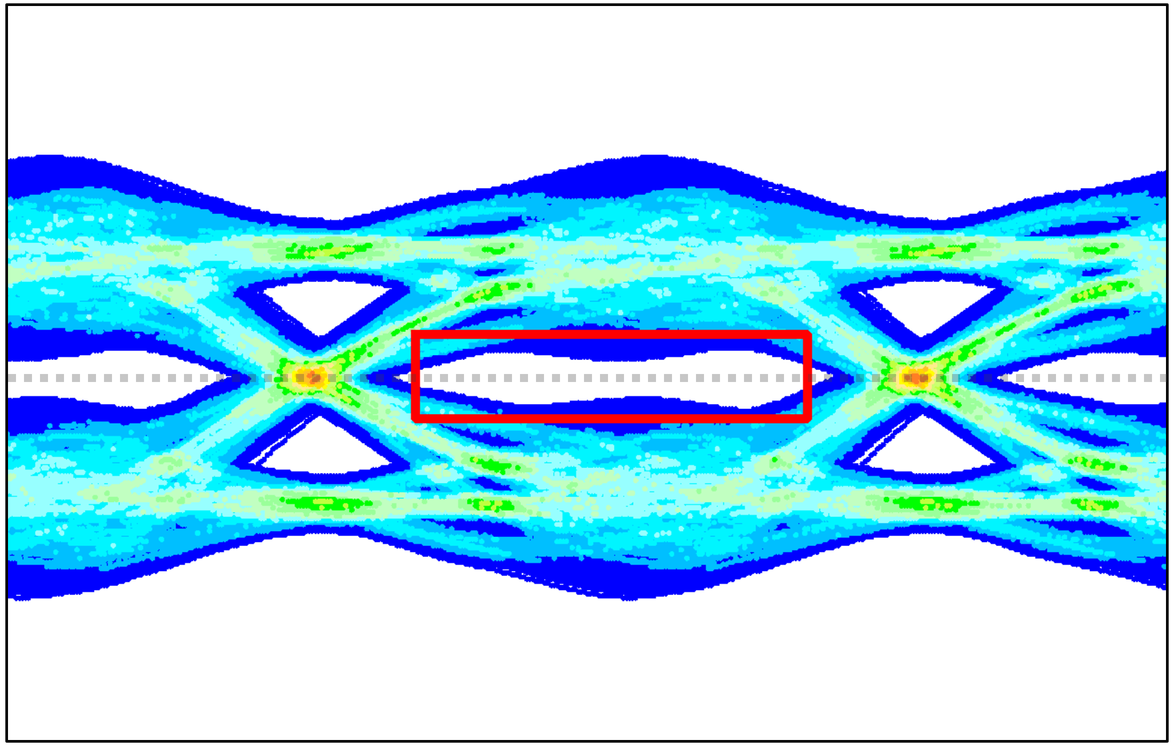
Channel length 18 mm



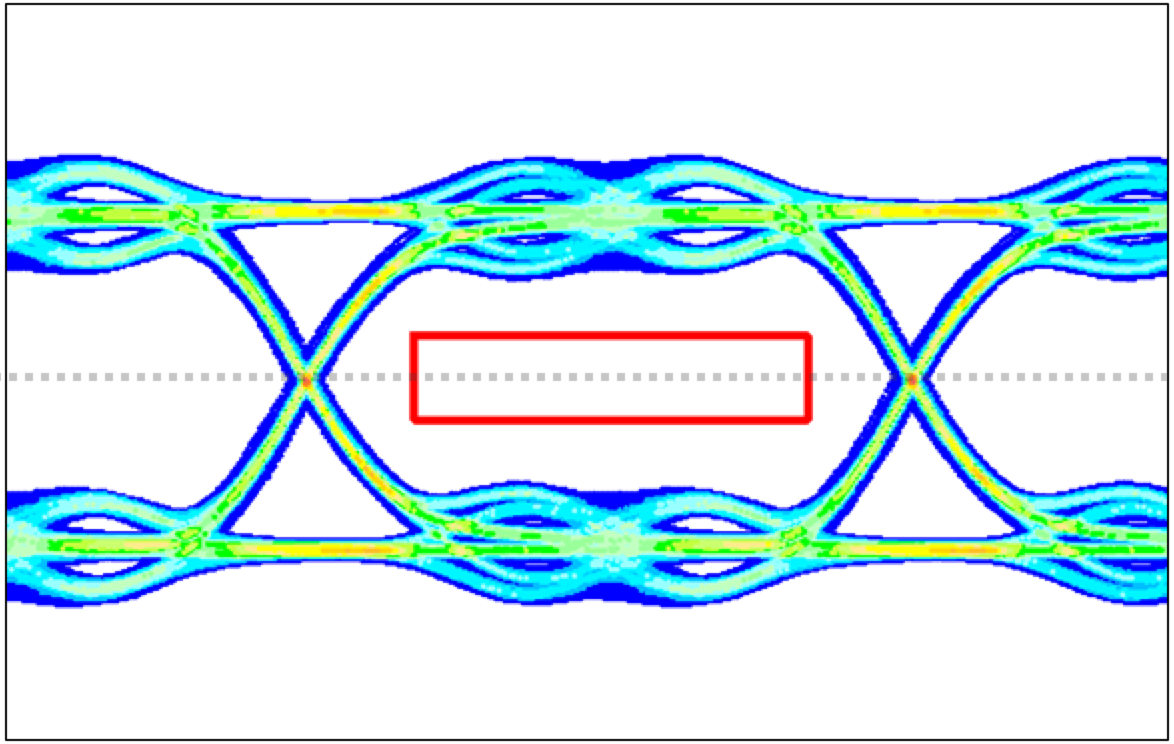
KEYSIGHT

Eye Opens Up as Channel Length Decreases

Channel length 25 mm

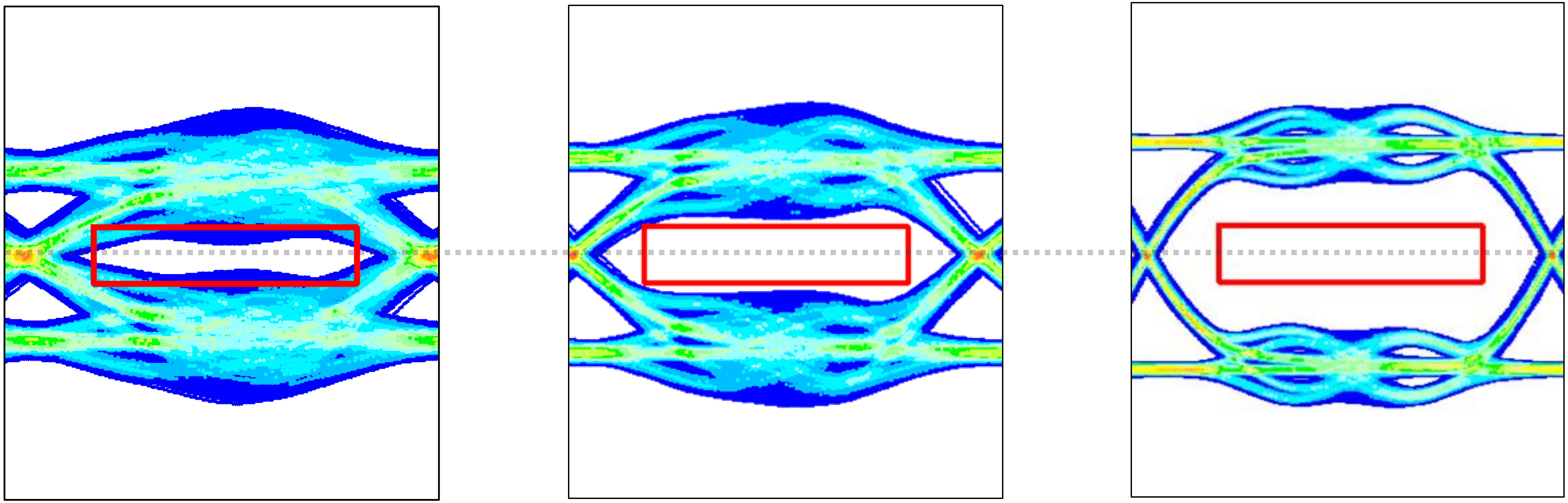


Channel length 10 mm



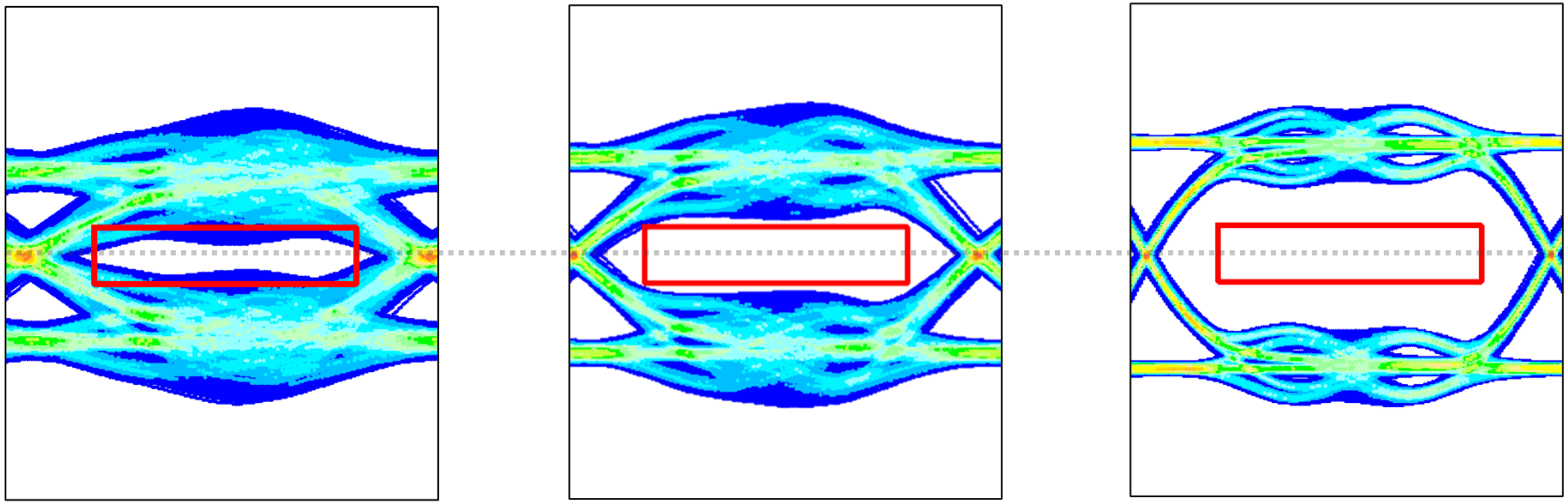
Eye Opens Up as Channel Length Decreases

Channel length 25 mm　　Channel length 18 mm　　Channel length 10 mm



As expected, one achieves a larger eye-opening as channel length decreases.

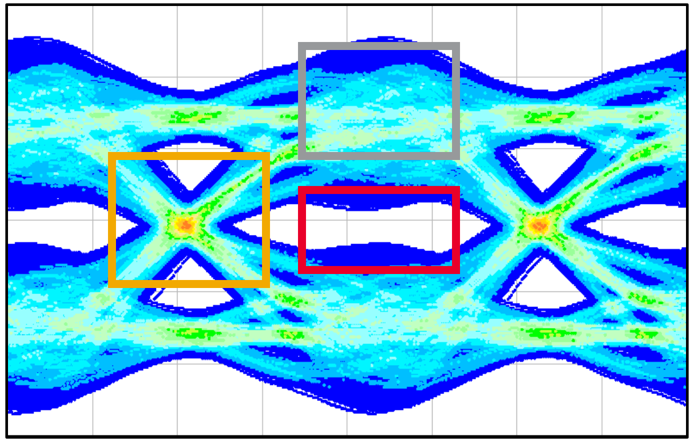
Fix Rise Time Degradation by Decreasing Channel Length



Channel length 25 mm | Channel length 18 mm | Channel length 10 mm

Signs in the Eye	Root cause	Fixes
• The transition edge slope is slow/gradual	Frequency-dependent loss from the channel	• Reduce channel length to reduce loss

Improve Your Signal Integrity by Removing the Root Cause



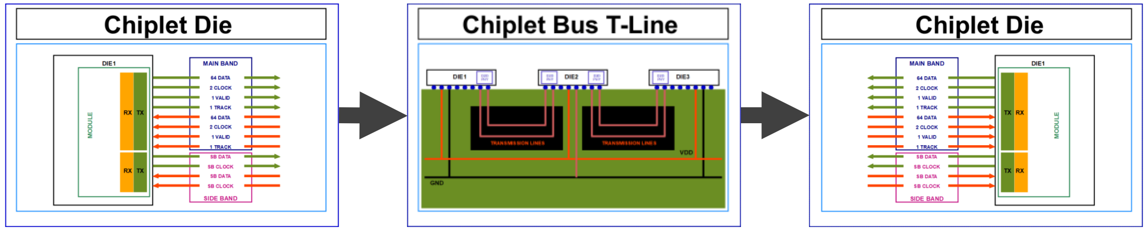
1. Signs of reflection
2. Signs of crosstalk
3. Signs of frequency-dependent loss

Signs in the Eye	Root cause	Fixes
• Deformed eye shape • Reduced eye amplitude	Impedance discontinuities	• Locate impedance discontinuity and match it with channel impedance
• Peaks in eye transitions • Lumped peaks in the eyes	Crosstalk from adjacent channels	• Move channels farther apart • Maintain the same channel length
• The transition edge slope is slow/gradual	Frequency-dependent loss from the channel	• Reduce channel length to reduce loss

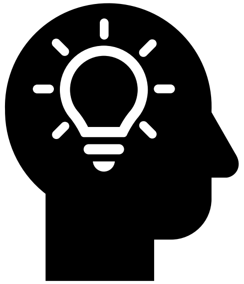
KEYSIGHT

Key Attributes to a Chiplet System SI Analysis Software

Standard-focused
Let the software work for you



Die-to-Die Link and System Analysis
Identify problems early, reproduce existing problems

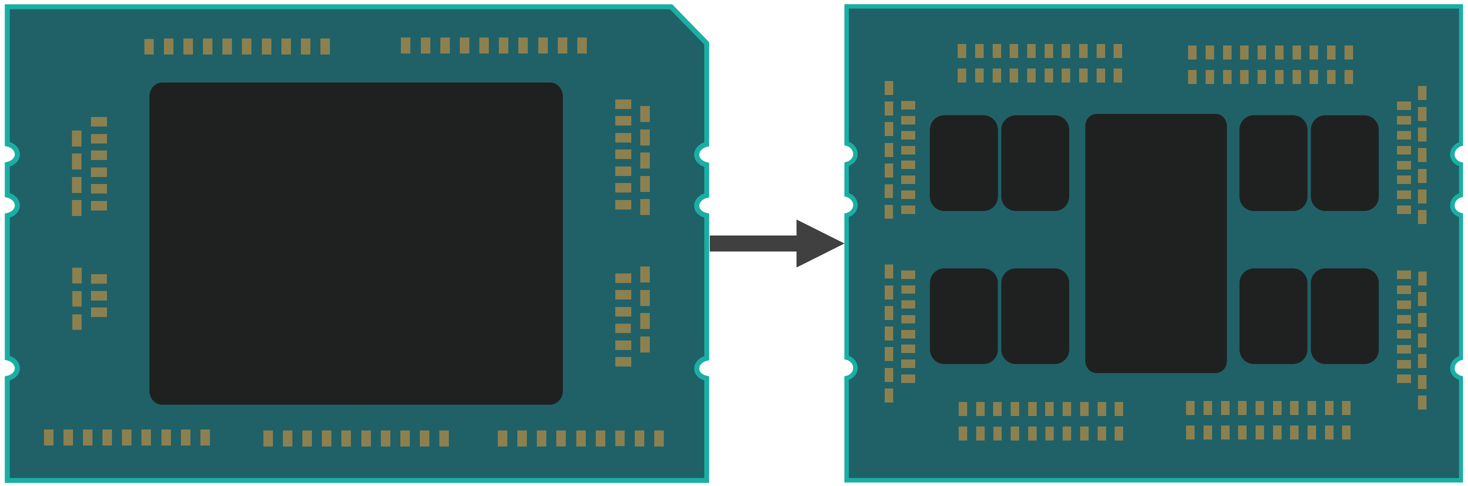


Usability and Integration
Don’t work for the computer

Chiplet PHY Designer Demo

Chiplet and UCIe Standard Quick Recap

Monolithic Die Designs **Chiplet Designs**



Chiplet Design Philosophy

- Maximizes wafer usage
- Has a higher yield
- Has a lower cost
- Easy to scale!

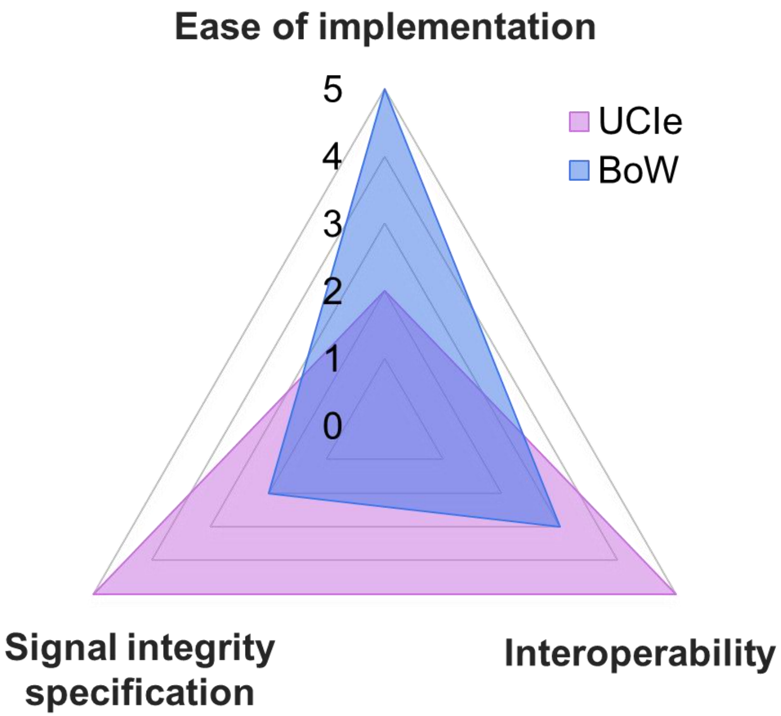
Die-to-die (D2D) communication is important

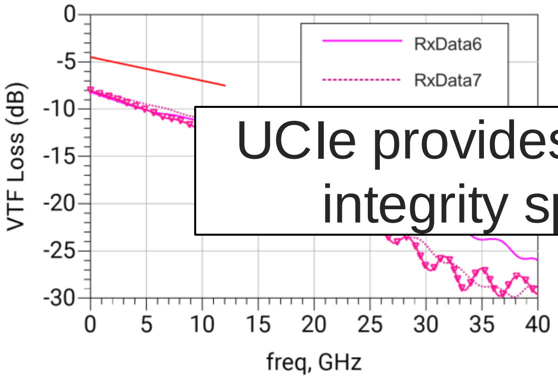
BoW OPEN Compute Project

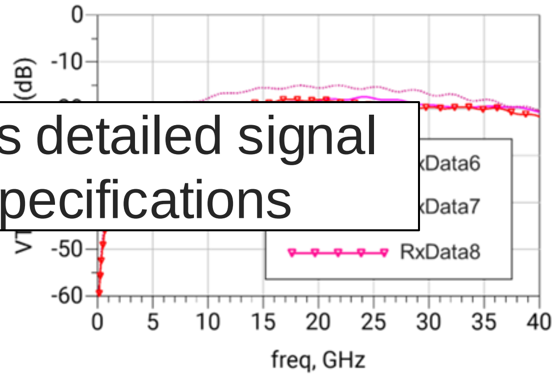
Standards to facilitate the adoption

UCIe™ Universal Chiplet Interconnect Express

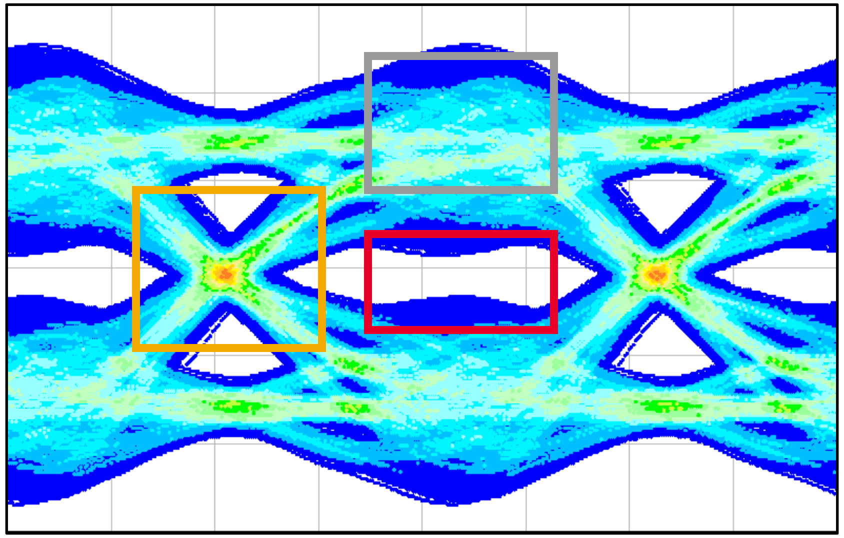
UCIe vs. BoW and Signal Integrity Insight Completed!







UCIe provides detailed signal integrity specifications



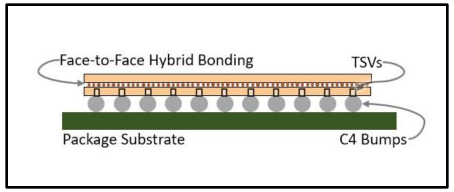
Rule #9

1. Signs of reflection
2. Signs of crosstalk
3. Signs of frequency-dependent loss

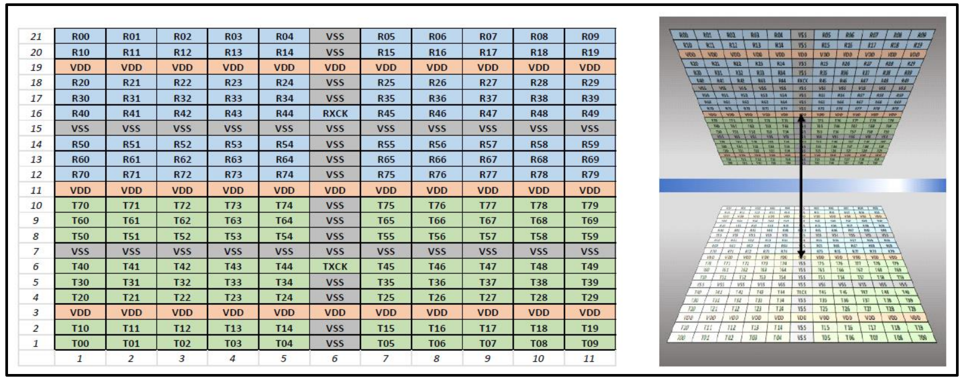
KEYSIGHT

Future Direction of UCIe and BoW

UCIe 2.0: Higher performance



Example of 3D die stacking [2]



21	R00	R01	R02	R03	R04	VSS	R05	R06	R07	R08	R09
20	R10	R11	R12	R13	R14	VSS	R15	R16	R17	R18	R19
19	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
18	R20	R21	R22	R23	R24	VSS	R25	R26	R27	R28	R29
17	R30	R31	R32	R33	R34	VSS	R35	R36	R37	R38	R39
16	R40	R41	R42	R43	R44	RXCK	R45	R46	R47	R48	R49
15	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
14	R50	R51	R52	R53	R54	VSS	R55	R56	R57	R58	R59
13	R60	R61	R62	R63	R64	VSS	R65	R66	R67	R68	R69
12	R70	R71	R72	R73	R74	VSS	R75	R76	R77	R78	R79
11	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
10	T70	T71	T72	T73	T74	VSS	T75	T76	T77	T78	T79
9	T60	T61	T62	T63	T64	VSS	T65	T66	T67	T68	T69
8	T50	T51	T52	T53	T54	VSS	T55	T56	T57	T58	T59
7	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
6	T40	T41	T42	T43	T44	TXCK	T45	T46	T47	T48	T49
5	T30	T31	T32	T33	T34	VSS	T35	T36	T37	T38	T39
4	T20	T21	T22	T23	T24	VSS	T25	T26	T27	T28	T29
3	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
2	T10	T11	T12	T13	T14	VSS	T15	T16	T17	T18	T19
1	T00	T01	T02	T03	T04	VSS	T05	T06	T07	T08	T09
	1	2	3	4	5	6	7	8	9	10	11

UCIe-3D Module Bump Map [2]

BoW 2.1: Broader applications space

BoW.Optical

Provide a common set of recommended configurations for optical chiplets [5].

BoW.Memory

Allow dynamic bidirectional and mixed-direction slices for memory and DRAM chiplets [5].

BoW.FlexI

Offer a single data-rate, streamlined PHY for cost-sensitive and/or ultra-wide applications [5].

Why You Should Design UCIe Systems with Keysight W3650B

Standard-focused and Compliance

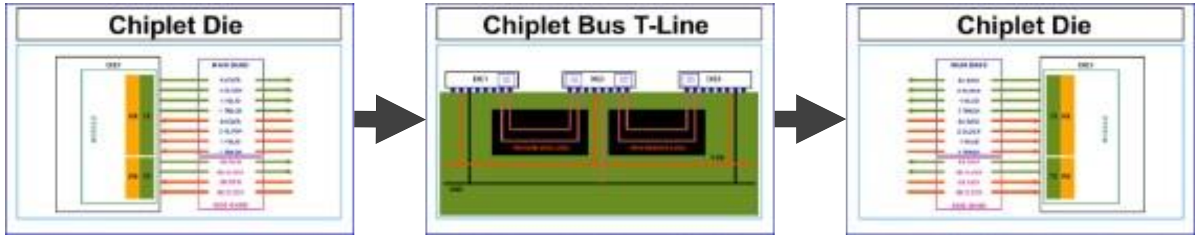
Improve productivity, ensure interoperability

UCIe™ Universal Chiplet Interconnect Express

BoW OPEN Compute Project

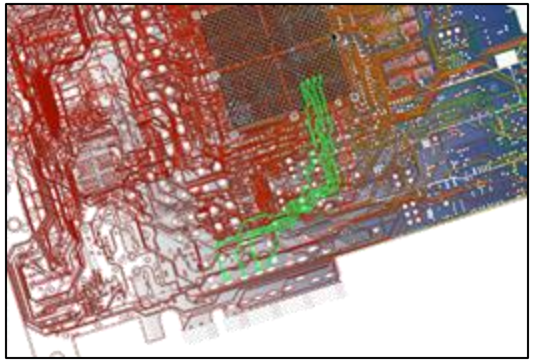
End-to-end UCIe System Analysis

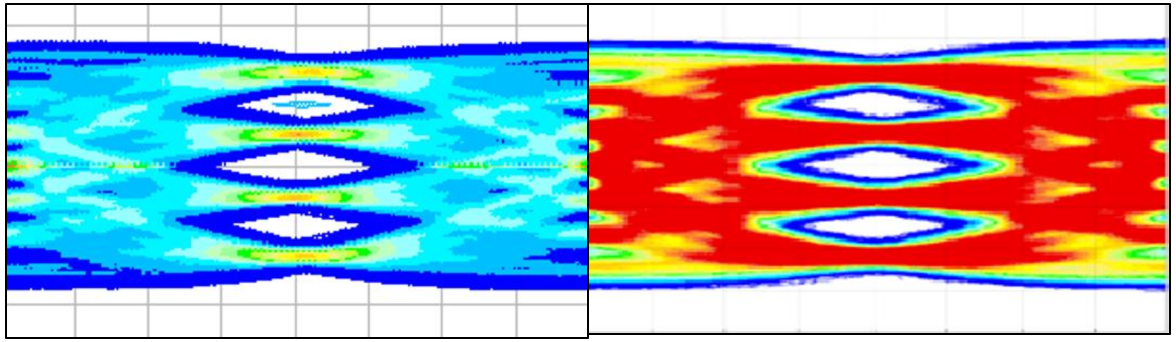
Identify system level issues, optimize performance



Simulation and Measurement Solutions

Enable practical design validation, secure first-pass design success





Simulate your UCIe system with ADS2025 Update 2

Thank you

References

[1] G. Loh, "An Overview of Chiplet Technology for the AMD EPYC™ and Ryzen™ Processor Families," [Online Video], Available: https://youtu.be/wqRAG_5KzBE.

[2] "Universal Chiplet Interconnect Express (UCIe) Specification," August 6, 2024, Revision 2.0, Version 1.0.

[3] The Open Domain-Specific Architecture BoW Workstream, "Bunch of Wires (BoW) PHY Specification," DRAFT Version 2.0, March 1st, 2023. [Online]. Available: https://www.opencompute.org/documents/bow-specification-v2-0d-1-pdf.

[4] E. Bogatin, "Bogatin's 20 Rules for Engineers," Signal Integrity Journal, [Online]. Available: https://www.signalintegrityjournal.com/blogs/4-eric-bogatin-signal-integrity-journal-technical-editor/post/1539-bogatins-20-rules-for-engineers.

[5] K. Donnelly, K. Johal, and S. Ardalan. "BoW PHY 2 1," *YouTube*, 22 Oct. 2024. [Online]. Available: https://youtu.be/sqd7ea0TP-I.