

Cut Digital Validation from Days to Hours



Speakers



Ben Miller

Product Marketing Manager

Keysight Global Marketing



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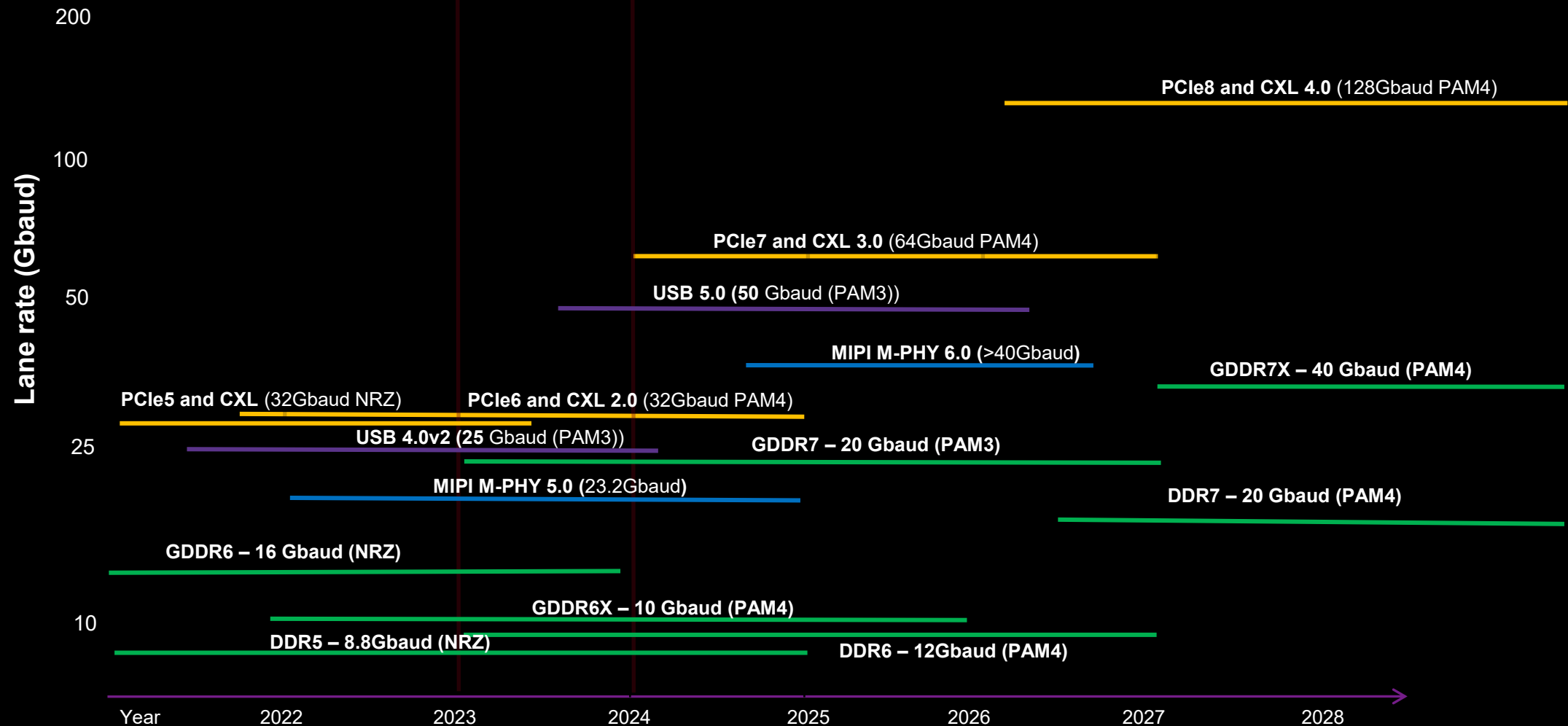
Mike Beyers

Product Planner

Oscilloscopes R&D

High-Speed Digital Standards in 2026

Higher data rates, more complex modulation, shorter lifecycles



Three Bottlenecks of Digital Validation



Long test cycles

Dozen of measurements

Slow analysis

Repeated testing

Manual calibration



Tight noise margins

Smaller thresholds

Limited margin

Scope noise

Low resolution



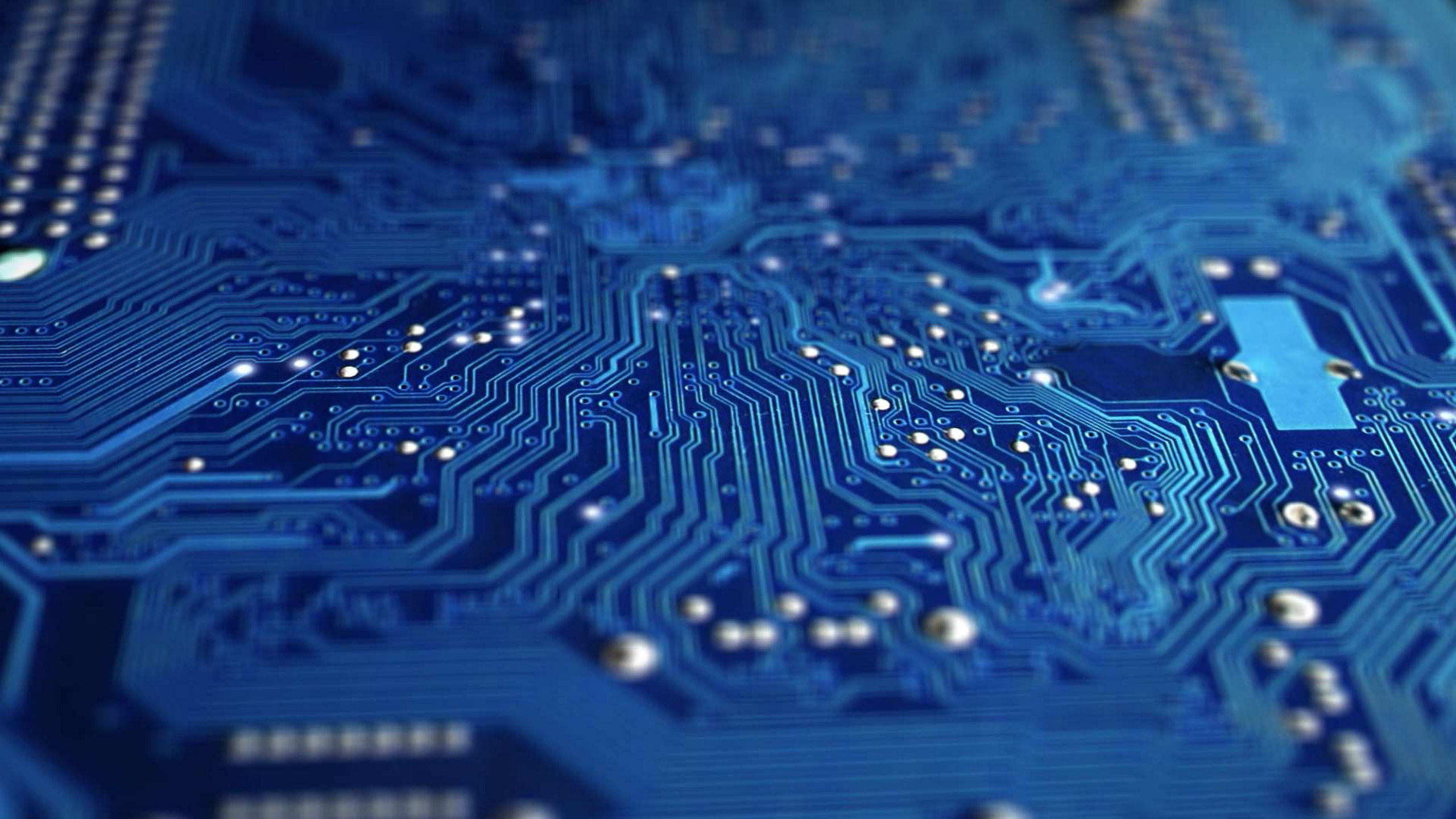
Lab constraints

Large footprint

Limited mobility

High power consumption

Loud ambient noise



Keysight XR8 | Turn Days of Digital Validation Into Hours



Faster Analysis

Multicore processing

Improved firmware

Enhanced visualization

Custom SCPI automation



Clearer Insights

12-bit ADC

Ultra-low noise

Up to 8 Gpts memory

15.6" screen



Better Fit

Reduced size

Lighter weight

Power efficient

Quieter

XR8 Application Software at Launch

Signal Analysis

Advanced signal integrity

Jitter, vertical, and phase noise

Pulse amplitude modulation analysis

Measurement server software

Compliance Automation

USB3 / 4 / 4v2

DDR5 / LPDDR5

DisplayPort 2.1

MIPI D-PHY

With many more to come...



Keysight High-Performance Oscilloscope Portfolio

New XR8 increases processing speed and signal integrity up to 33 GHz

Expert



Pro



Model	MXR Series	XR8	UXR Series
Bandwidth	500 MHz to 6 GHz	8 GHz to 33 GHz	10 GHz to 110 GHz
Analog channels	4 to 8	4	2 to 4
Max sample rate	16 GSa/s	128 GSa/s	128 GSa/s to 256 GSa/s
Max memory depth	1.6 Gpts	8 Gpts	2 Gpts
ADC resolution	10 bits	12 bits	10 bits
Display size	15.6 inch	15.6 inch	15.4 inch
Applications	Power and signal integrity, digital debugging	High-speed digital standards development, compliance	Data center interface development, advanced R&D

USB, DP, & DDR Were **Meant** to Be Tested With The XR8 Oscilloscope



USB4



USB4 Technology and Industry Overview

USB4 was announced by USB-IF in March 2019 and it was released September 2019

- The short timeline was achieved as it is based on the released Thunderbolt 3 protocol.
- It uses the Type-C connector and supports two 20 Gb/s PHY lanes bonded into one logical 40 Gb/s link.

The Compliance Test Specification (CTS) is available but future updates to test methodology are expected

- There will be only one spec, one electrical CTS for USB4/TBT4/TBT3.
- Numerous USB4 products shipping and available on the market. 5G adoption driving new devices.

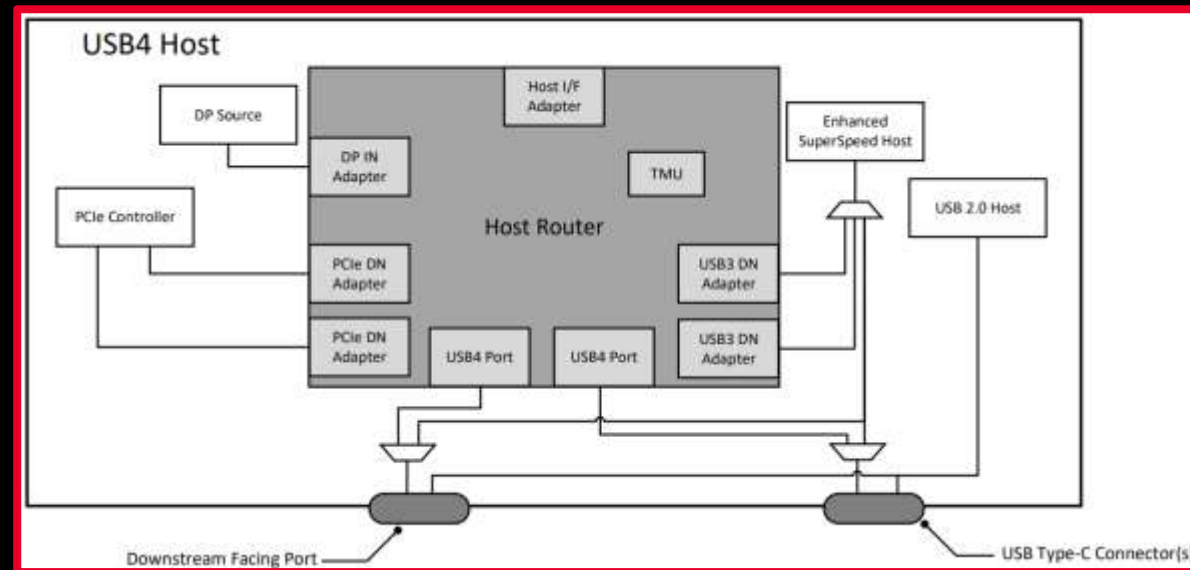
USB4 Customer Challenge

Backwards compatibility:

- USB 2.0, USB 3.2 5G / 10G, USB4 10G / 20G
- DisplayPort 1.4, 2.0 HBR / UHBR 10G / 13.5G / 20G
- TBT 10.3125G/20.625G

Challenge:

- Same port, multiple standards,
- Similar/multiple speeds, different loss budgets, short/long channel.
- Must test for USB4 with and without retimers.



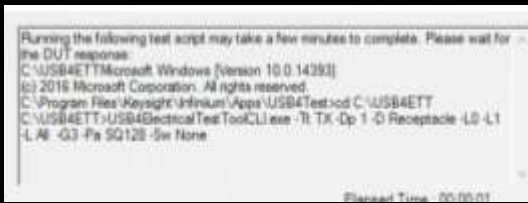
Customers: Silicon, IP, Host, Device, Display, Dock, Hub, External GPU

USB4 Electrical Transmitter Test

USB4 Transmitter Test Software with Integrated SigTest

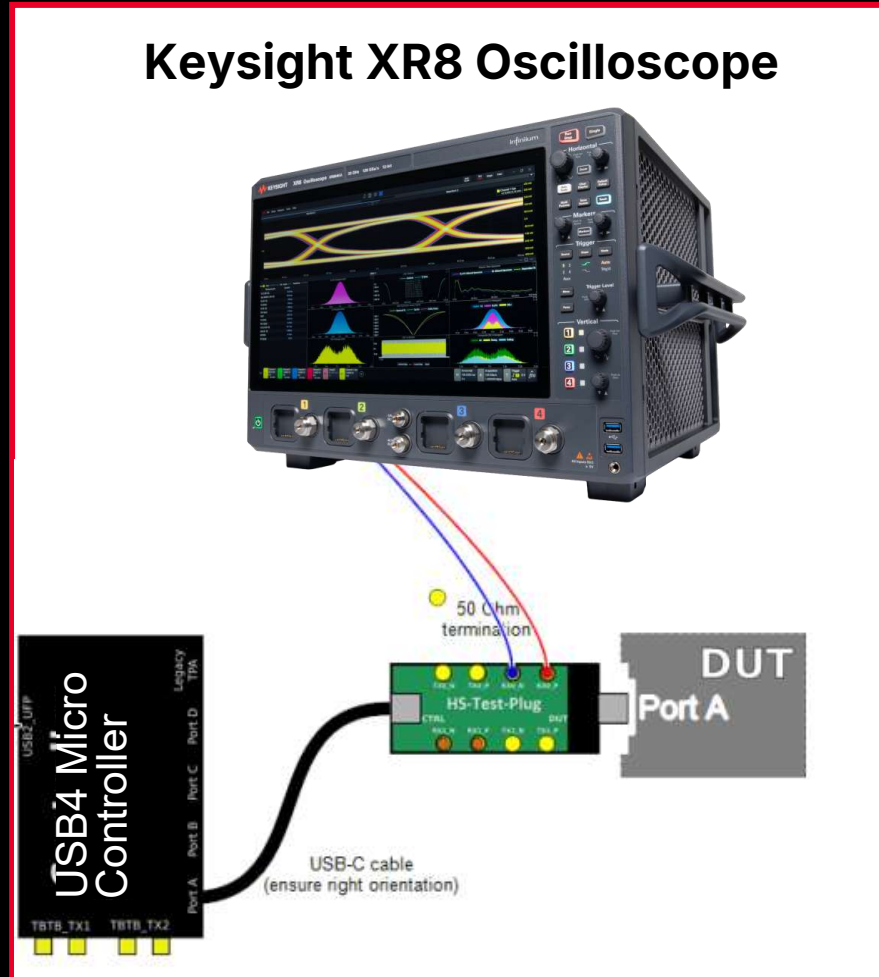


USB4ETT



Control data rate, Tx EQ preset and test pattern with USB4 Controller

Keysight XR8 Oscilloscope



Example: USB4 Test Pattern Changes

Rise/Fall Time: SQ128 (64 bit "1", 64 bit "0")










Eye Diagram Test: PRBS31



DisplayPort 2.1b



Keysight DisplayPort Solutions

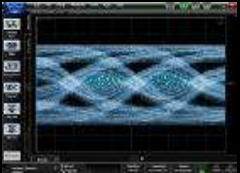
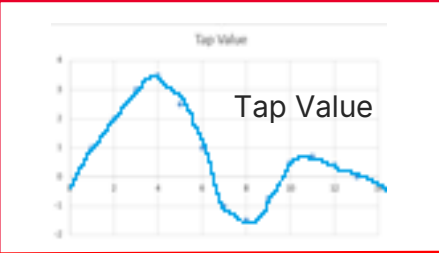
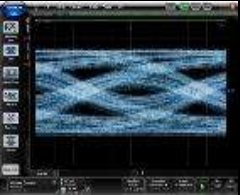
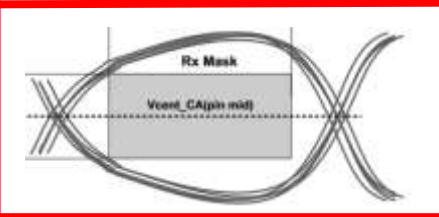

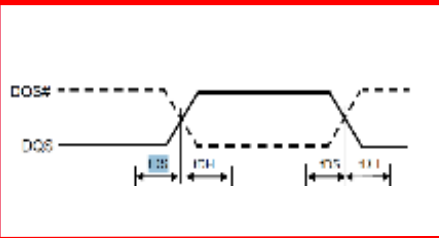
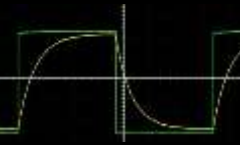
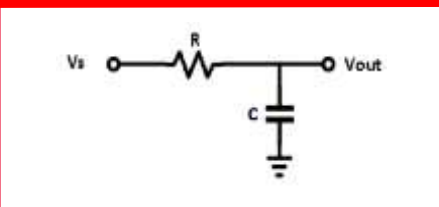
	Source	Sink
<p>Test Automation Software</p>	 <p>Automated Tx tests Debug & characterization Automation via AUX channel</p>	
<p>Instruments</p>	 <p>XR8 Oscilloscope Low noise Fast, accurate measurements Channel embedding & de-embedding CDR, equalization, eye/jitter analysis</p>	 <p>M8050A BERT Best signal integrity Lowest noise Equalization, RJ, PJ, CMI Test patterns</p>
<p>Accessories</p>	 <p>UCD-323 Gen2 Reference Sink/Source</p>  <p>DPR-100 Reference Sink</p>	 <p>UCD-323 Gen2 Reference Sink/Source</p>  <p>DPT-200 Reference Source</p>

DDR5 / LPDDR5



How Did We Get to DDR5?

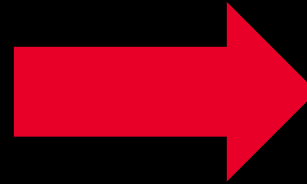
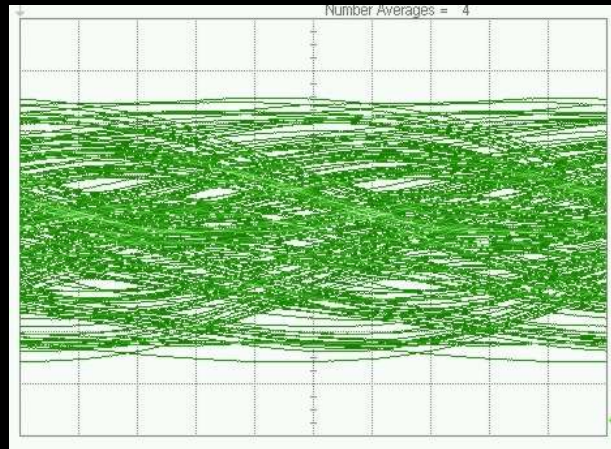
A road paved by innovation

Signal	MT/s	Generation	Characteristics	Specification	Introduction
	4200 – 8000+	DDR5+	<p>"Hyper Speed"</p> <ul style="list-style-type: none"> • Eye collapses • Impulse response • BER Rj/Dj, Rn/Dn 		2019
	1600 – 4200	DDR4	<p>"Serial Speed"</p> <ul style="list-style-type: none"> • Eye Diagrams • Rx Masks • Bit error rates 		2014
	200 – 1600	DDR/2/3	<p>"High Speed Digital"</p> <ul style="list-style-type: none"> • Transmission lines • Ts / Th, Skew 		2002
	33 – 133	SDRAM	<p>"Low Speed"</p> <ul style="list-style-type: none"> • Fanout • Capacitance 		1961

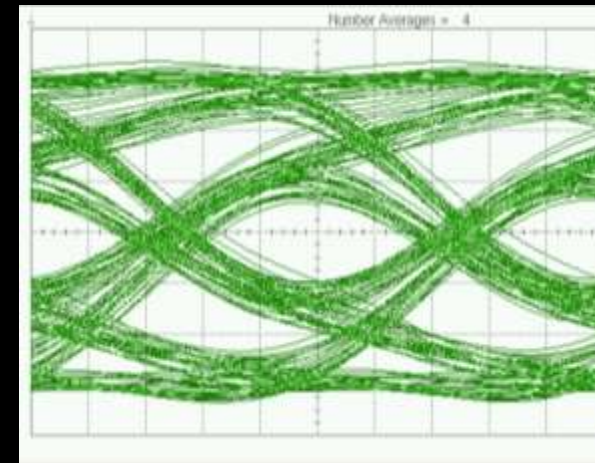
DDR5 Eyes

Equalization

Closed eye



Open eye



A whole new game for memory

LPDDR5 Tx Design Test and Validation

Challenges and Solutions

CHALLENGES



Signal integrity



Ensure interoperability



Time-to-market pressure



SOLUTIONS

Higher bandwidth / low-noise scope and probes

LPDDR5 test parameters

Automated characterization and compliance software

Debug tools

Data analytics tools

Analysis and Debug

Compliance

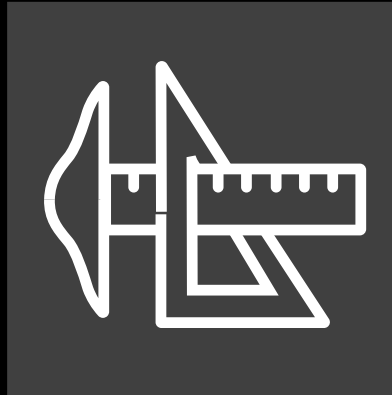
Data Analytics

The **XR8** is

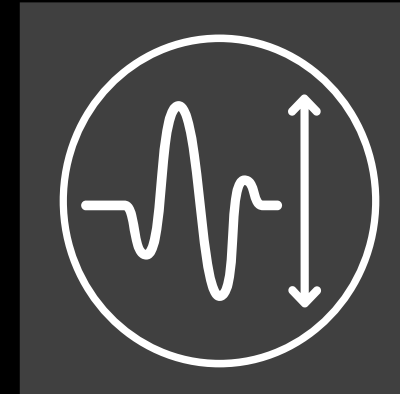
Smarter.



Smaller.



Superior.



Smarter Software. Smaller Size. Superior Signal Integrity.

Keysight XR8 Oscilloscope

Digital Validation. Faster.

Unmatched Signal Integrity

- New 12-bit ADC
- Ultra-low noise
- Leading ENOB performance

Next-Generation Software Platform

- Leading measurement science
- **Multi-Core** CPU processing
- Modern user experience

Smarter, Leaner Hardware Design

- 30% less depth
- 1/3 less power
- 4x quieter
- Improved reliability

Future-Ready Technology

- Advanced Interconnect
- 12 bits DSP/ADC
- **Low noise** Pre-Amp/Sampler

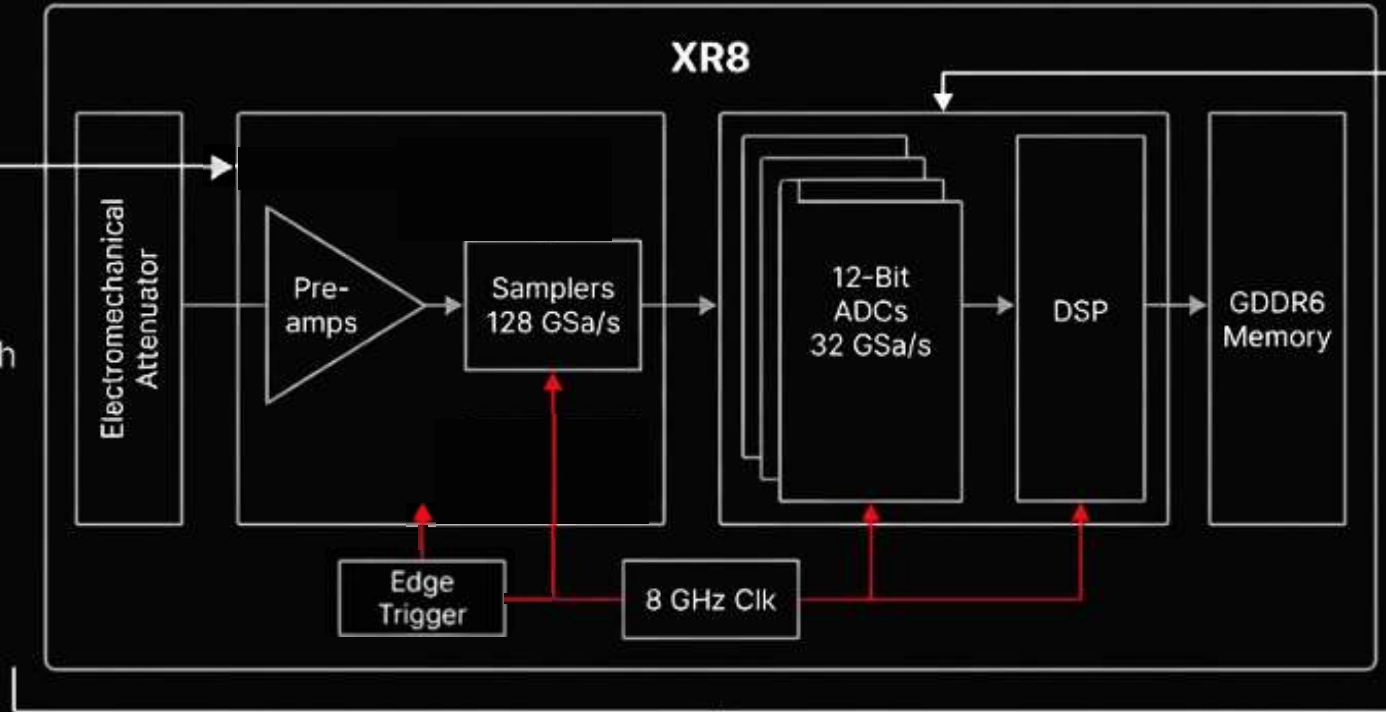


New in XR8 - Hardware

Modern Architecture Built on Three Pillars of Innovation

Pillar 1: The Front-End

Perfecting the Signal Path with a fully integrated front-end ASIC.



Pillar 2: The Digital Core

Multiplying Power and Efficiency with a new, highly integrated digitizer.

Pillar 3: The Mechanical Platform

Enhancing Reliability and Thermal Performance through a redesigned physical architecture.

Acquisition

From the World's Best to What's Next

Single-Chip Integration:

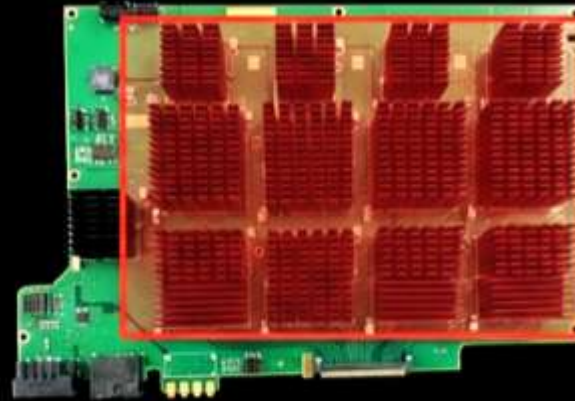
- A newly designed 12-bit ADC incorporating the DSP, memory controller, and buffering functions

Precise Layout:

- Drastically reduced the footprint of the acquisition system

Improved Efficiency:

- Consolidation resulting in lower power consumption and simplified system design

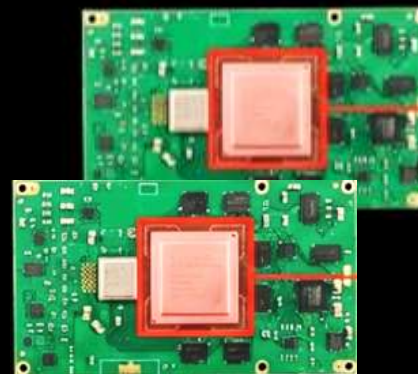


UXR

Twelve Separate ASICs (Six per Channel):

10-bit ADC, DSP, Memory Controller,
Buffering Functions.

This generated substantial heat and
required extensive cooling.



XR8

Single-Chip Integration

Incorporates DSP, memory controller,
and buffering, leading to a drastic
reduction in size and power consumption.

Efficiency in Design

Compact without Compromise

Compact:

- >30% less depth
- >30% lighter

Optimized:

- $\frac{1}{3}$ less power (900W)
- 4X quieter
- Larger, higher-resolution screen

Refined:

- Thermally efficient
- Superior reliability



XR804KA

UXR0334B

New Software Features

Infiniium 2026

Expanded Analysis Capability

- Multicore analysis with full memory access
- 64 available functions (up from 16 previously)

Enhanced Visualization Tools

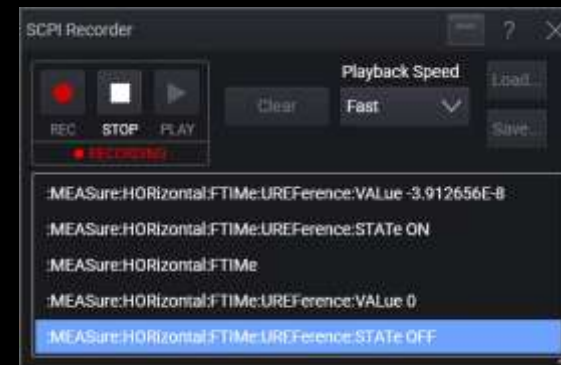
- 4 waveform histograms
- 4 measurement histograms
- 4 jitter analyzers

Advanced Equalization and Automation

- Up to 64 equalizers
- SCPI command recorder
 - 1 to 1 Input/Output simplifies automated workflows

Significant Performance Improvements

- Jitter analysis up to 3× faster
- PAM4 plotting up to 4× faster
- PAM4 SNDR analysis up to 10× faster
- Waveform saving in HDF5 format—up to 40× faster

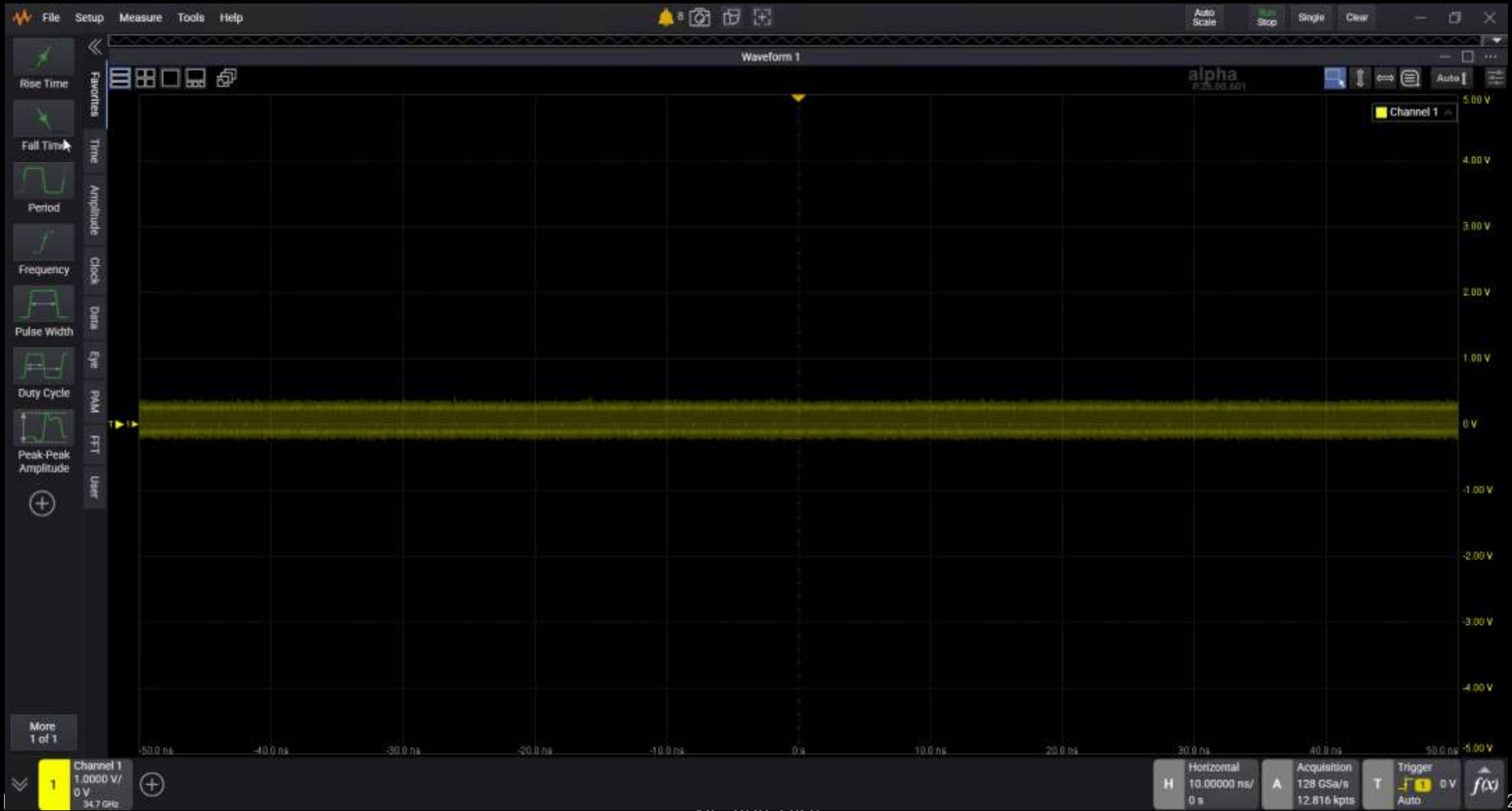


Drag and Drop Functions

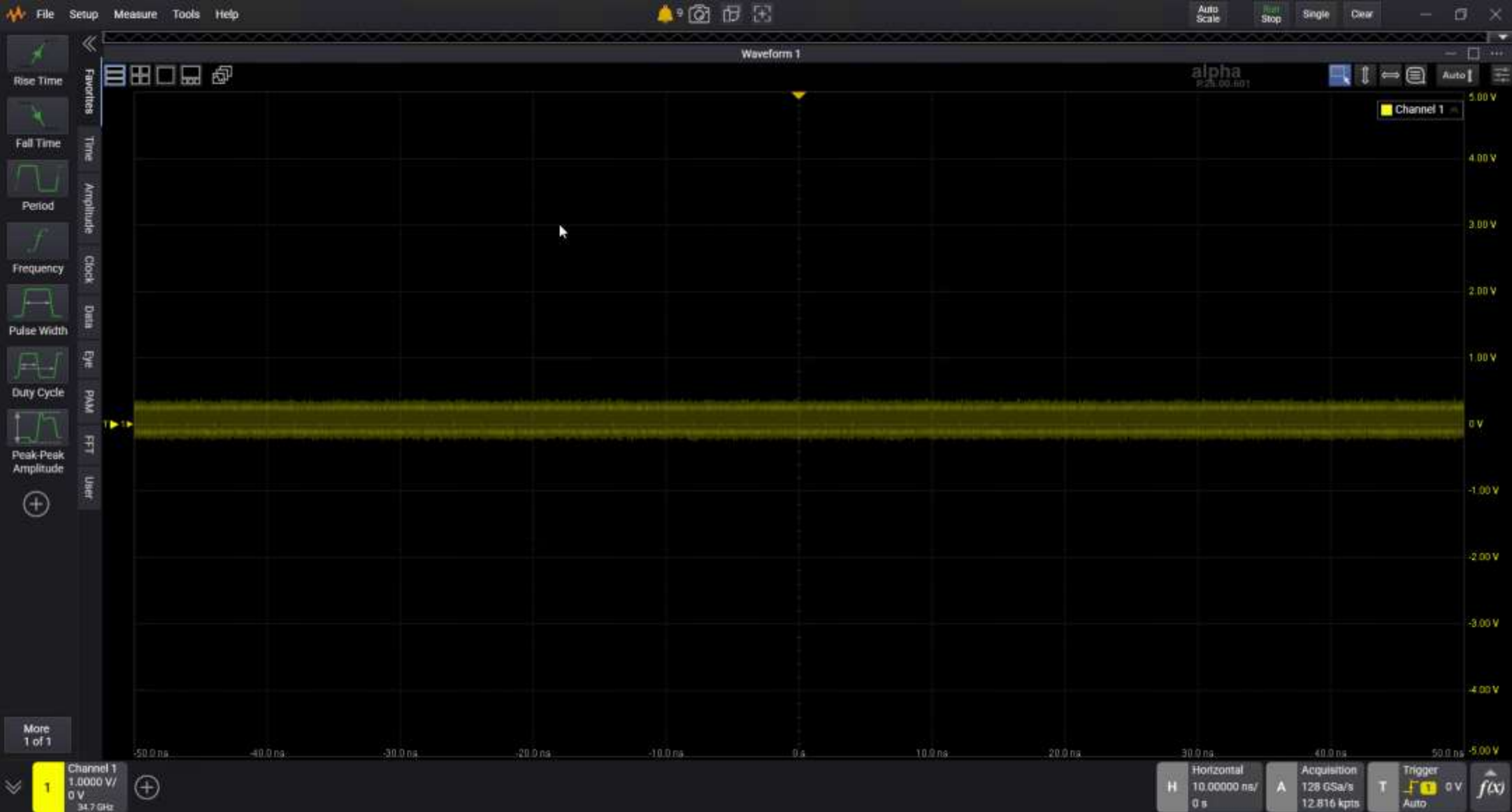


- **64 functions with variety of operations**
- **New functions:**
 - **Equalization (EQ)**
 - **De-embedding**
 - **InfiniiSim**
- **User / Custom Operators by Python, Matlab or XML**

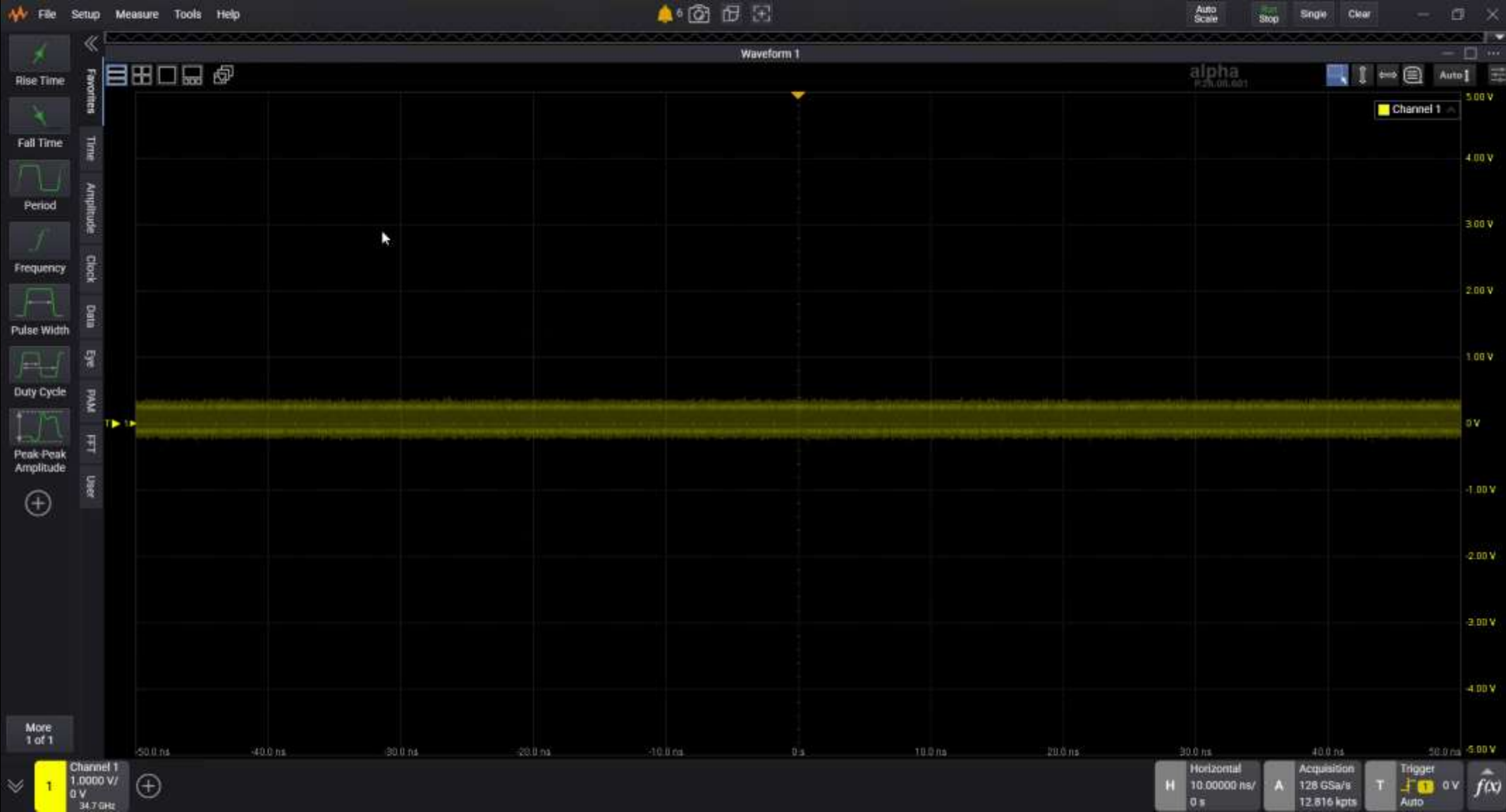
Setup Real-Time Eye Plot



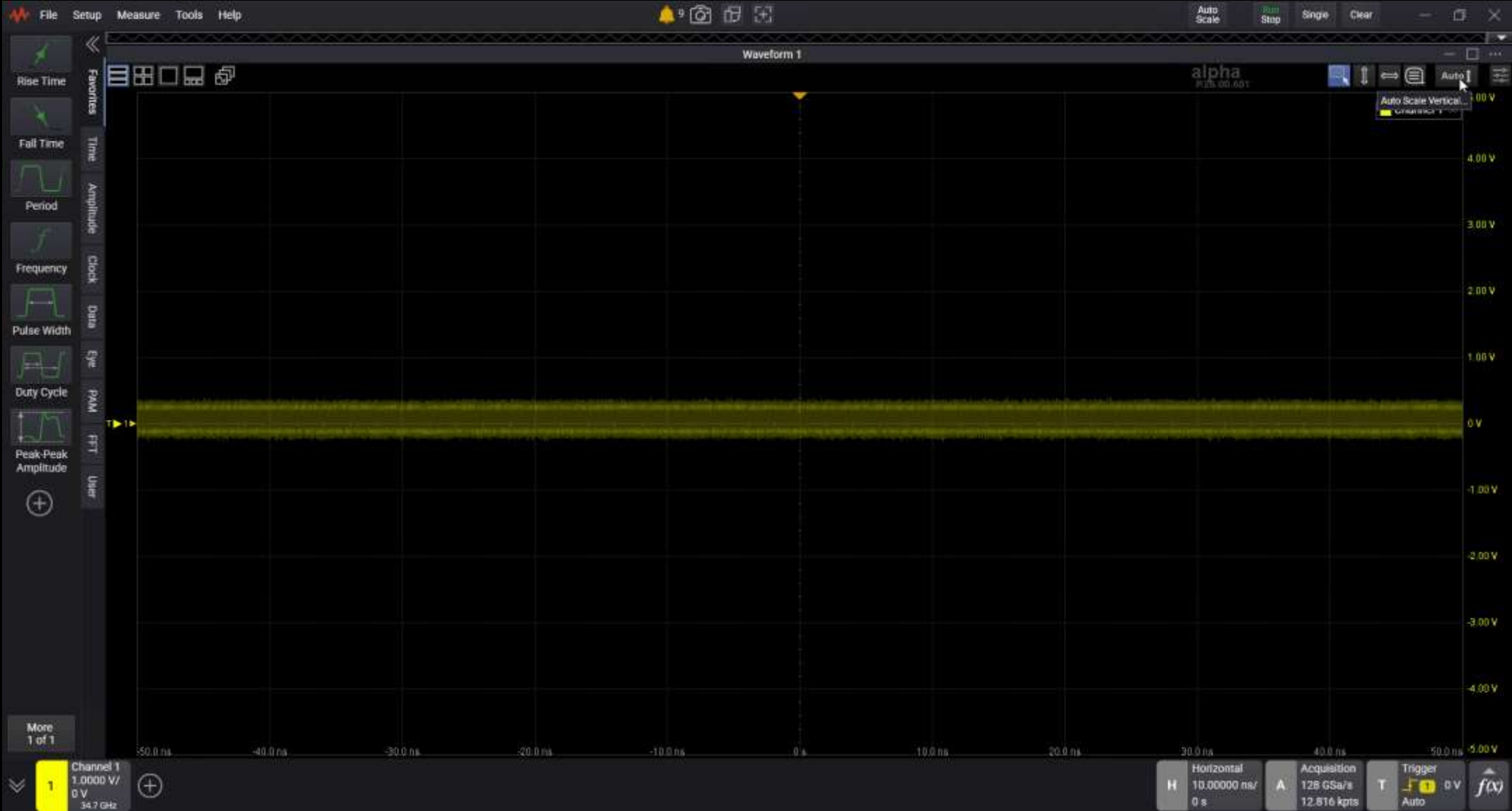
Built-In Waveform Simulation



Superior Analysis for Long Memory Capture

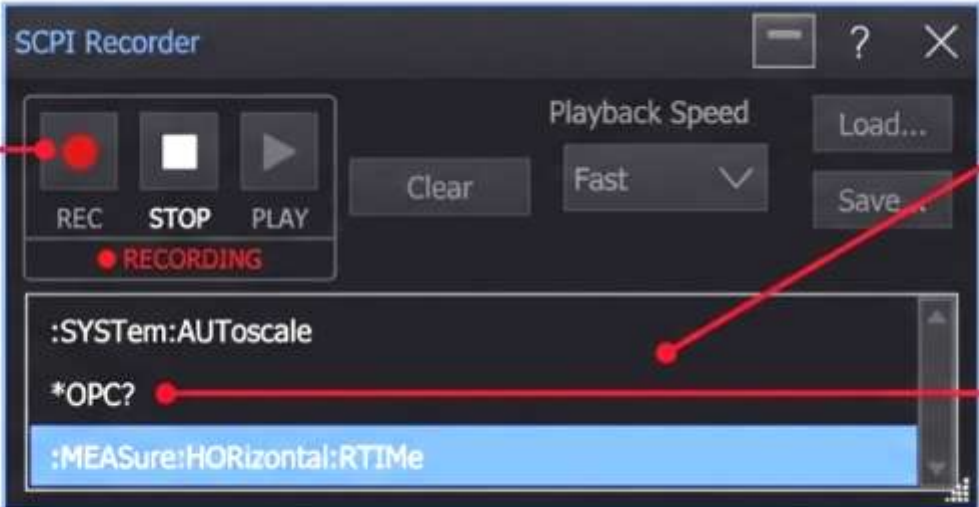


Standard Zone Qualify Trigger



Your Most Powerful Tool: The SCPI Recorder

Stop searching through manuals. Start recording your actions



The screenshot shows the SCPI Recorder application window. At the top left, there are three buttons: REC (with a red dot), STOP (with a white square), and PLAY (with a grey triangle). Below these buttons, a red dot and the word "RECORDING" are visible. To the right of the buttons are "Clear", "Fast" (with a dropdown arrow), "Load...", and "Save..." buttons. The main area of the window is a text box containing the following SCPI commands:
:SYSTem:AUToscale
*OPC?
:MEASure:HORizontal:RTIME
The last command is highlighted in blue. Red arrows point from the text annotations to the REC button and the *OPC? command.

Click **REC** to start.

Perform actions in the GUI... and the exact **SCPI commands** are generated here.

Copy these commands directly into your script. It even adds ***OPC?** for synchronization where needed!

How it works:

- Start recording
- Perform actions/measurements using the scope graphical interface
- The recorder captures all actions and translates them into SCPI commands
- Copy, save for your automation program, or **play back the sequence for repeated operation**

Thank you

www.keysight.com/find/XR8