KEYSIGHT

EDA World Tour

Power Integrity
Design and Simulation

KEYSIGHT

PI Master Class on Ground Bounce and EMI

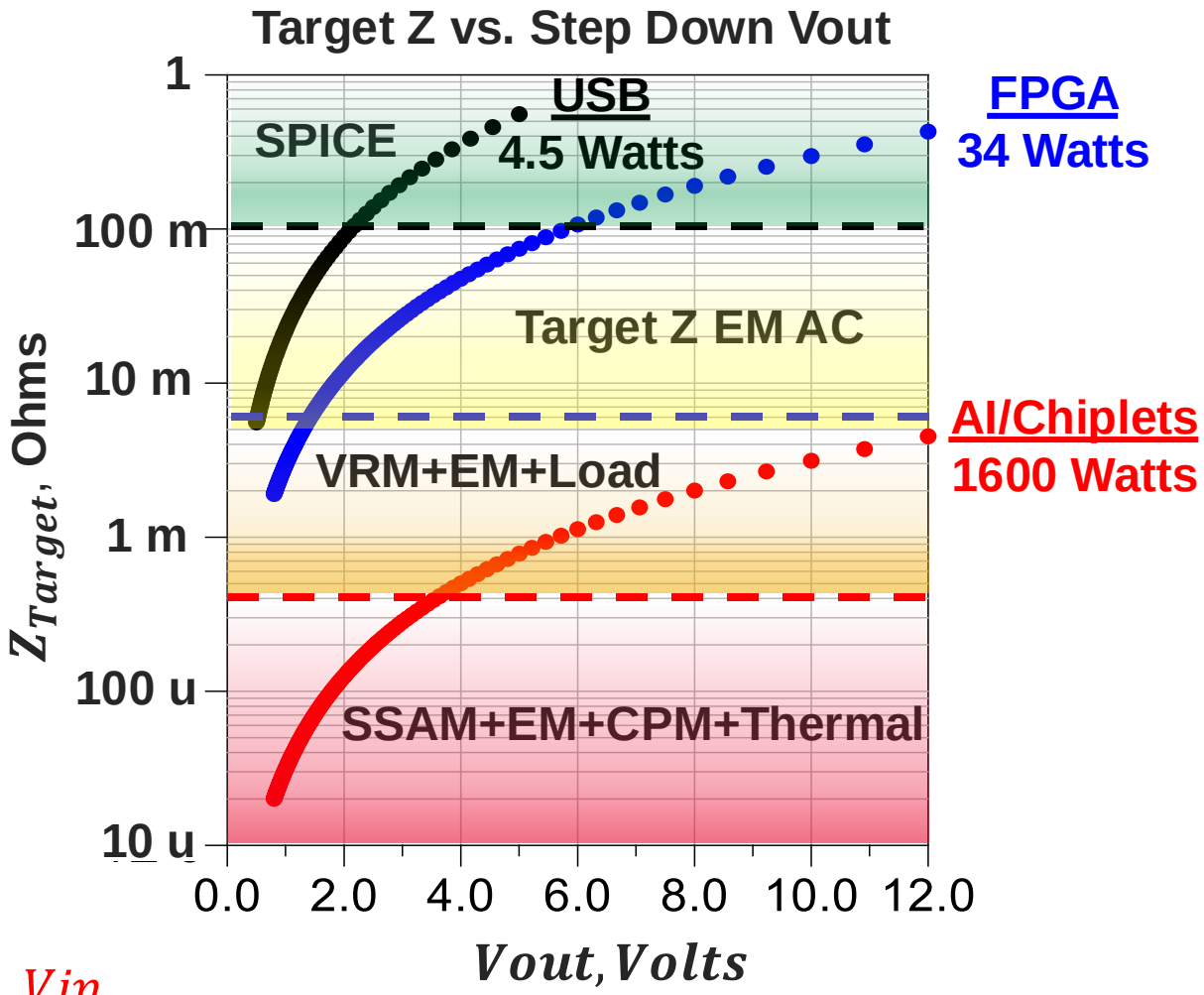
Heidi Barnes, Power Integrity Engineer

Hardware Engineers are Learning the Hard Way
Power Integrity Requires EM Simulation!

PCB EM is needed for designing for Target Z that is down in the micro-ohms.

Target Impedance Calculation

$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$



Note- Target Z Rules of Thumb:

- 5% allowed Voltage Ripple
- Dynamic Transient Current 50% of Imax
- VRM DC to DC Converter where Vout =D*Vin

Power In = Power Out $Vin * Iin = DVin * \frac{1}{D} Iin$

Core Power Rail $Z_{Target} = \frac{D * Vin * 5\%}{\frac{1}{D} * Iin\_max * 50\%} = D^2 \frac{Vin}{Iin\_max} * 10\%$

*VRM (Voltage Regulator Module)

Agenda

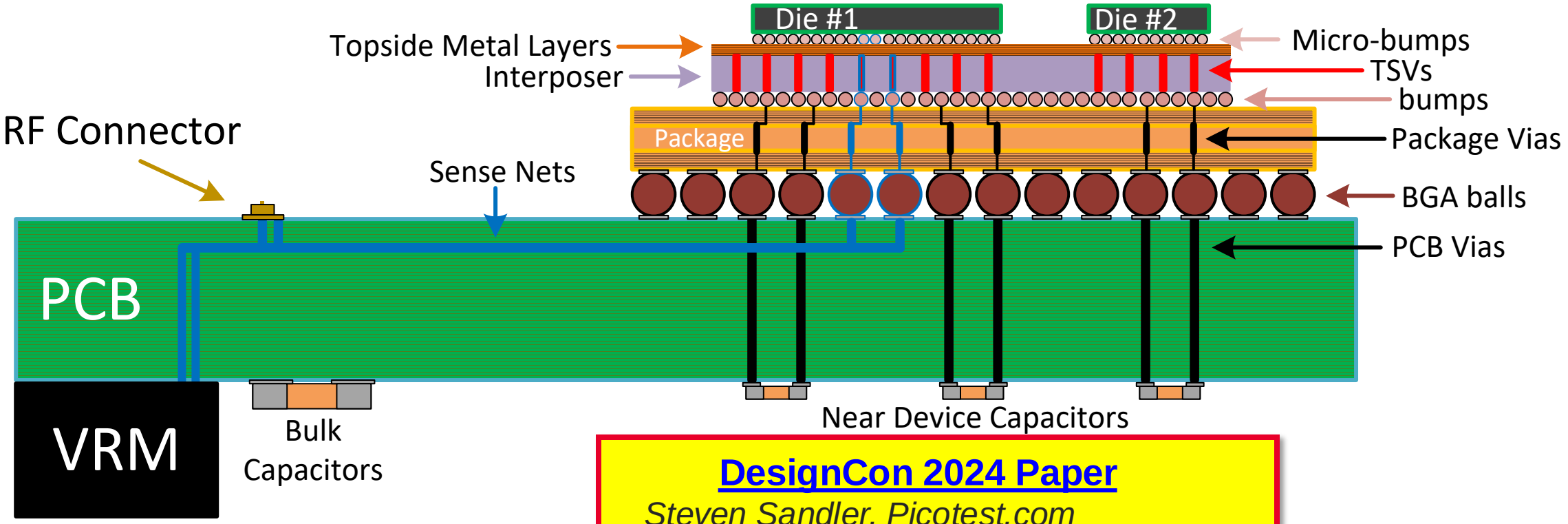
- **The Noise Challenge with 1000 Amps per Nanosecond**
  - *Learn how to use Harmonic Balance for non-linear PI Digital Twin simulations*
- **Conducted EMI – DC/DC Converter Noise Source**
  - *Learn how automation is simplifying complex dc/dc converter EMI simulations*
- **Crosstalk/Ground Bounce – Dynamic Sink Noise Source**
  - *Learn how to separate ground bounce from net-to-net power rail crosstalk*

New for ADS 2025 Update 2

PDN Design, Simulation, and Validation of a 2000 Amp Core Power Rail

Understanding the Power Delivery System

- VRM Vendors, Scalable Topologies, Power Delivery Network (PCB, Package and Die)



DesignCon 2024 Paper

Steven Sandler, Picotest.com
Benjamin Dannan, Signal Edge Solutions
Heidi Barnes, Keysight Technologies
Idan Ben Ezra, Broadcom
Yu Ni, MPS

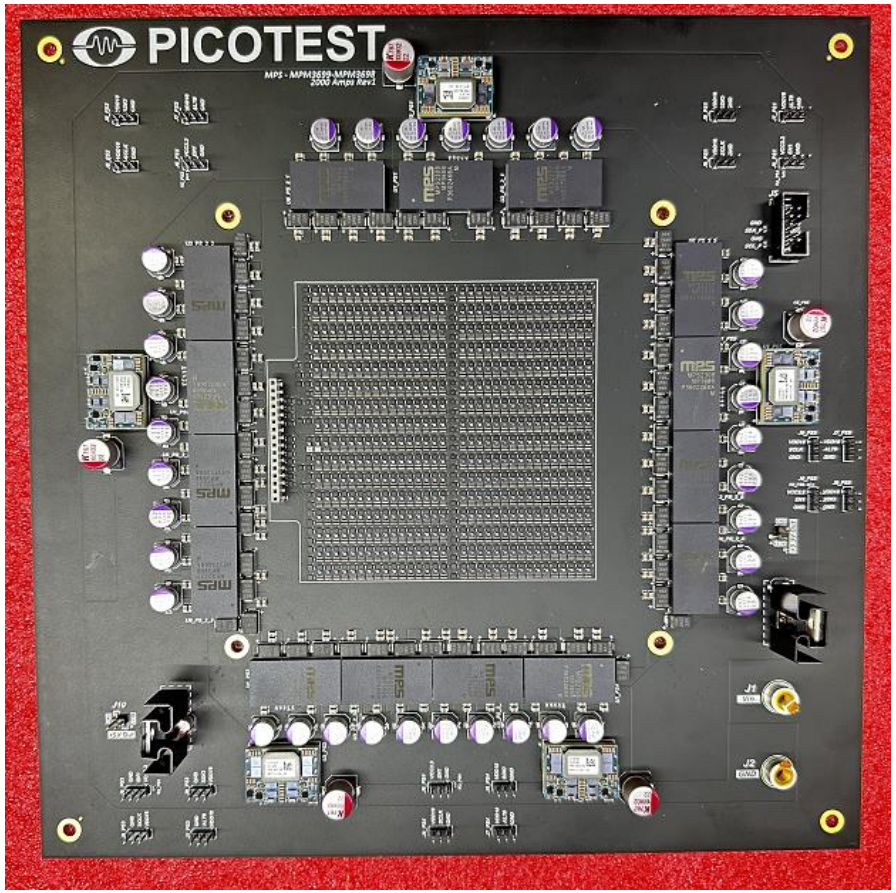
Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

The Picotest 2000 Amp VRM and Step Load Design

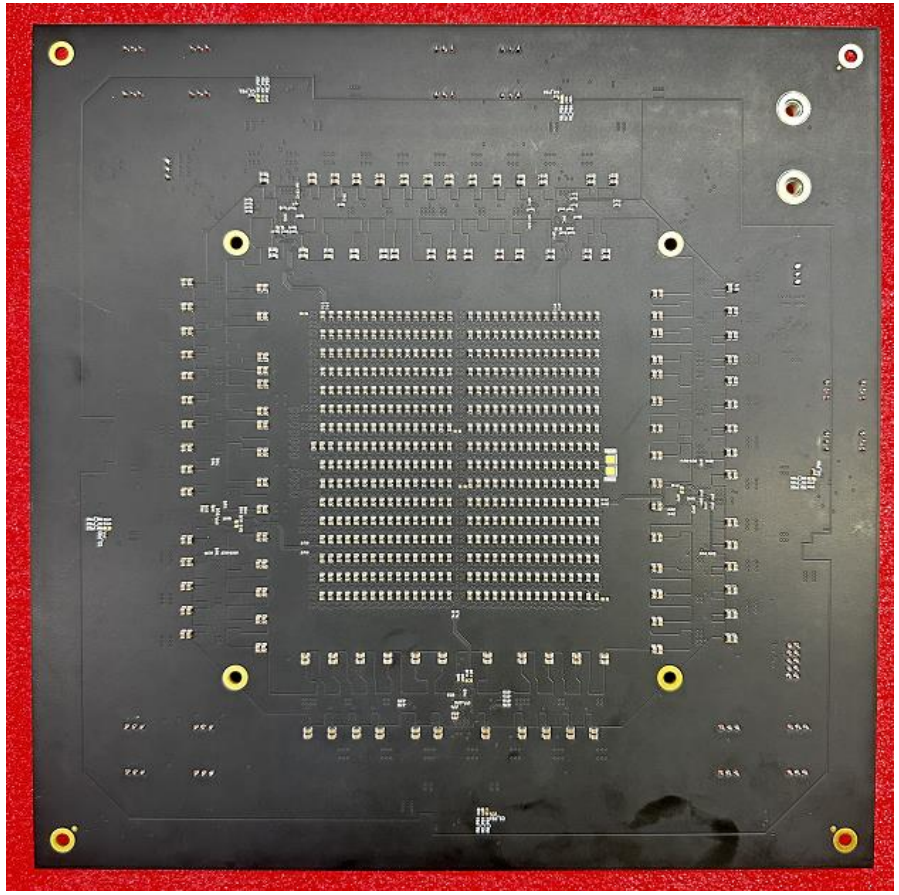
Custom PDN step loaders enable large signal testing for power rail ripple and crosstalk.

- 15 MPS Modules
- 5 Groups
- 5x 48V to 12V
- 15x 12V to 0.8V
- 55 Phases
- 512 Load Cells
- 11 bit 50 MS/s

TOP



BOTTOM

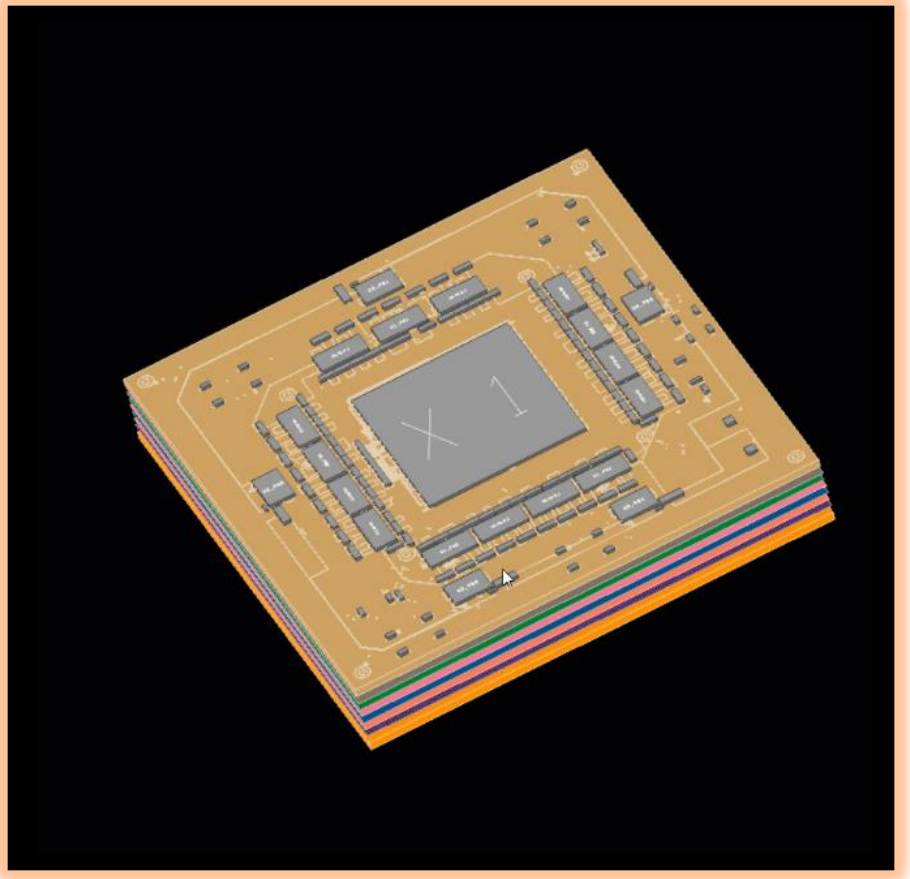


Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

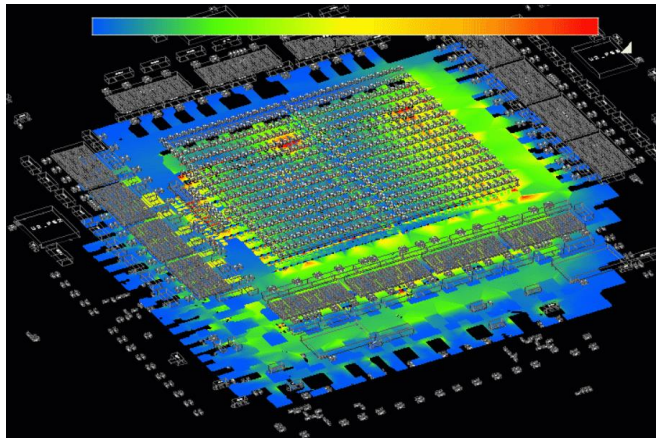
2000 Amp PDN EM Simulations → DC, AC, and Thermal

EM simulators are critical for achieving Target Z in the micro-ohms

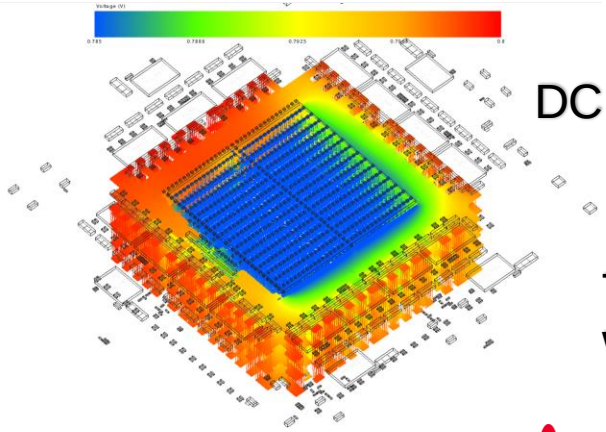
Picotest Step Loader



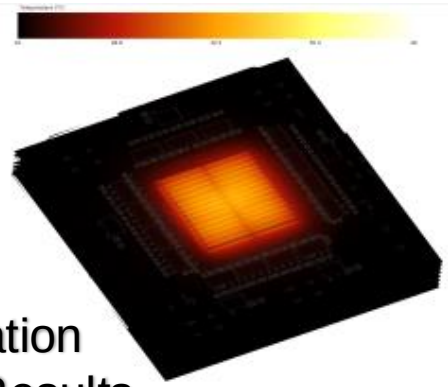
Keysight PIPro



AC Current Density



DC IR Drop



Thermal Simulation Water Cooled Results

KEYSIGHT

PICOTEST

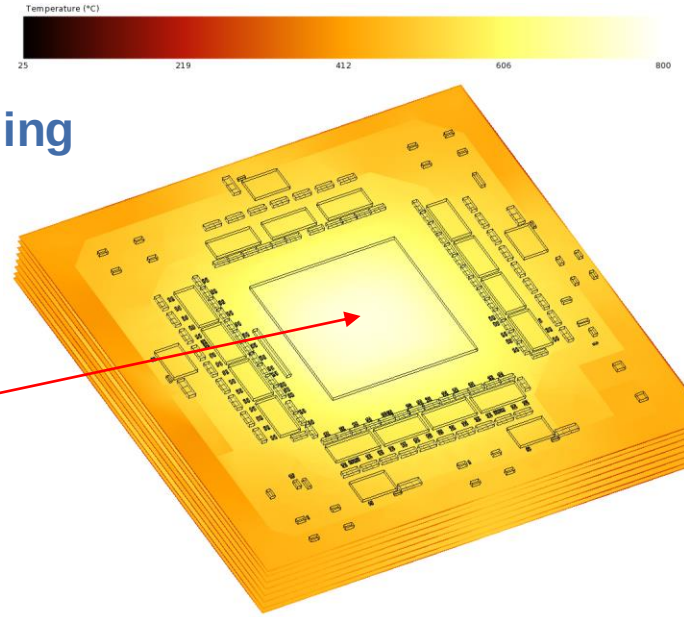
KEYSIGHT EDA

Validating Thermal Considerations

PIPro DC IR Drop can be directly copied to DC Electrothermal to check thermal cooling requirements.

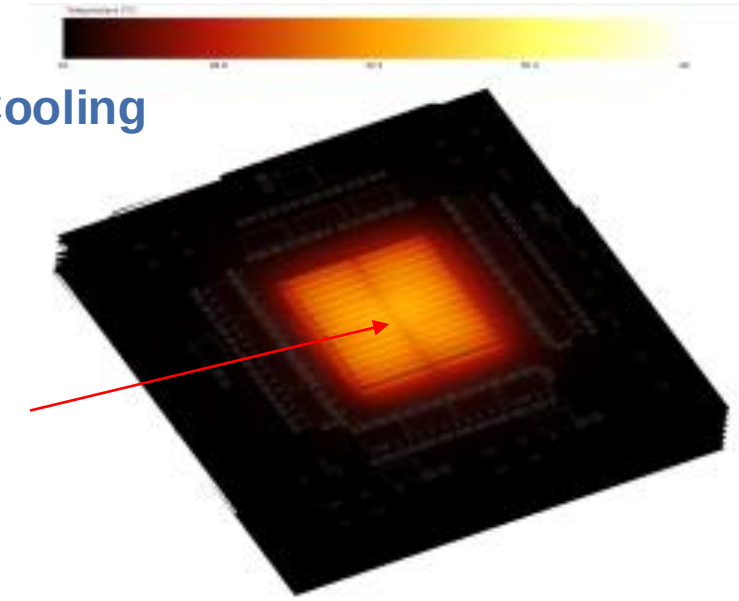
Thermal Analysis

- Operating at 2000 Amps steady state, along with large dynamic step loads, can generate significant thermal heat rise in components



No Cooling

766 C



With Cooling

37 C

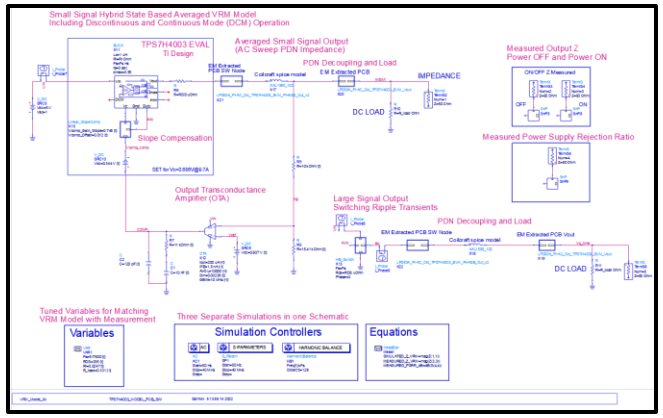
Thermal analysis for a 2000A load with no cooling on the left, and with cooling on the right. This is a symmetric design, so the hottest location is in the center with 766C on the left with no cooling, and a reasonable 37C on the right with ideal water cooling

Digital Twin End-to-End Modeling

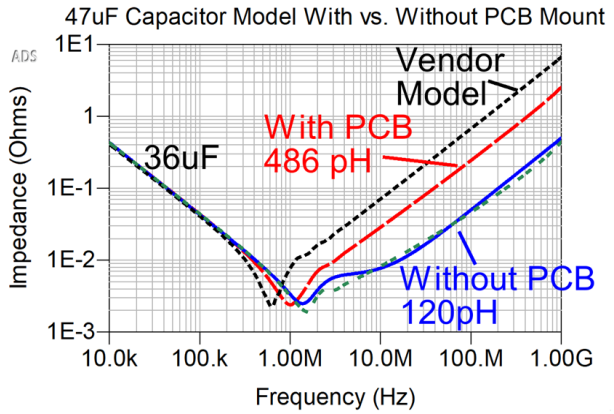
*"SIMPLIS and SABER **DO NOT** work for end-to-end power integrity modeling with die!"*
Ben Dannan of Signal Edge Solutions

If vendors don't provide models for all EDA tools, then build a behavior model

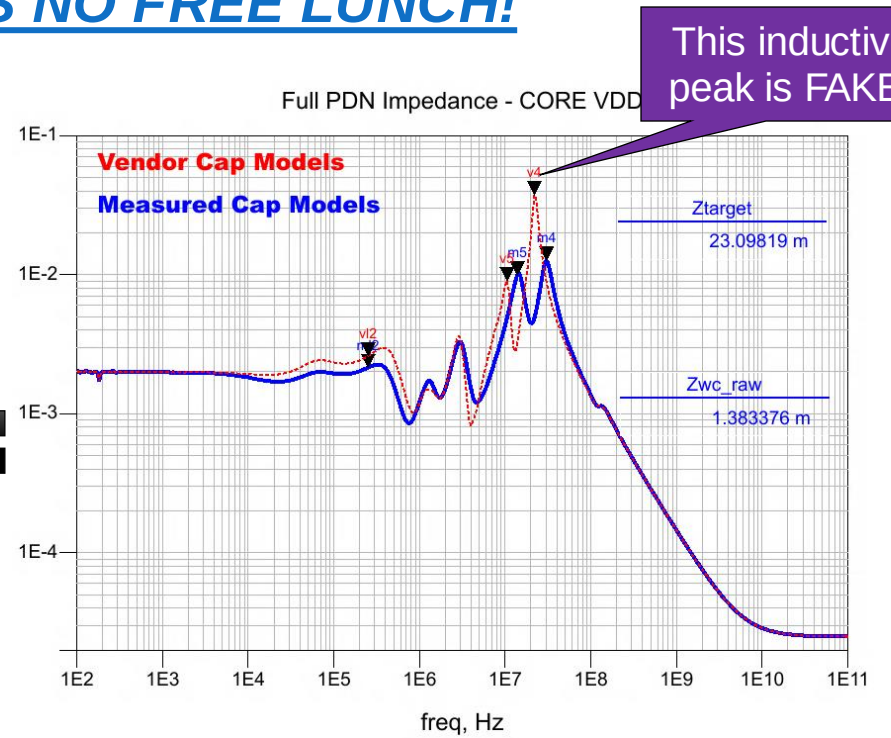
- *Vendor Capacitor models are provided for free – **THERE IS NO FREE LUNCH!***
  - *VERIFY your cap models!*
  - *There is no industry standard!*



Source: DesignCon2023 – VRM Modeling and Stability Analysis for the Power Integrity Engineer – S. Sandler, B. Dannan, & H. Barnes, C. Yots

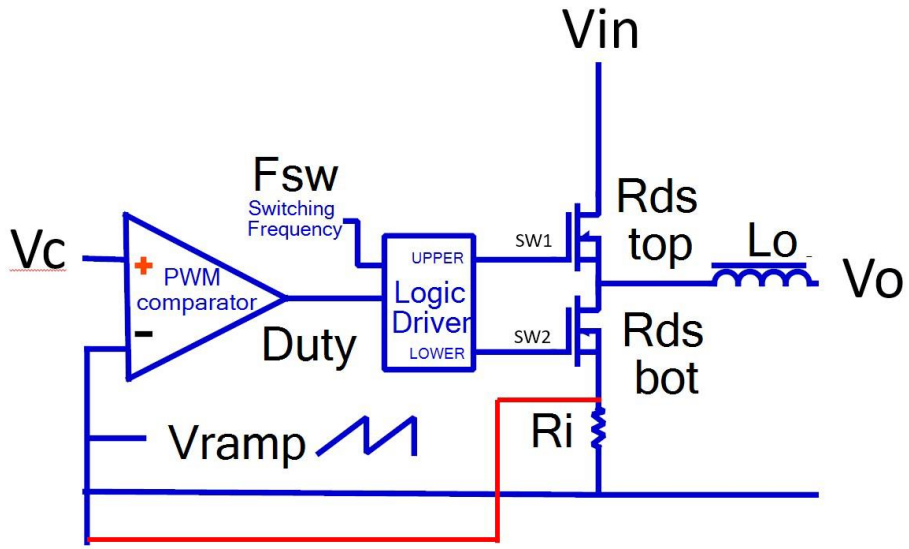


Source: EDICon 2021 Partial Inductance – The secret to correlating simulation and measurement – S. Sandler, B. Dannan, & H. Barnes

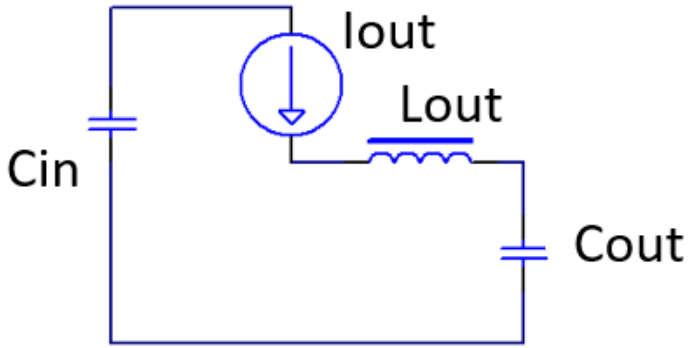


Source: Signal Integrity Journal 2024. Who Put that Inductor in My Capacitor – W. McCaffrey, et. Al

What is a State-Space Average (SSAM) VRM Model



A state space model is a simple way of modeling the two states of a switched mode dc/dc power supply



State 1: SW1 = On and SW2= Off

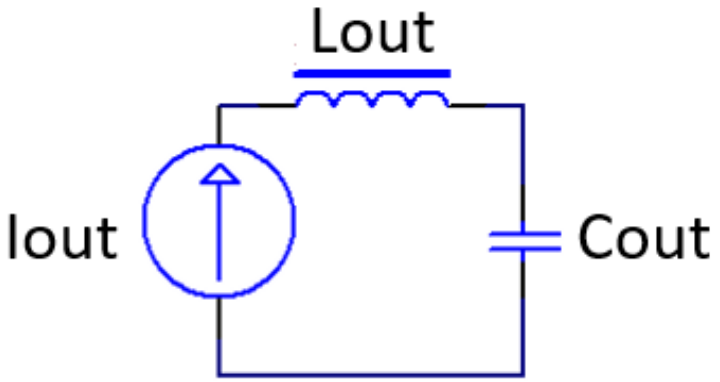
STATE SPACE AVERAGED MODEL

$$Duty = Ton\_SW1 \cdot Fsw$$

$$Vout = Vin \cdot Duty$$

CURRENT MODE

$$Iout = k\frac{Vc}{Ri}$$

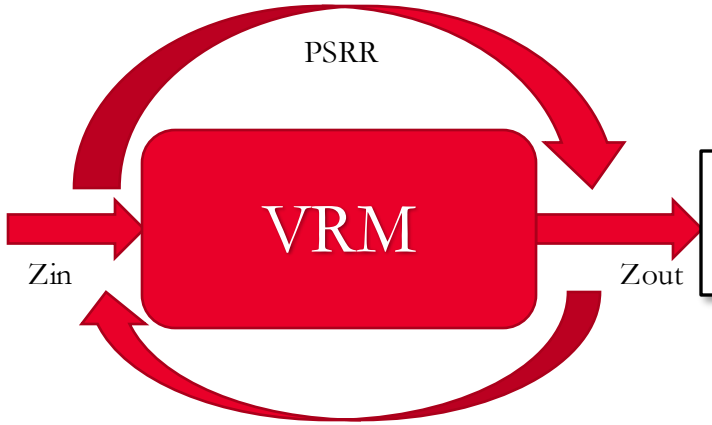


State 2: SW1 = Off and SW2= On

The Switch Mode Power Supply State Space Equations

Parameter	Description
Lo	Output Filter Inductance
Vc	Error Amp Output Voltage
Fsw	Switching Frequency
Vin	Input Voltage
Vo	Output Voltage
DCR	Output Filter Inductor DCR
RDSon	Mosfet RDSon
Ri	Current Sense Resistance
Vramp	Slope Comp/Ramp
Av	Feedback Amplifier Gain

$$PSRR\_dB = 20log\left[\left|\frac{Vo\cdot(Ri\cdot Vo - 2\cdot Fsw\cdot Lo\cdot Vramp}{Ri\cdot Vin^2 - 2\cdot Ri\cdot Vo\cdot Vin + 2\cdot Fsw\cdot Lo\cdot Vin\cdot Vramp + 2\cdot Av\cdot Fsw\cdot Lo\cdot Vin}\right|\right]$$



$$Rout = \frac{\frac{2\cdot Fs\cdot Lo\cdot Ri\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp} + DCR + RDSon}{1 + Av\cdot\frac{2\cdot Fs\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}}$$

$$Lout = \frac{Lo}{1 + \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}\cdot Av}$$

$$Bode = \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}\cdot Av$$

$$Ri \cong \frac{\Delta Vc}{\Delta Io}$$

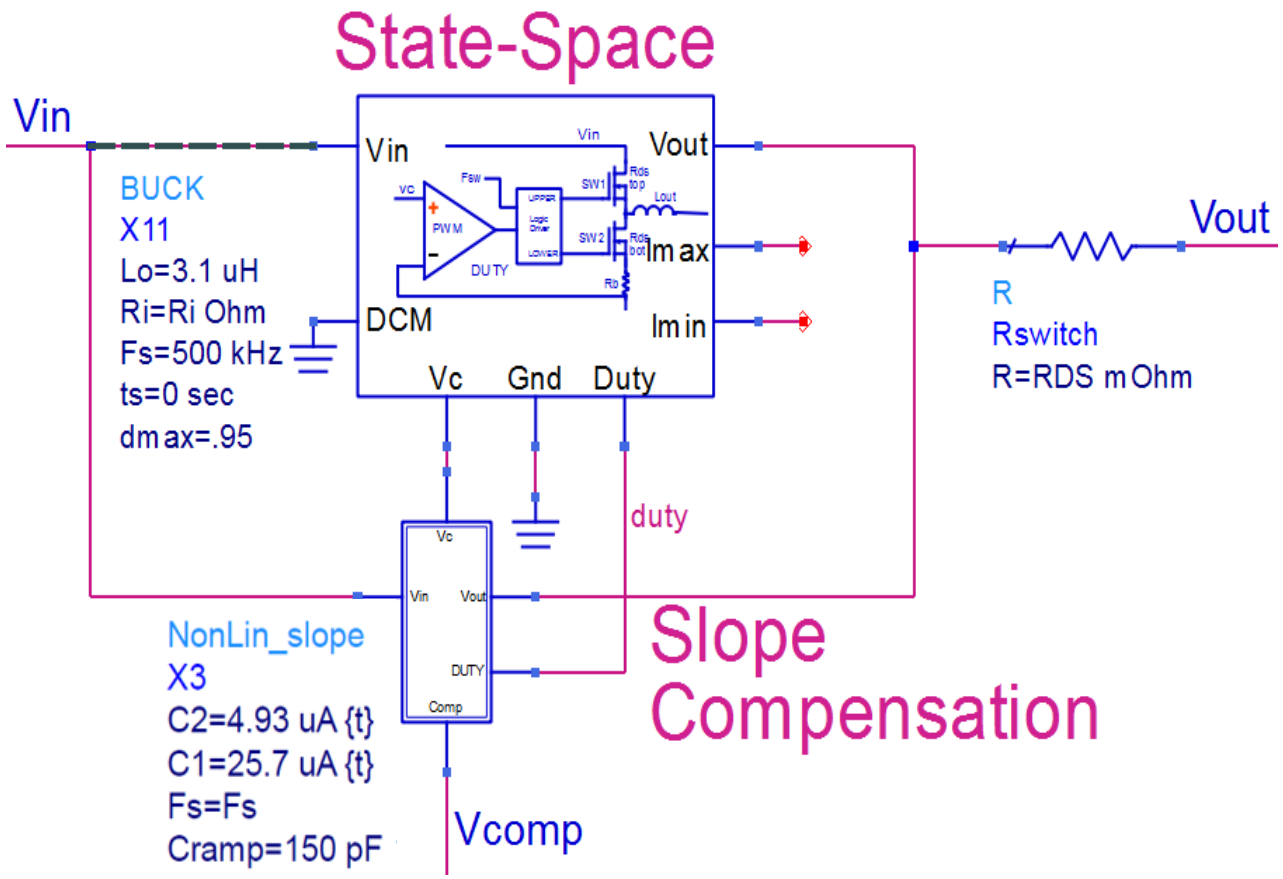
$$\frac{Vo}{Vc} = \frac{2\cdot Fsw\cdot Lo\cdot Vin}{Ri\cdot Vin - 2\cdot Ri\cdot Vo + 2\cdot Fsw\cdot Lo\cdot Vramp}$$

The Sandler State Space Average Model (SSAM) only needs a few data sheet parameters and measurements to create a high fidelity VRM model.

Frequency domain characteristics are determined by solving non-linear differential equations using a technique known as State Space Modeling

Small Signal PARAMETERIZED MODEL

The small signal AC model determines the correct duty cycle for a given load.



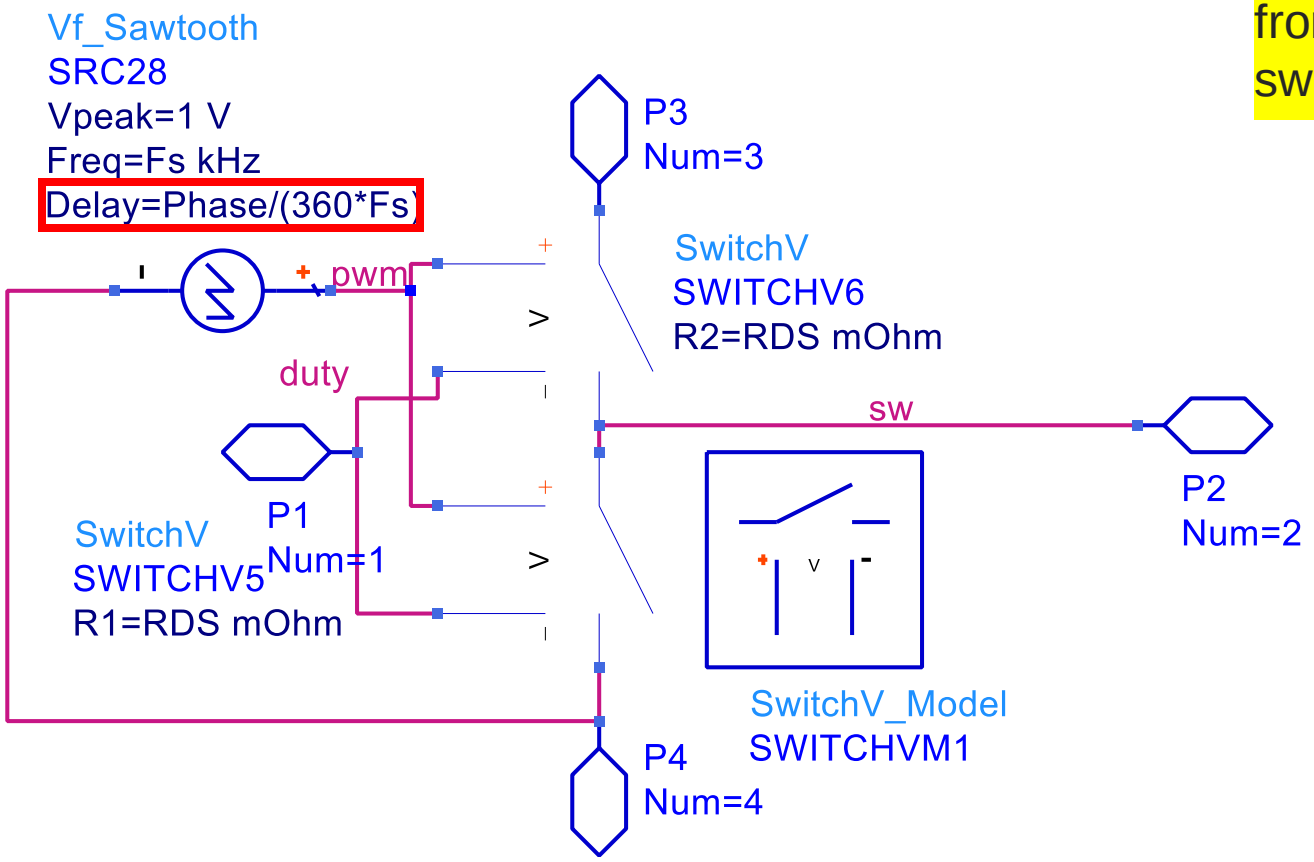
The math is inside these blocks. The required parameters are passed to the model

Just enter the parameter values, most of which are easily identified

We'll determine those that aren't easily identified using a few very simple measurements

$$Vramp = \frac{C1+C2\cdot(Vin-Vout)}{Fs\cdot Cramp}\cdot DUTY$$

ADDING Large Signal TIME DOMAIN RESULTS



The large signal model uses the duty cycle from the small signal result to generate the switching transients

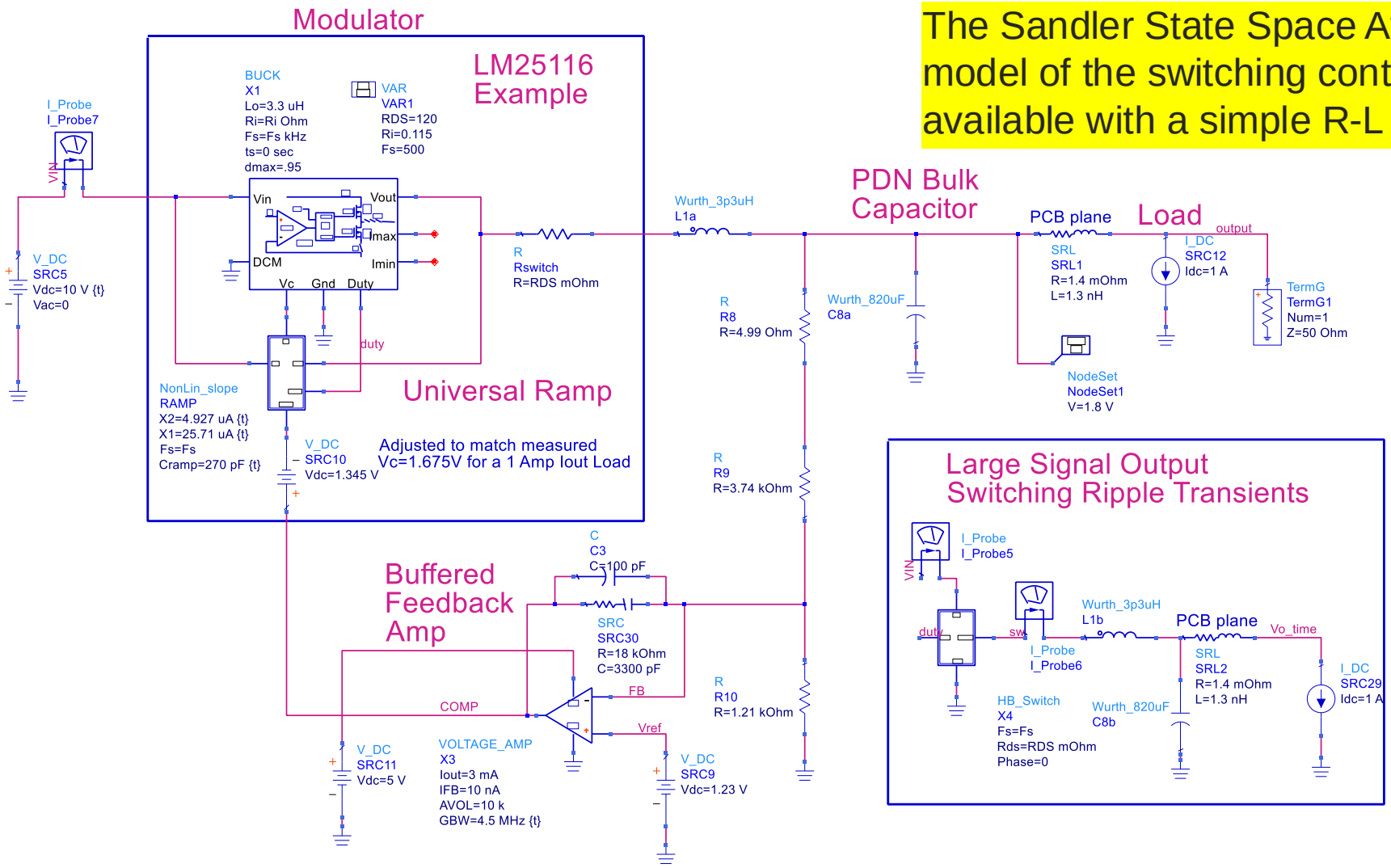
The state space model knows the instantaneous duty cycle, or switch positions, at every instant in time

A 1V ramp at the switching frequency converts the duty cycle to switch positions

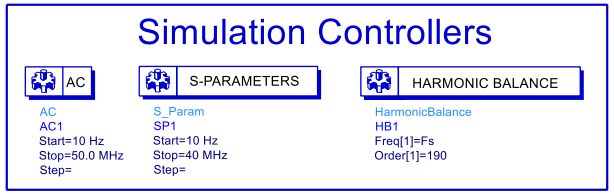
A delay is used to position independent phases in a multiphase system

Complete Parameterized Small Signal and Large Signal VRM Model

The Sandler State Space Average Model provides a complete model of the switching control loop behavior which is not available with a simple R-L model.



Three Separate Simulations in one Schematic

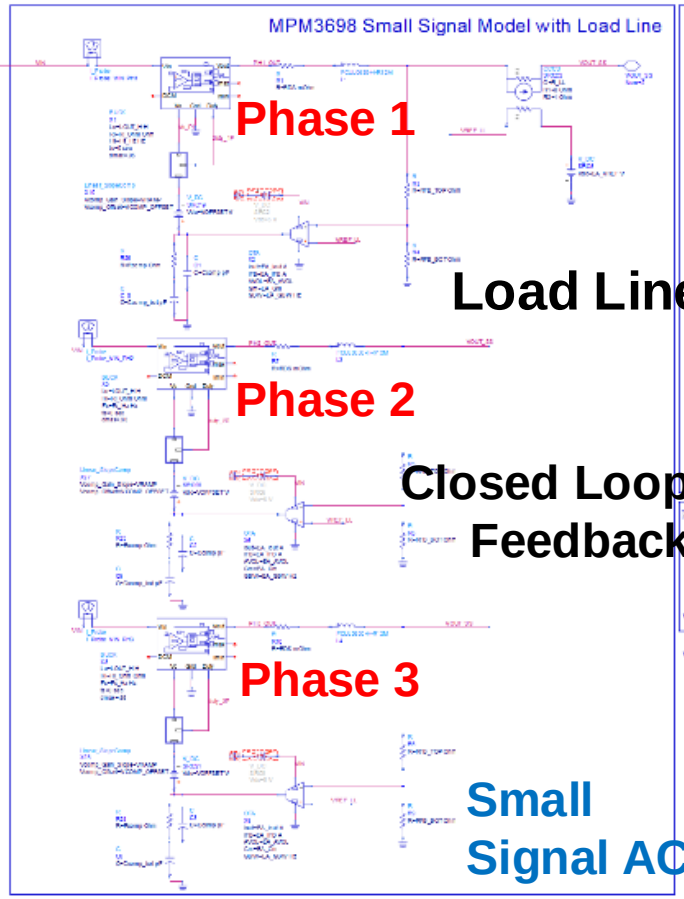


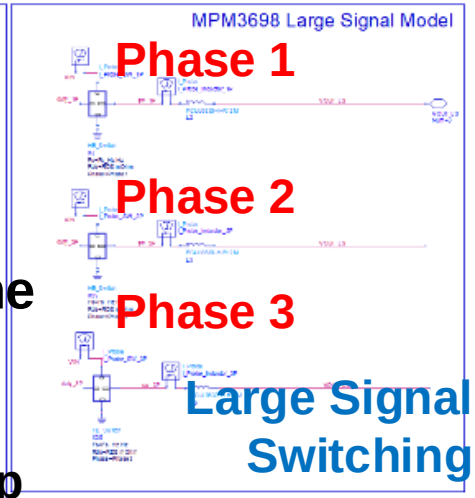
Note that the output network, including the output inductor, capacitors (and the PCB if included) must be EXACTLY replicated in the state space and large signal models

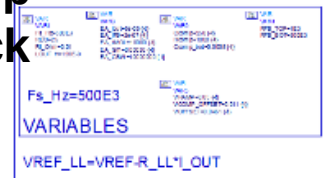
55-Phase VRM SSAM Model with Load Line

The SSAM can be cascaded for high current multi-phase power delivery.

5x MPM3698 – 3 phases

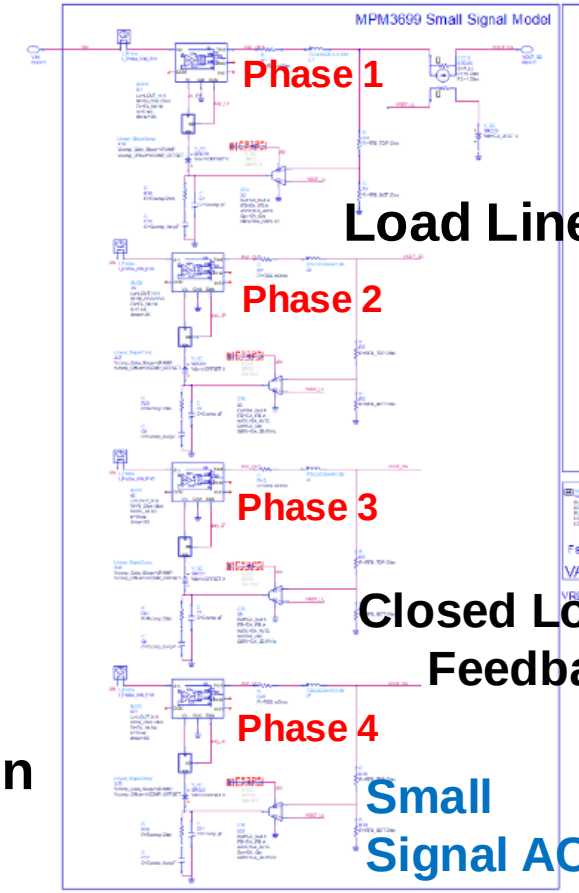


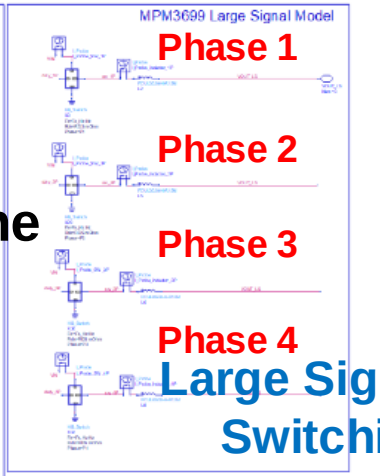




Harmonic Balance
Steady State Solution

10x MPM3699 – 4 phases



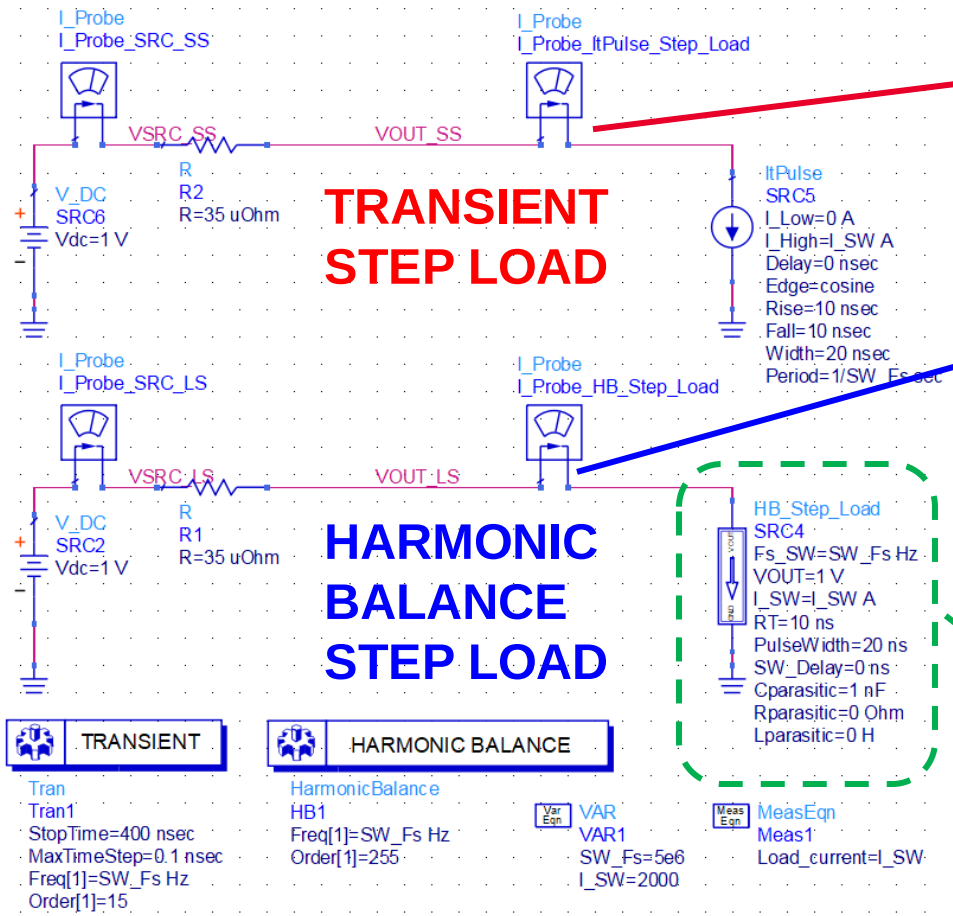


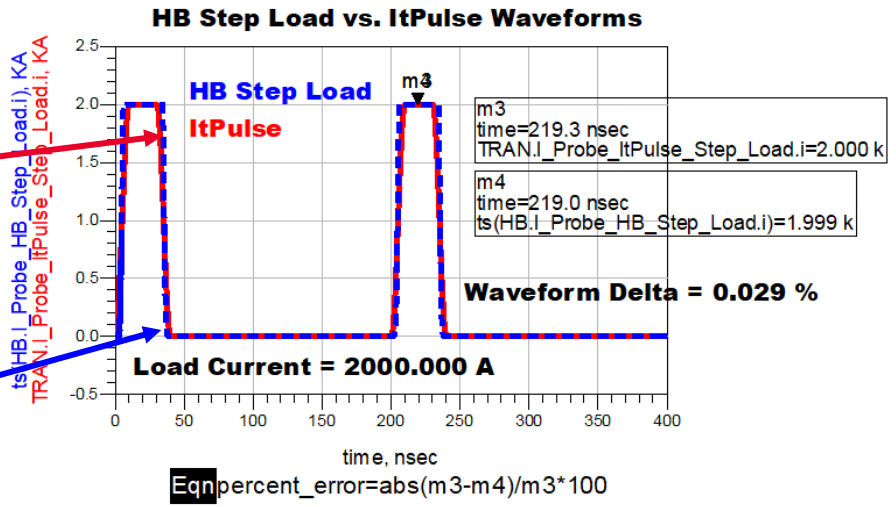
Sandler State-Space Average VRM Model was used for both the MPM3698 and MPM3699

Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

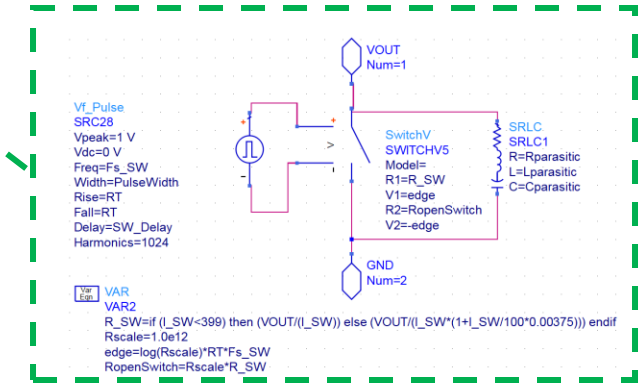
ADS Harmonic Balance Simulation with the Step Load Model

- Creating a step load model for simulation with Harmonic Balance in ADS





HB step load model correlates very well to the Transient step load model



Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

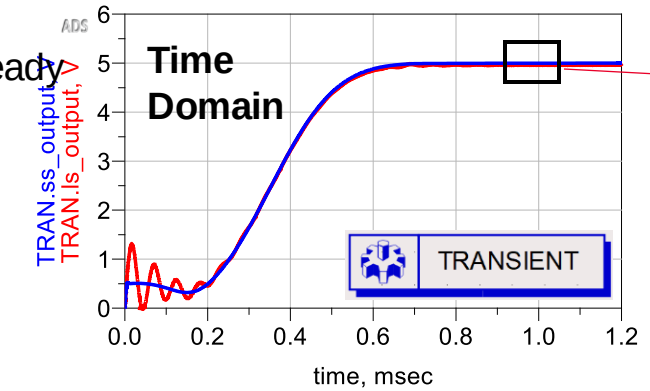
Why use the Harmonic Balance Simulator with SSAM

- Fourier Theory says time domain waveforms are made up of frequency domain waveforms.
- Solving a circuit in the Frequency Domain can be much faster since it limits the frequencies and jumps to steady-state.

Transient must reach steady state to measure ripple.

50,000 time-steps!

Simulator Results



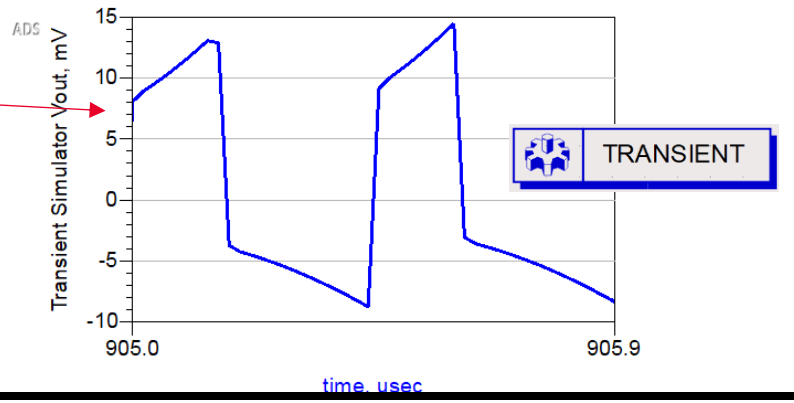
Time Domain

Transient Sim

Wait for Steady State

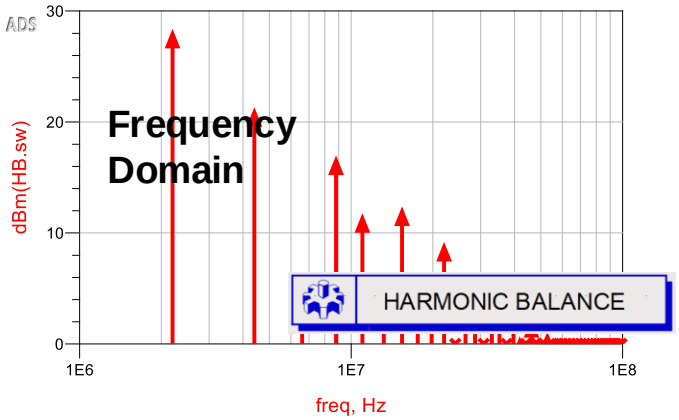
Minutes, Hours, **Days**

Steady State Ripple vs. Time



Harmonic Balance simulates harmonics of the switching frequency.

Only 255 Frequencies for steady state ripple!

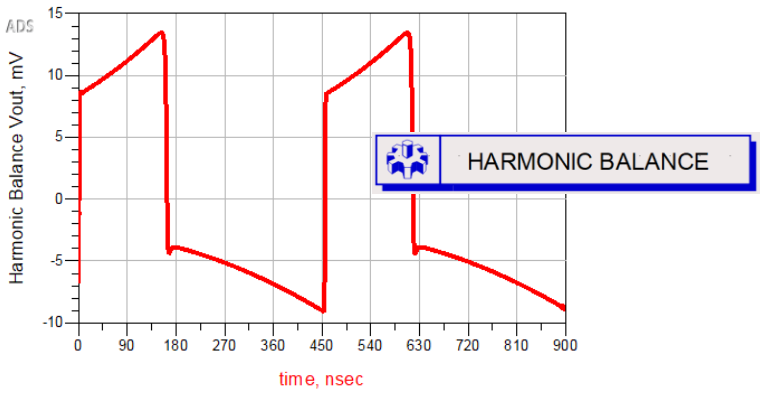


Frequency Domain

Harmonic Balance Sim

FFT jumps to Steady State

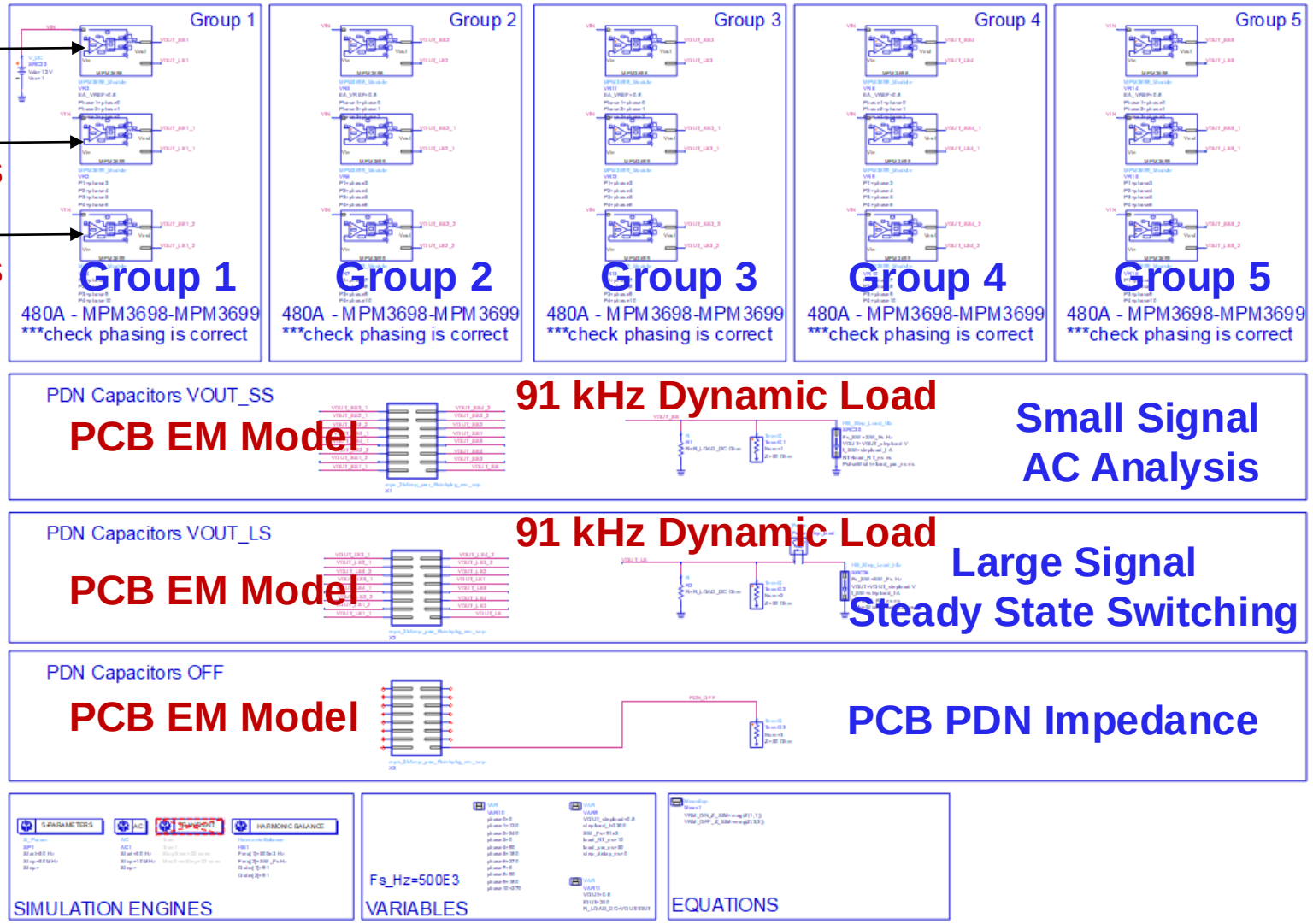
Seconds, Minutes, Hours



Data shown is for one VRM, typical PCB design has dozens of VRMs

End-to-End 55 Phase VRM Digital Twin Model

MPM3698
3 Phases
MPM3699
4 Phases
MPM3699
4 Phases



500 kHz Switching Frequency

Final End-to-End Power Delivery simulation for delivering 2000 Amps.

Harmonic Balance Steady State Solution

KEYSIGHT

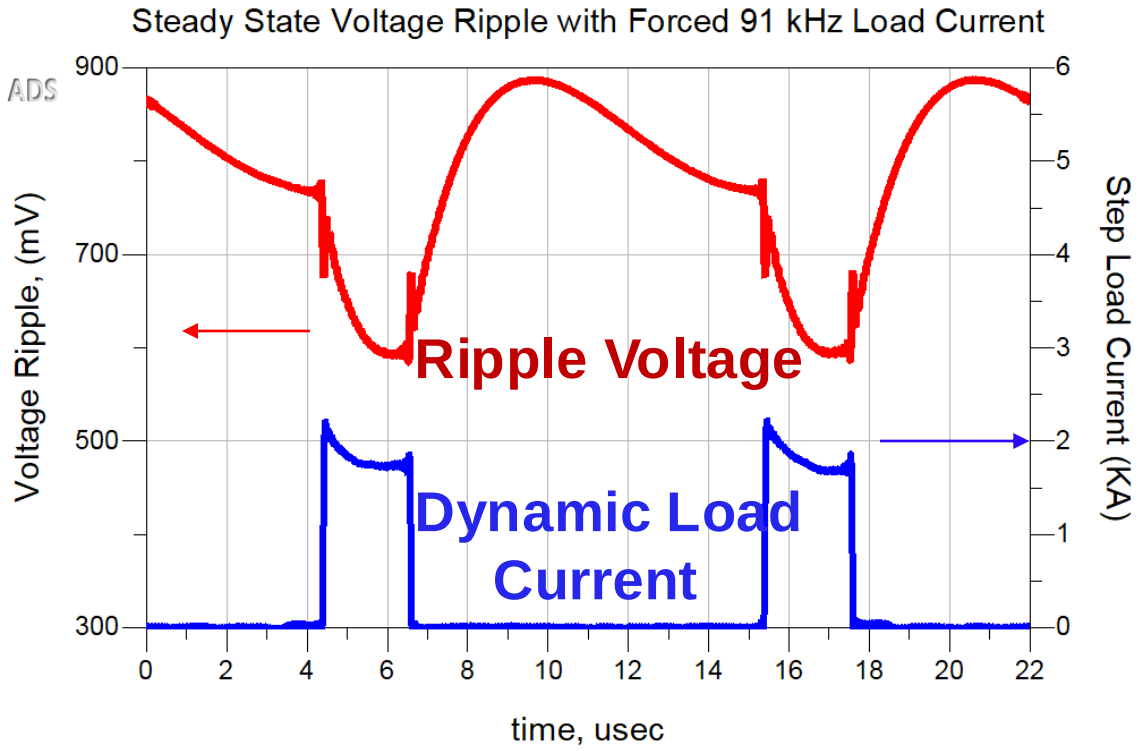
Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

End-to-End Digital Twin Simulations

- A complete system simulation model is created with accurate capacitor models, EM-extracted PCB effects, and a 2000A VRM model that was scaled by using 5 groups of MPM3698 and MPM3699 modules

55 Phases at 500 kHz
Dynamic Load at 91 kHz

Steady State Harmonic Balance Results in 77s

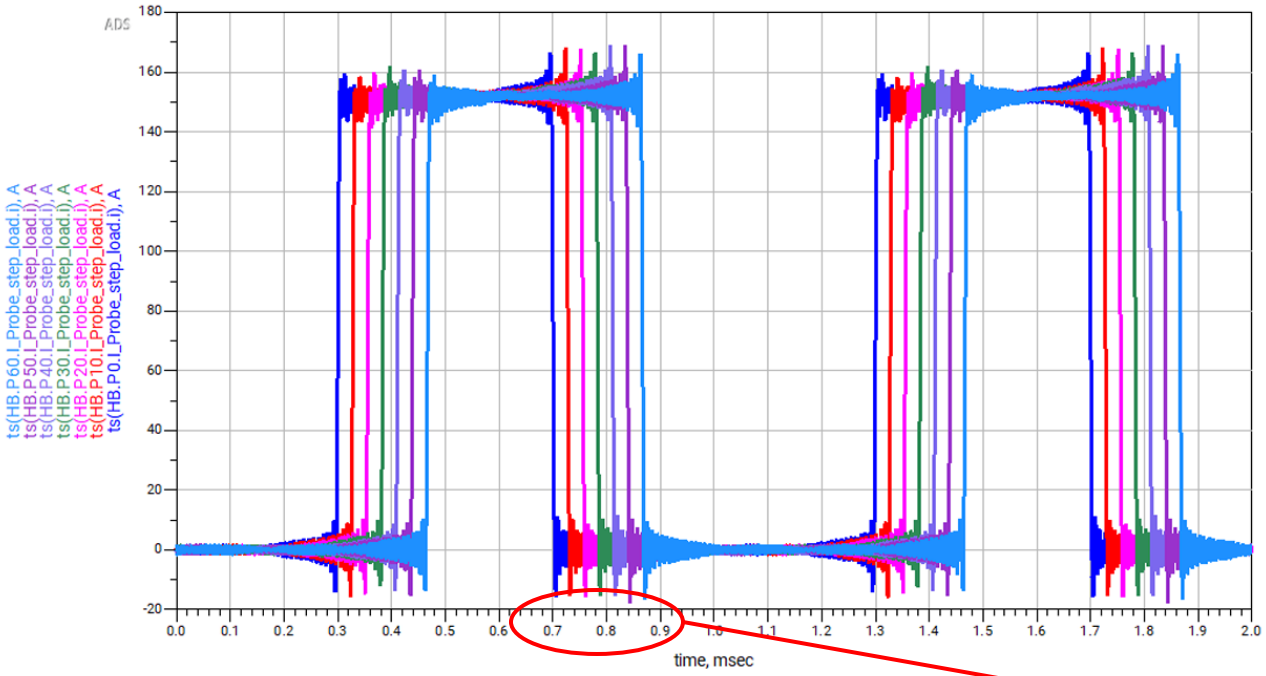


Steven Sandler et al. “Design, Simulation, and Validation Challenges of a Scalable 2000 Amp Core Power Rail”, DC2024.

Non-Linear Large Signal Step Load Response, Different Start Times

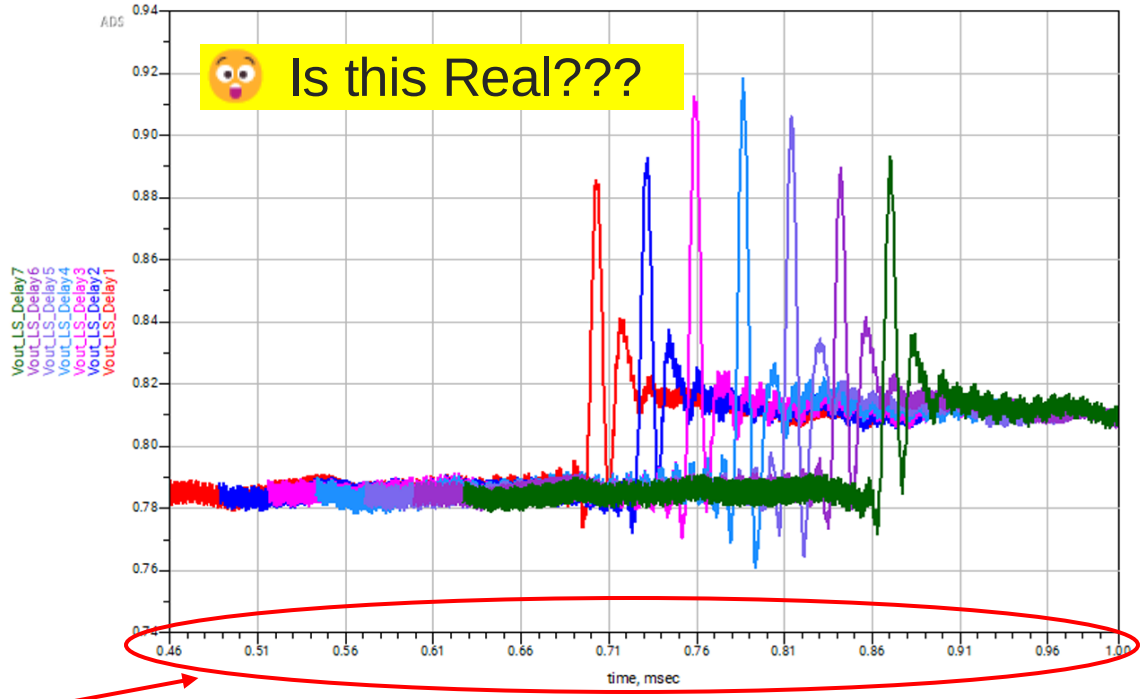
- *7 Phase 500kHz Switching VRM with 1kHz 160Amp Dynamic Load Example*

Different Start Times
Same 1kHz, 160 Amp Excitation



Excitation

Voltage Kick at 160A Load Dump
Large Signal Response is **Not the Same**



Power Rail Ripple

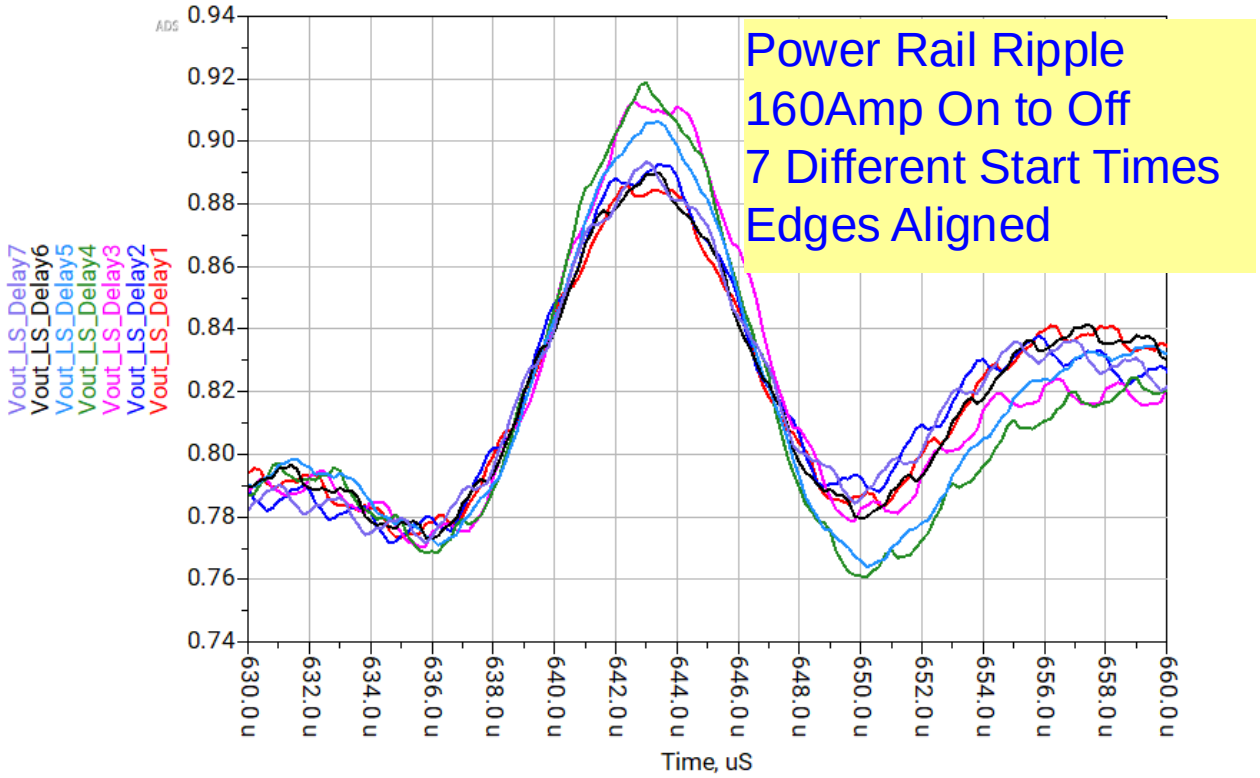
Zoom-in on 160Amp
On to Off Load Step

Harmonic Balance Captures Large Signal Voltage Ripple

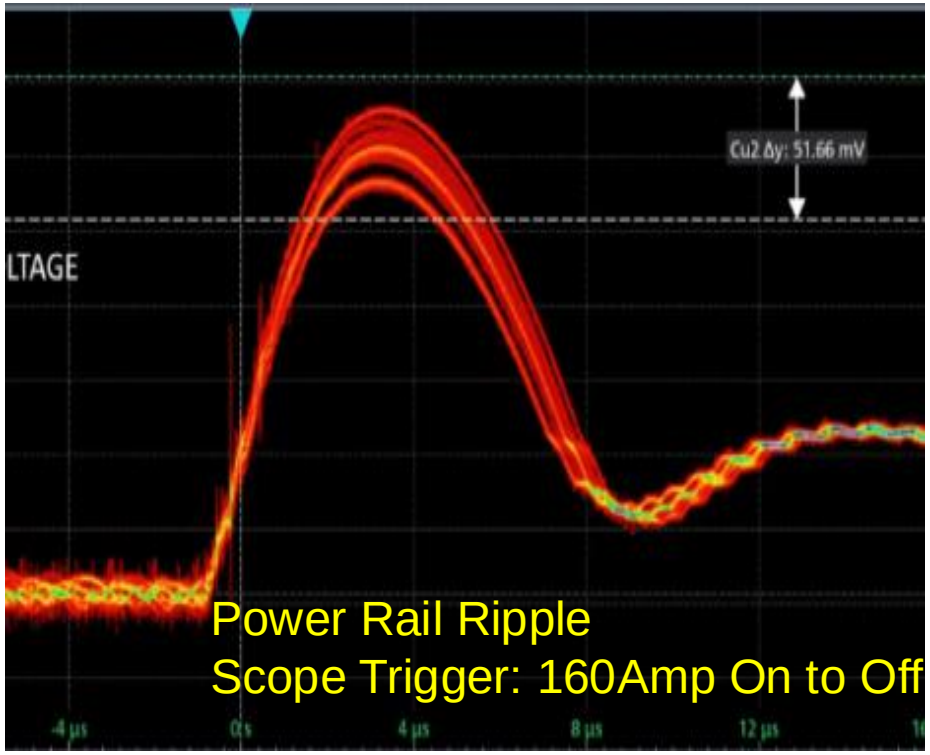
- *7 Phase 500kHz Switching VRM with 1kHz 160Amp Dynamic Load Example*

LOAD Step On-to-Off Voltage "Kick" has multiple responses for the same 160A LOAD Step

Digital Twin Simulation



Measurement



7 Simulations in 10 Minutes!!!

Agenda

- **The Noise Challenge with 1000 Amps per Nanosecond**
  - *Learn how to use Harmonic Balance for non-linear PI Digital Twin simulations*

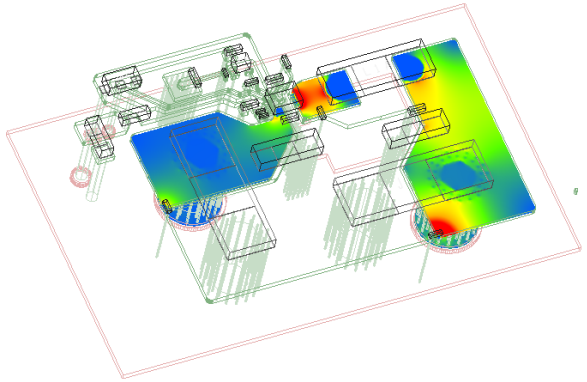
- **Conducted EMI – DC/DC Converter Noise Source**
  - *Learn how automation is simplifying complex dc/dc converter EMI simulations*

New for ADS 2025 Update 2

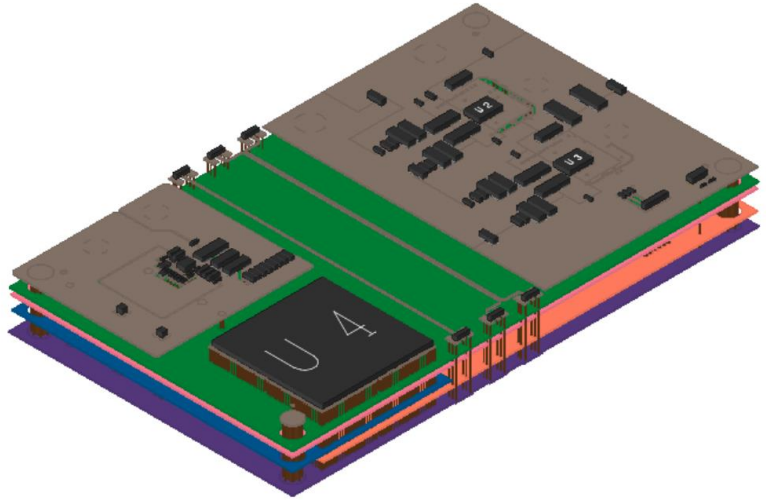
- **Crosstalk/Ground Bounce – Dynamic Sink Noise Source**
  - *Learn how to separate ground bounce from net-to-net power rail crosstalk*

How Automation is Helping the PI Engineer Solve EMI and Ground Bounce

- **PIPro Conducted EMI**



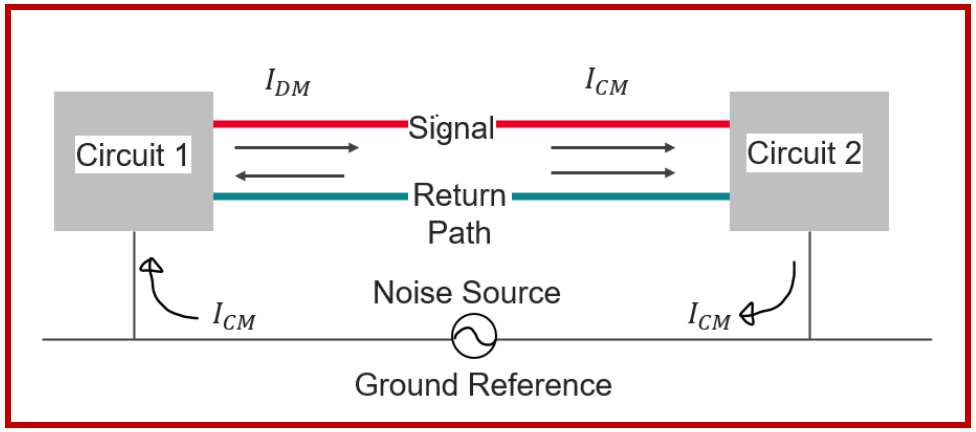
- **PIPro Dynamic Sink Analyzer**



Common Mode Currents are the Main Source of EMI

Un-desired return paths cause EMI !

Signal Integrity

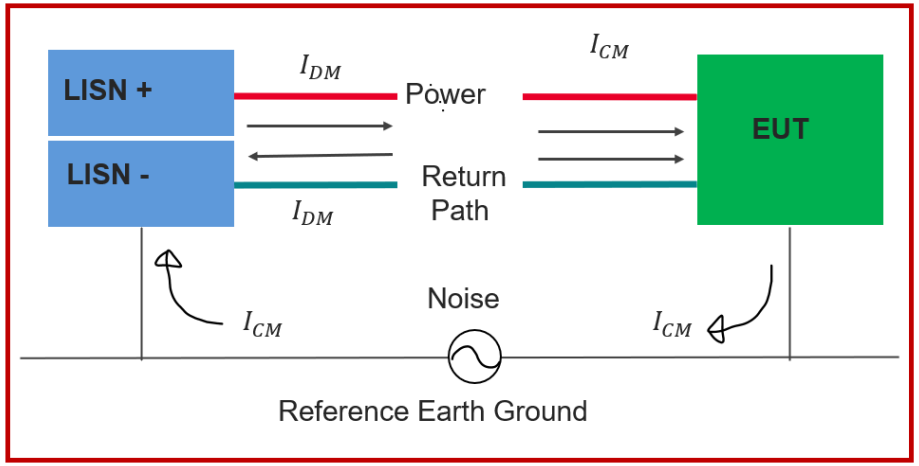


It only takes 5µA of common current to fail an FCC part 15 Class B EMC compliance test.

[Rule of Thumb #31: How much common current on external cables is too much?]

https://www.edn.com/how-much-common-current-is-too-much-rule-of-thumb-31/

Power Integrity



Note: LISN = Line Impedance Stabilization Network

The automotive CISPR 25 average limit for the FM band is 18 dBuV. This is only 8mV. 8mV across 50 ohms at the analyzer is 160 nano-Amps!

ADS PIPro Conducted EMI DEMO

PI Conducted EMI Example ships with ADS and one can even buy the hardware from Picotest.com

Conducted EMI Option W3036E In ADS PIPro
2021_ADS_PIPro_CEMI_Demo_wrk
Using Picotest SIC531 PI VRM Demo Board 0-0 with Max Gnd Cut

NOTE:
-Use the View menu pick [Push into Hierarchy] and [Pop Out of Hierarchy] to quickly open the selected schematic symbols below. (The green down arrow and the adjacent up arrow on the icon Tool Bar also push in and pop out of the hierarchy)
-Or right click on a symbol in the schematic and select menu pick >Open Instance View to select the specific view to open and not close the top level schematic.

1) Open the SiC531 Demo Board Layout, Check the Stackup, and Start SIPro/PIPro

Right Click on sic531_demo_00_em symbol below and select >Push Into Hierarchy
In the Layout Window: Select EM>Substrate
Check the substrate stackup then close the window
In the Layout Window: Select Tools>SIPro/PIPro>Open Setup to open PIPro

Max Ground Cut
Switch Node + Inductor
sic531_demo_00_em
0-0

sic531_demo_00_em
X1

2) Inside SIPro/PIPro setup and run a DC IR Drop analsysis and a Conducted EMI analysis.

- If the DC IR drop analysis has an input connector VRM and a discrete VRM with switching configuration then it can be copied to a CEMI analysis. The only modifcation required is to be sure that the decoupling capacitors have been added for the CEMI analysis to get the correct results.

3) Export the Conducte EMI (CEMI) Analysis Testbench to ADS schematic

1) In the SIPro/PIPro window export the CEMI test bench to ADS schematic by going to the CEMI_analysis Results and double clicking on the Generate Conducted EMI Test Bench....

2) The ADS CEMI Test Bench makes it easy to change the risetime, inductor parasitic C, and the input capacitor parasitic inductance. Use the Simulation>Settings menu pick to change the ADS schematic simulation results file name. Then in the ADS data display for the CEMI test bench simulation, use the data set selector in the icon tool bar to toggle between data sets.

Max Ground Cut 0-0
Switch Node + Inductor
PIPro Generated CEMI Test Bench

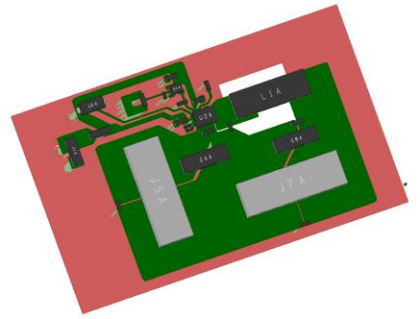
sic531_demo_00_em_CEMI_testbench
X6

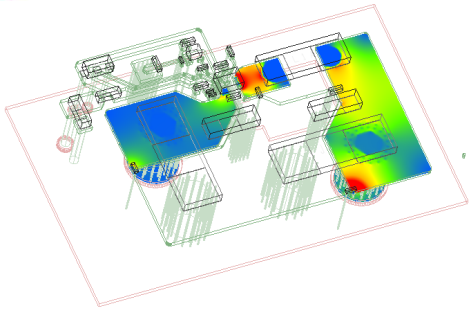
Reference: Component models from measurement and vendor data

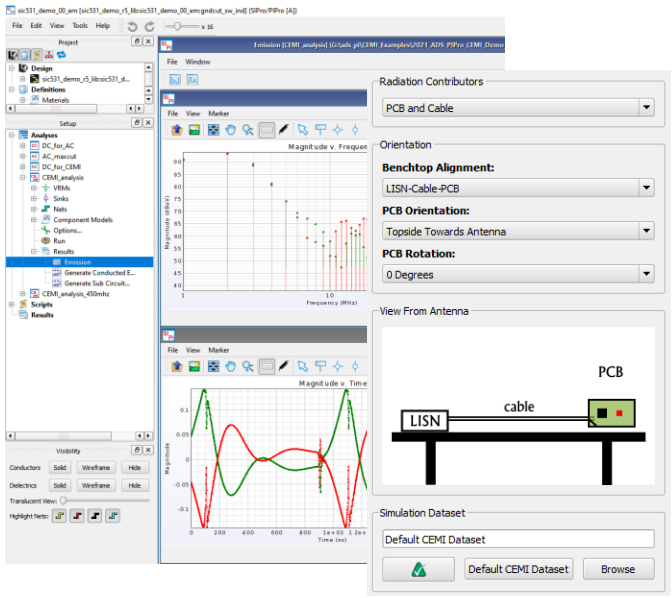
Component Models for
Picotest SIC531 PI Demo Board

00_readme_models
X5

2021_CEMI_Demo_lib | 00_readme | Mon Feb 7 13:03:54 2022



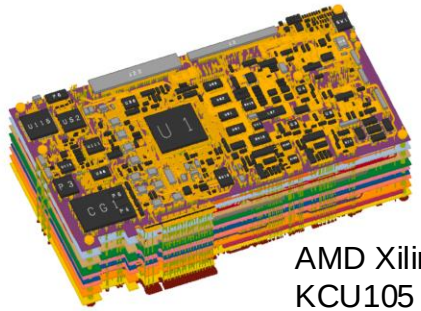




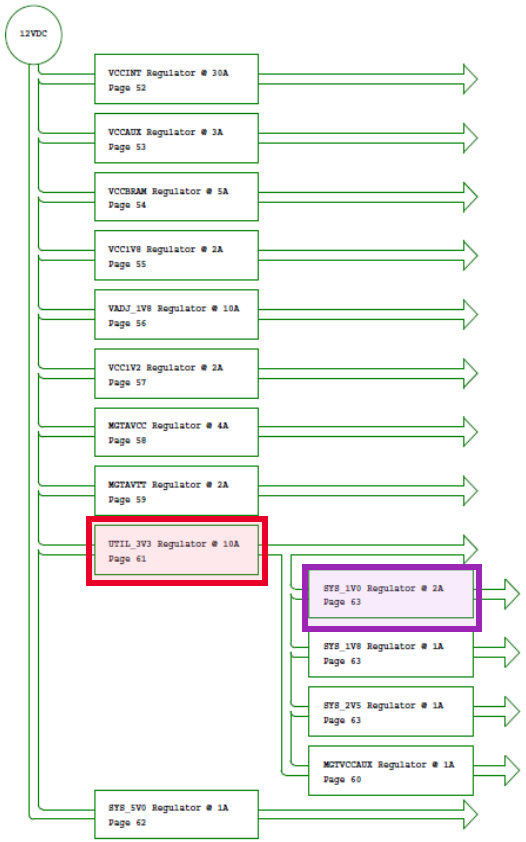
PIPro_Conducted_EMI_Example_wrk.7zads

Cascaded VRMs for DC IR Drop and AC Conducted EMI

Cascaded DC IR drop results can be confirmed with AC results from the PIPro CEMI Analysis



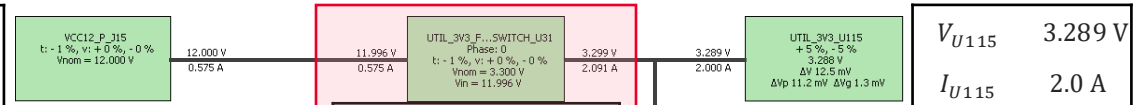
AMD Xilinx KCU105



PI-DC

Power Connector

V_{J15}	12.0 V
I_{J15}	575 mA



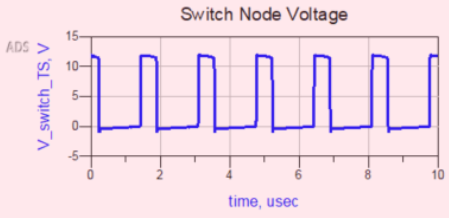
First Stage 12V to 3.3V

V_{U31_IN}	11.996 V
V_{U31_OUT}	3.299 V
I_{U31_IN}	575 mA
I_{U31_OUT}	2.091 A

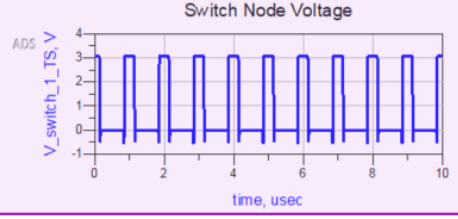
V_{U115}	3.289 V
I_{U115}	2.0 A

PI-CEMI

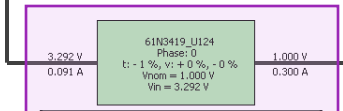
12 V to 3.3 V DC-DC Buck Converter



3.3 V to 1 V DC-DC Buck Converter

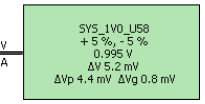


Second Stage 3.3V to 1V

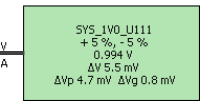


V_{U124_IN}	3.292 V
V_{U124_OUT}	1.0 V
I_{U124_IN}	91 mA
I_{U124_OUT}	300 mA

Load

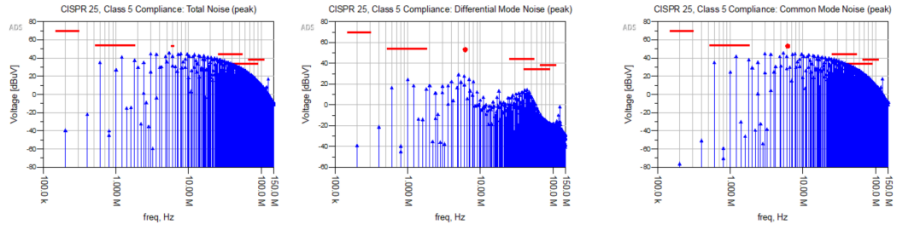


V_{U58}	0.996 V
I_{U58}	150 mA



V_{U111}	0.995 V
I_{U111}	150 mA

Conductive EMI



R. Sercu and H. Barnes, "DC IR Drop Steady State Estimate for Cascaded Switching Regulators", *2023 IEEE 27th Workshop on Signal and Power Integrity (SPI)*, Aveiro, Portugal.

Agenda

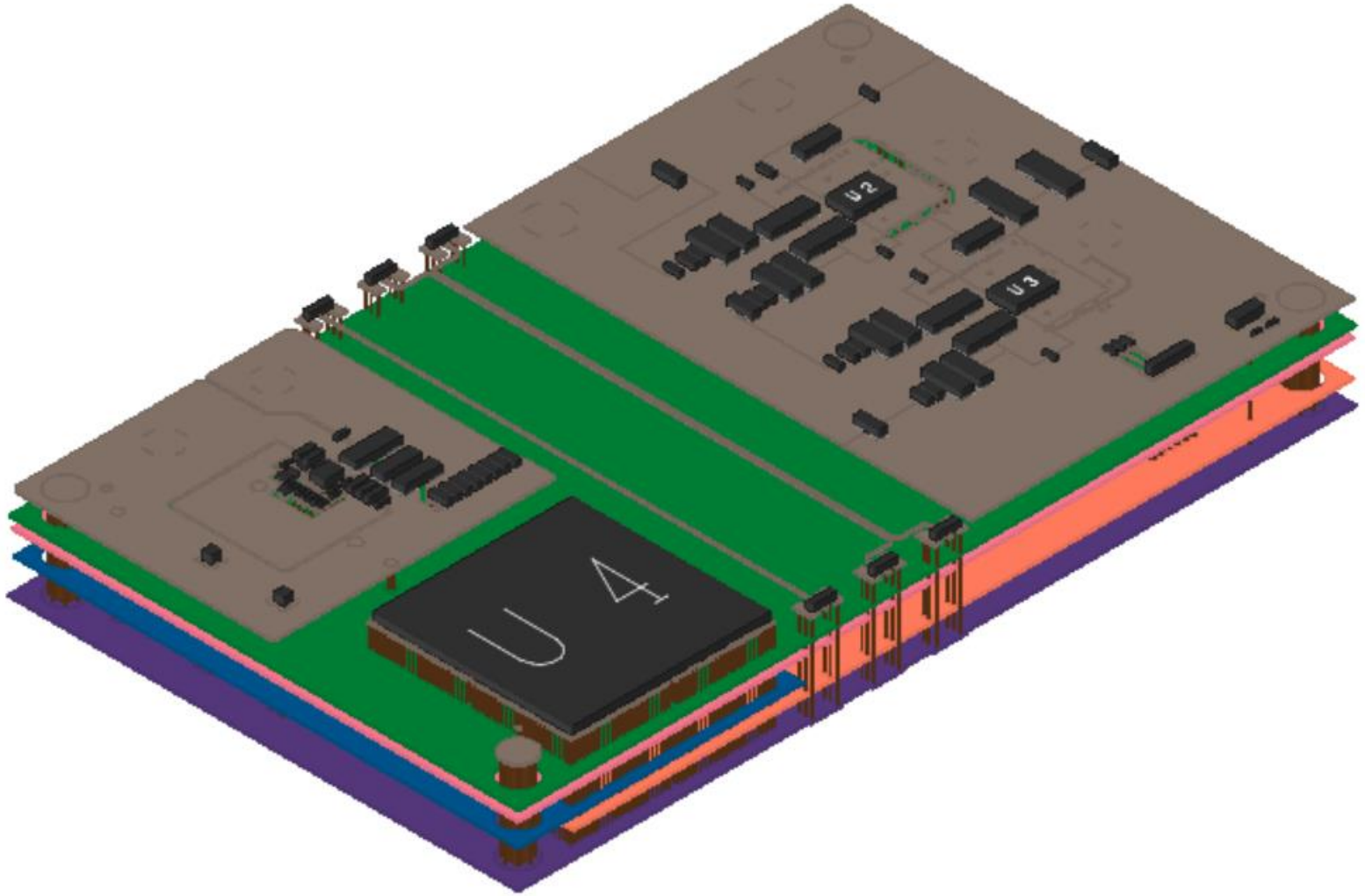
- **The Noise Challenge with 1000 Amps per Nanosecond**
  - *Learn how to use Harmonic Balance for non-linear PI Digital Twin simulations*
- **Conducted EMI – DC/DC Converter Noise Source**
  - *Learn how automation is simplifying complex dc/dc converter EMI simulations*
- **Crosstalk/Ground Bounce – Dynamic Sink Noise Source**
  - *Learn how to separate ground bounce from net-to-net power rail crosstalk*

New for ADS 2025 Update 2

Dynamic Sink Demo Board

Picotest LTC7151 LTC7132 PDN “EMI/Crosstalk” Demo Board

PCB with multiple power nets and ground are sensitive to EMI caused by crosstalk and ground bounce

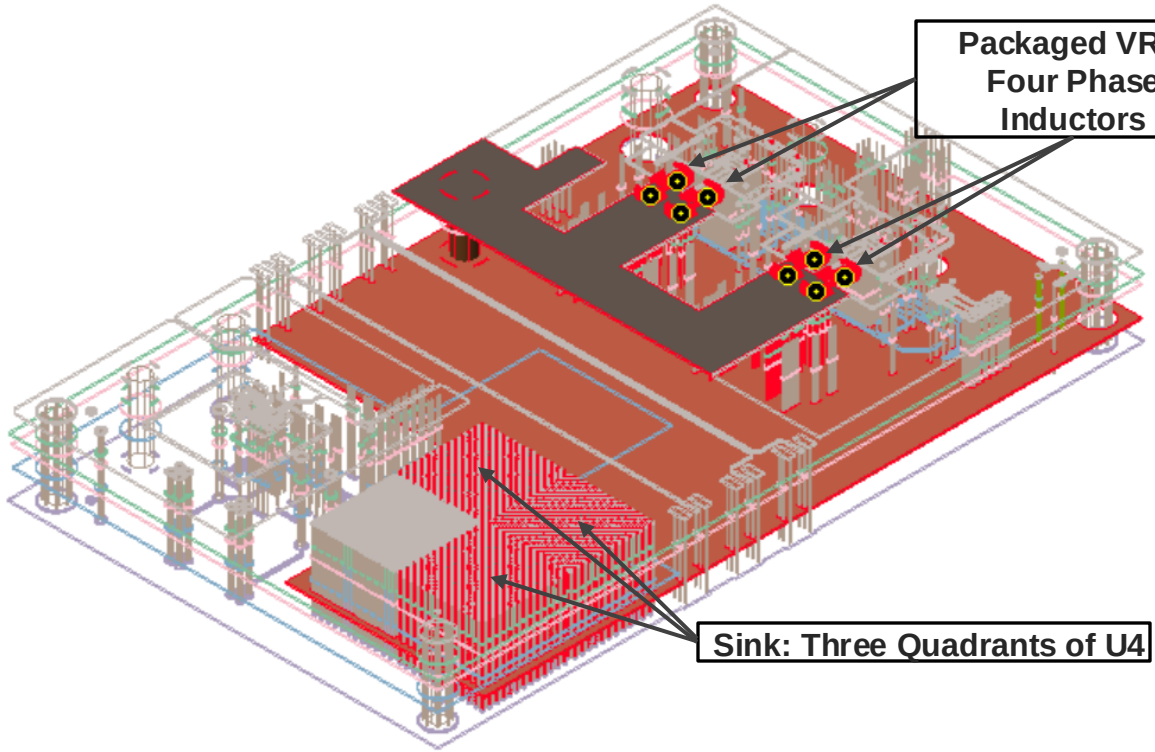


Dynamic Sink Demo Board

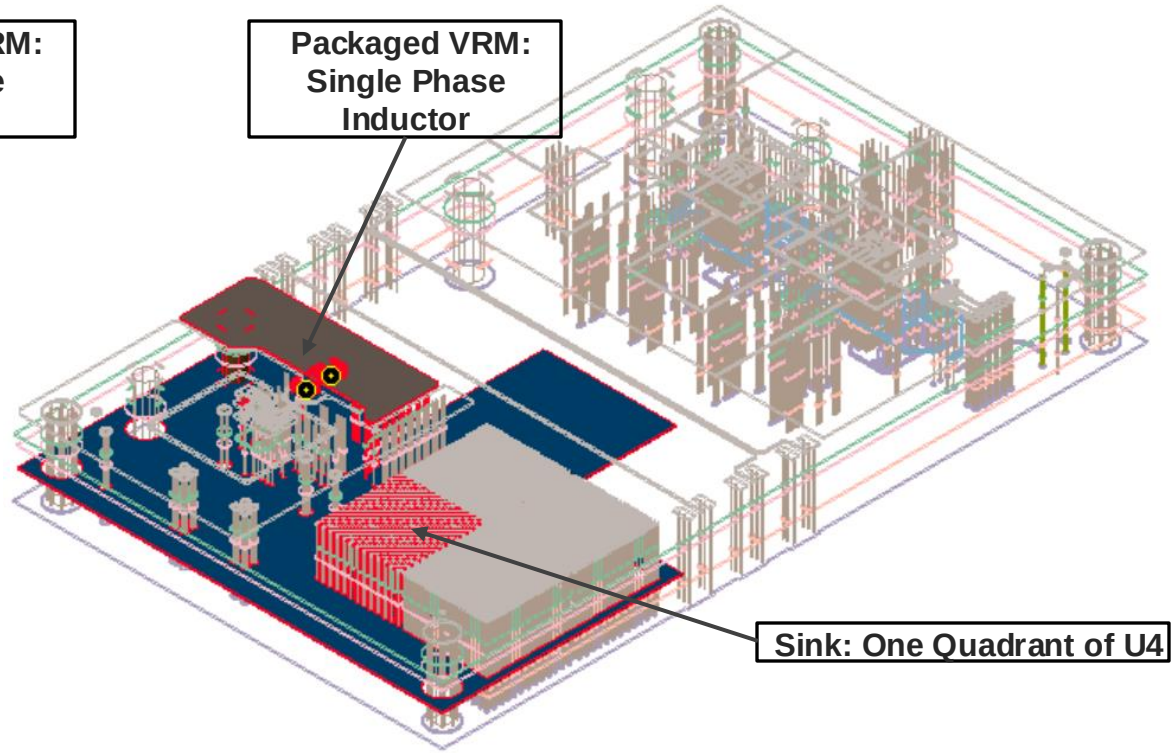
Test case with a dynamic high current, low voltage aggressor power rail adjacent to a low power victim power rail in the FPGA Sink.

Power Nets

Aggressor
Power Rail



Victim
Power Rail



Aggressor Power Net (VOUT_2) 0.85 V
Dynamic Sink Model – 50 Amp
Risetime: 10 ns
Hold Time: 100 ns
Period: 1 us

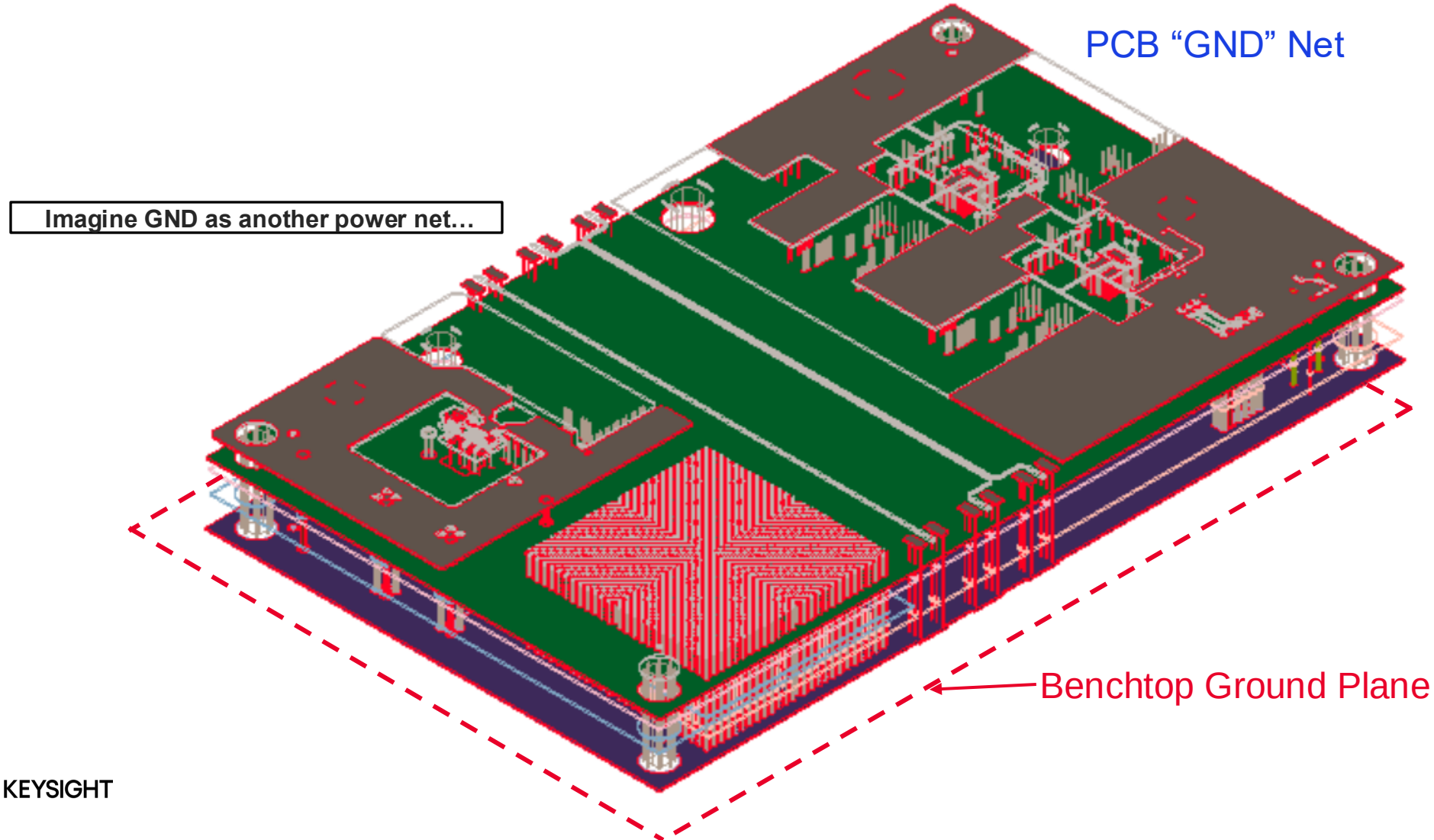
Victim Power Net (Vout_1) 1.0 V
Static Sink Model – 5 Amp

KEYSIGHT

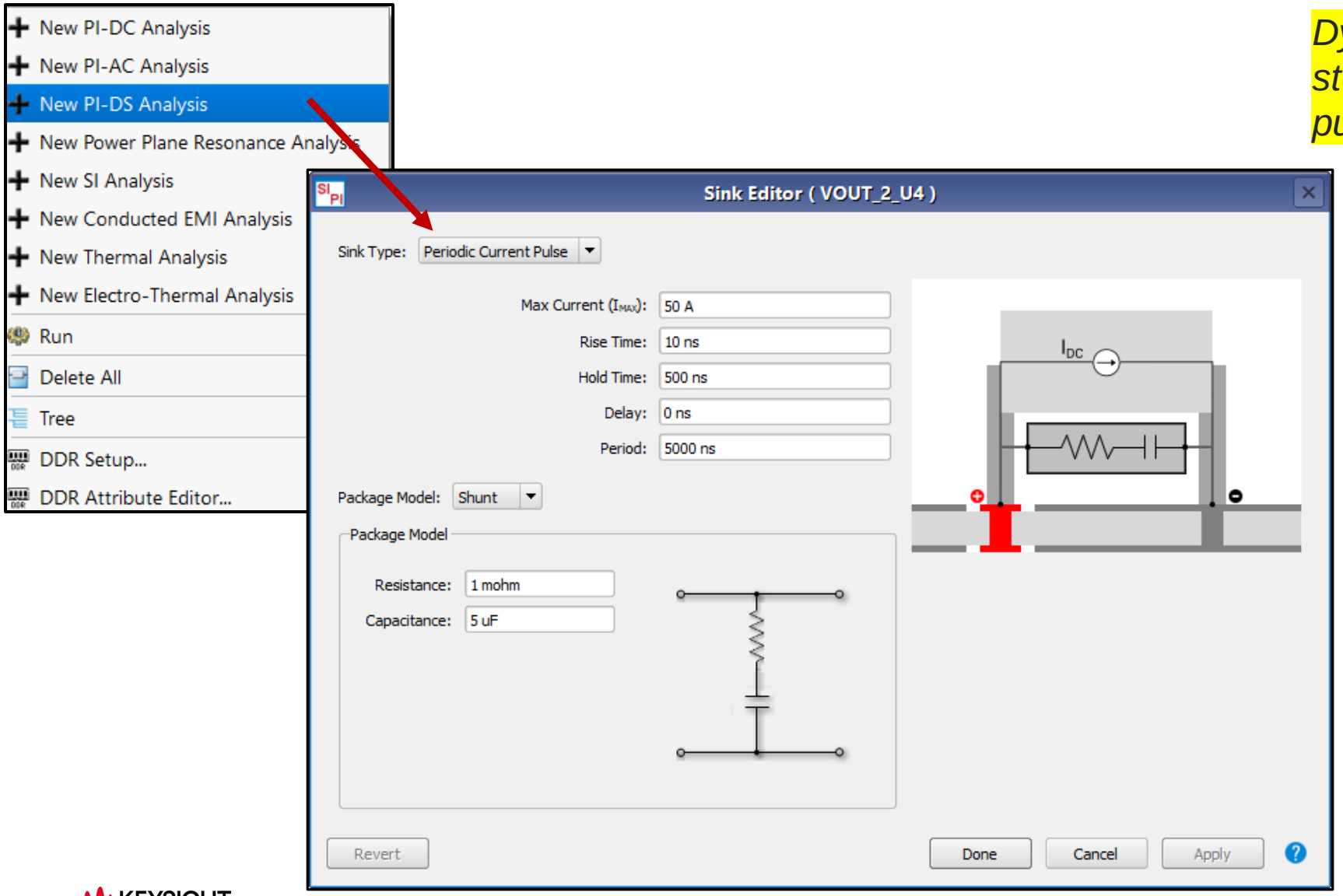
Voltage Ripple Probes

Probing Voltage on Ground Net <u>Relative to 'Benchtop' Ground Plane</u>

To see the net-to-net crosstalk separate from same net ground bounce the simulator must add a "benchtop" reference ground plane. Differential and Common Mode data.



PIPro EM Dynamic Sink Analysis (PI-DS) Enables New Current Pulse Sink



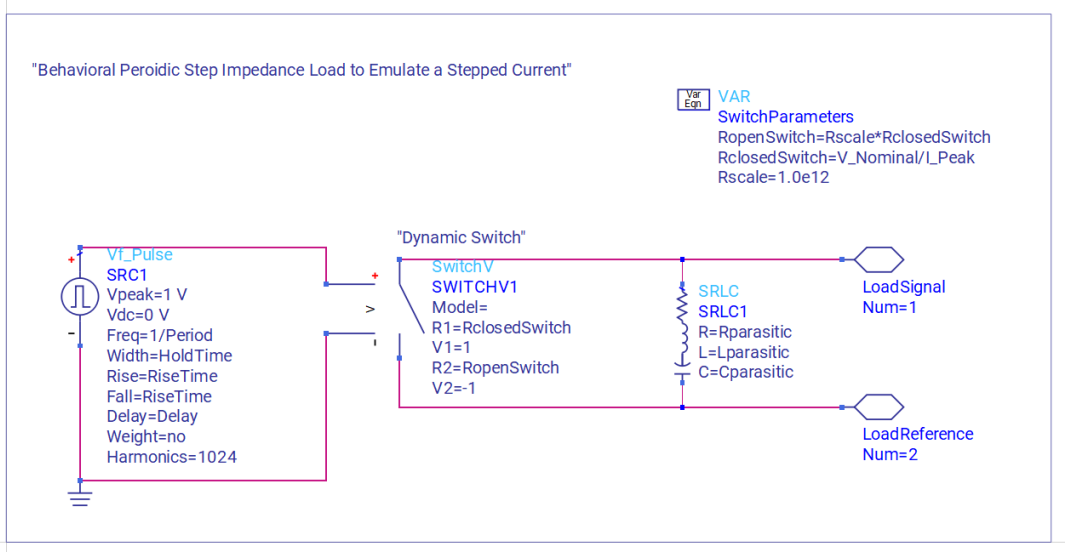
Dynamic Sink mimics transient load step measurements. A repetitive pulsed on/off step load.

Sink Type:
New Periodic Current Pulse

- Max Current
- Rise Time
- Hold Time
- Delay
- Period

Package Model
New RC shunt

The Dynamic Sink Transient Load Step is Periodic for HB

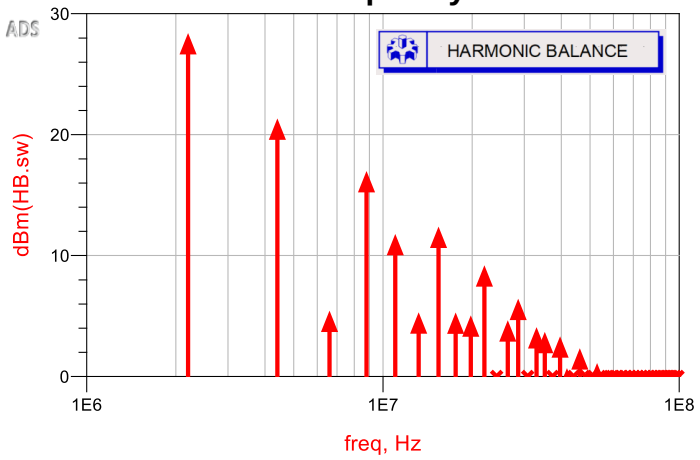


The Dynamic Step Load is modeled by a resistive switch with parasitics that runs fast with a Harmonic Balance simulator

---

Harmonic Balance
simulates harmonics of the switching frequency.
Only 255 Frequencies for steady state ripple!

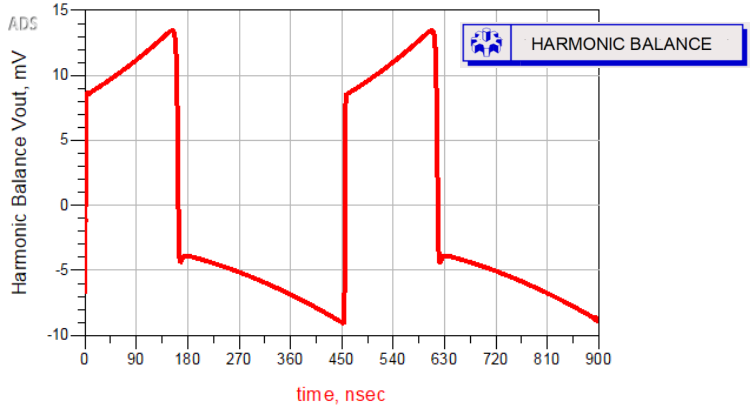
Simulate in Frequency Domain



Frequency Domain
Harmonic Balance Sim
iFFT jumps to Steady State

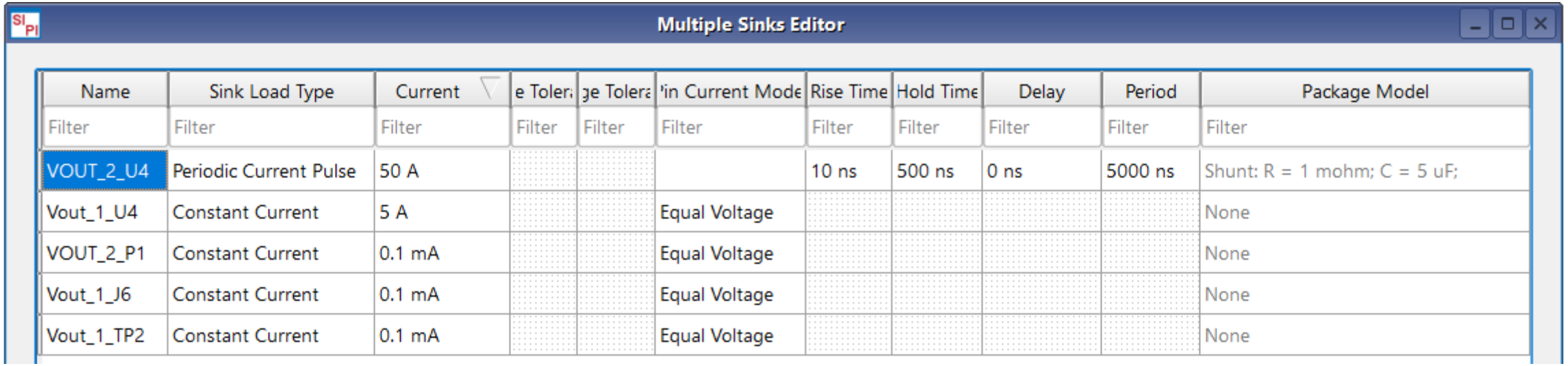
Seconds, Minutes, Hours

iFFT for Steady State Time Domain



Sink Ports Dynamic Voltage and Current Differential Data

Simulation data at a sink port is differential data with delta voltage between the power and return ground net.



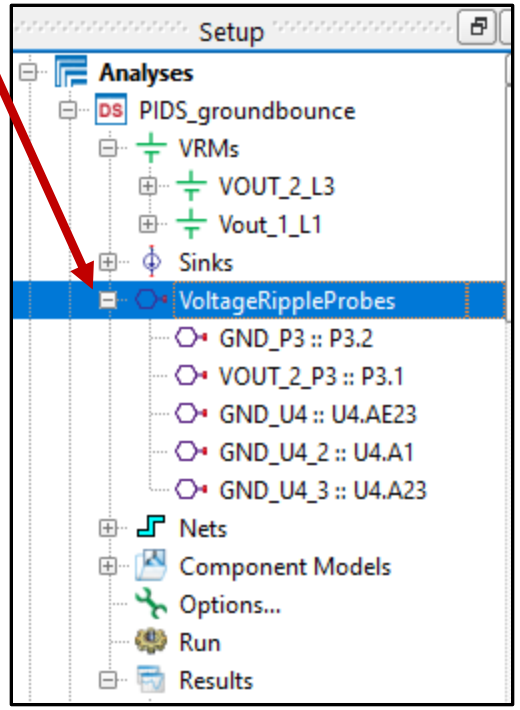
Name	Sink Load Type	Current	e Toler	ge Tolera	in Current Mode	Rise Time	Hold Time	Delay	Period	Package Model
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
VOUT_2_U4	Periodic Current Pulse	50 A				10 ns	500 ns	0 ns	5000 ns	Shunt: R = 1 mohm; C = 5 uF;
Vout_1_U4	Constant Current	5 A			Equal Voltage					None
VOUT_2_P1	Constant Current	0.1 mA			Equal Voltage					None
Vout_1_J6	Constant Current	0.1 mA			Equal Voltage					None
Vout_1_TP2	Constant Current	0.1 mA			Equal Voltage					None

- *A PIDS Analysis will measure ripple voltage and ripple currents at each sink.*
- *A sink can be added with a mA of current to act as a measurement probe point between two nets such as power and ground.*
- *This is a differential measurement.*

PIPro PI-DS Voltage Ripple Probes

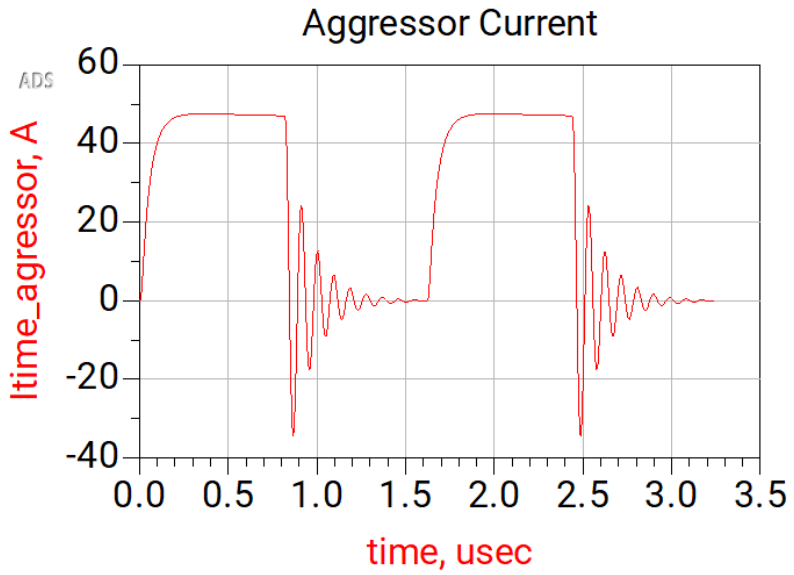
Simulation data at a Voltage Ripple Probe is common mode data referenced to a virtual bench top ground plane.

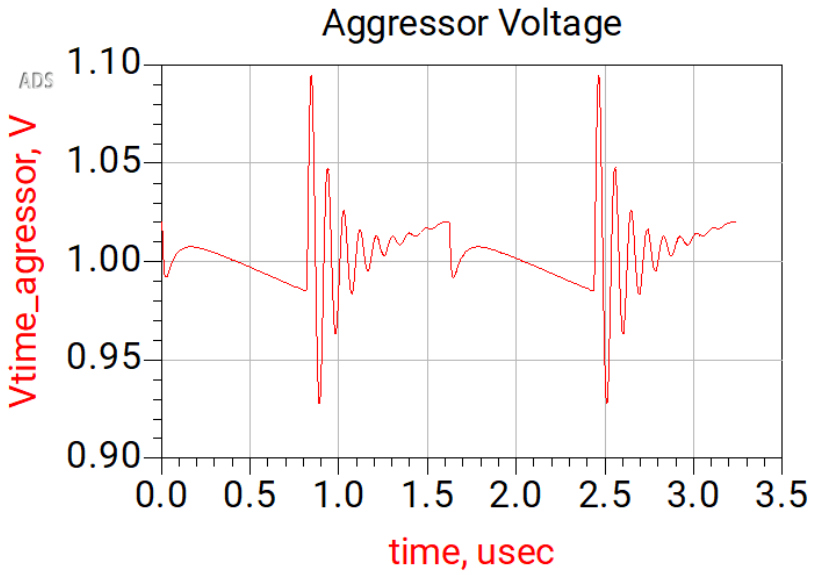
New VoltageRippleProbes in the PIDS Analysis

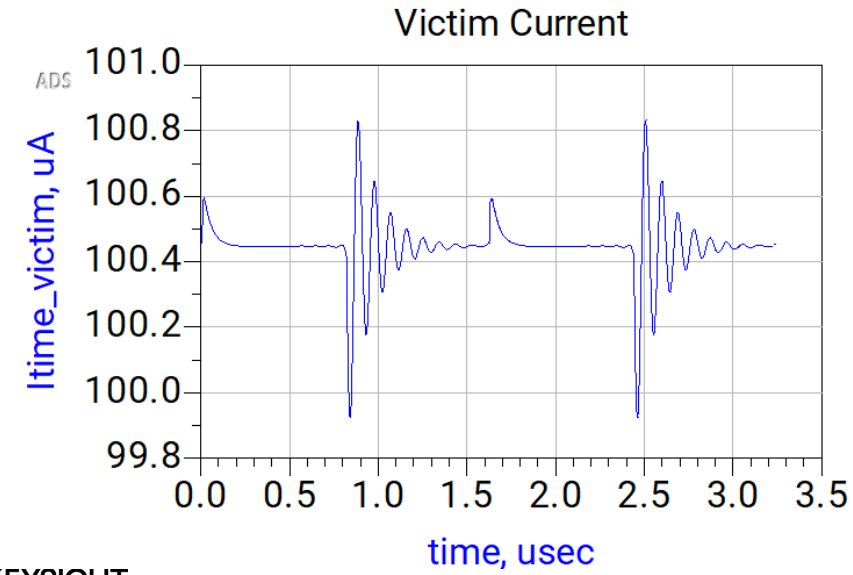


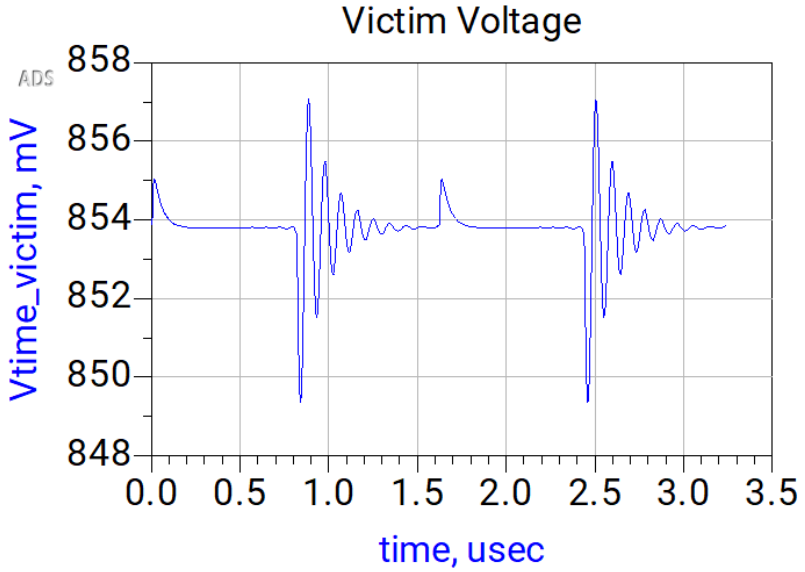
- Single Pin Measurement Points
- Data is a Common Mode Measurement made relative to benchtop ground
- Ideal for separating “ground bounce” from net-to-net crosstalk.

PIPro Dynamic Sink (PI-DS) Aggressor and Victim Sink Results Data







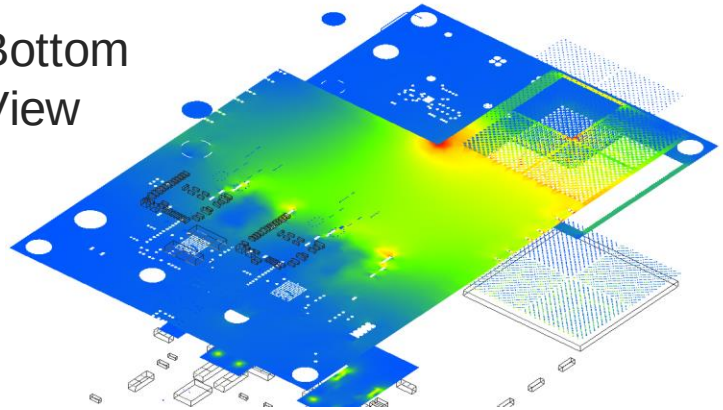


The results from a PIPro Dynamic Sink Analysis clearly show crosstalk from the aggressor sink to a victim sink.

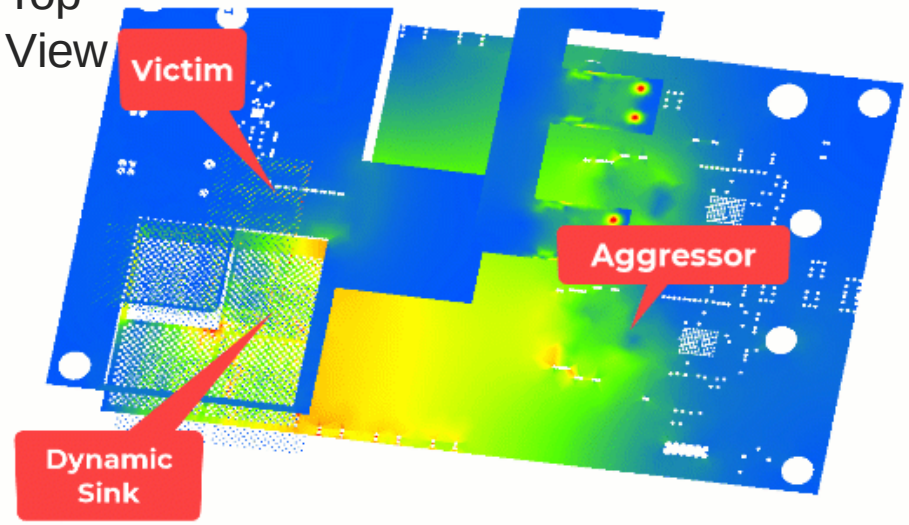
Power Integrity Power Net to Power Net Crosstalk

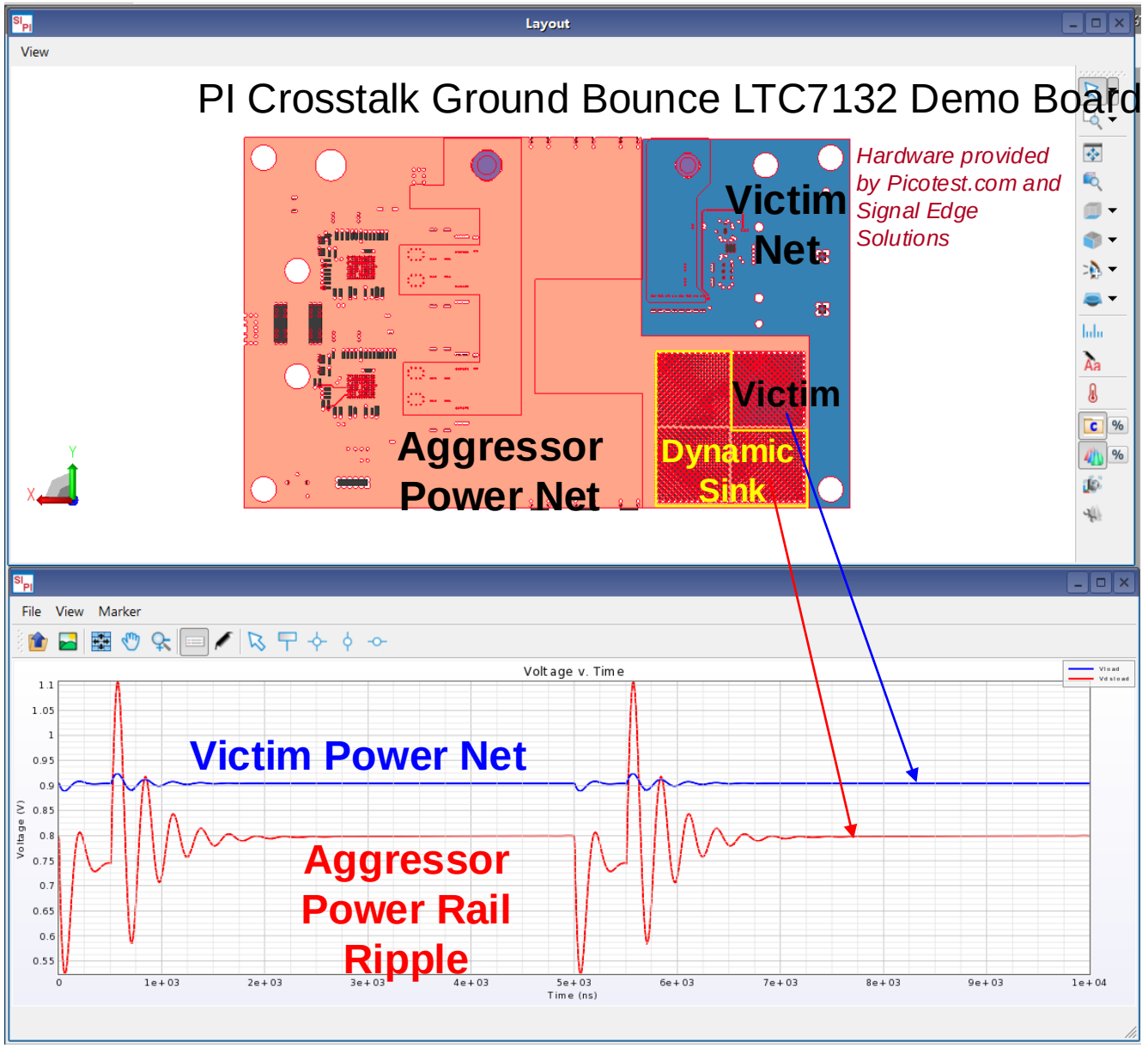
Field visualization helps locate the worst-case location for net-to-net crosstalk

Bottom View



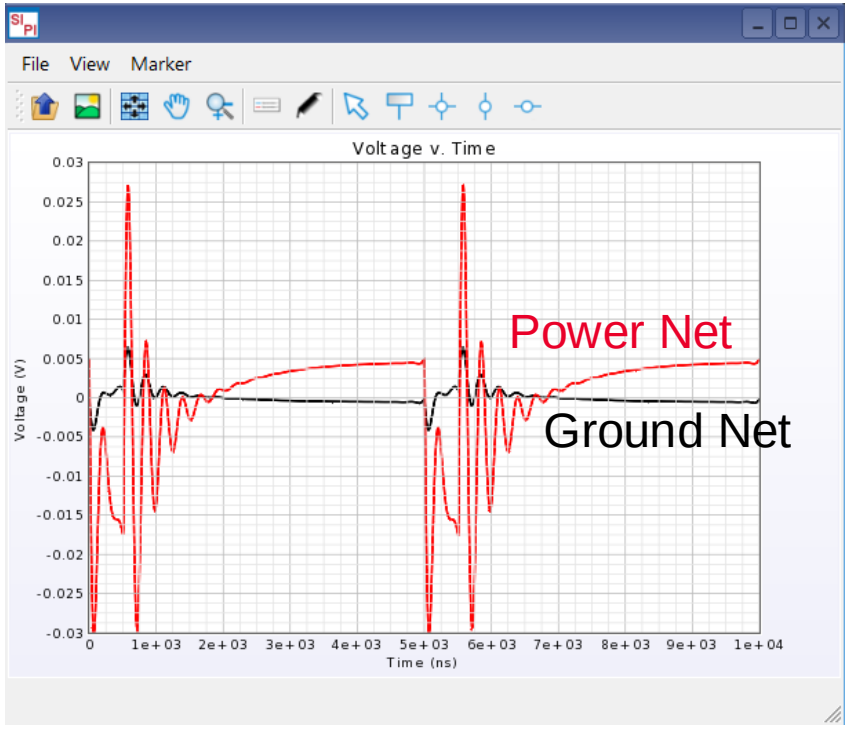
Top View

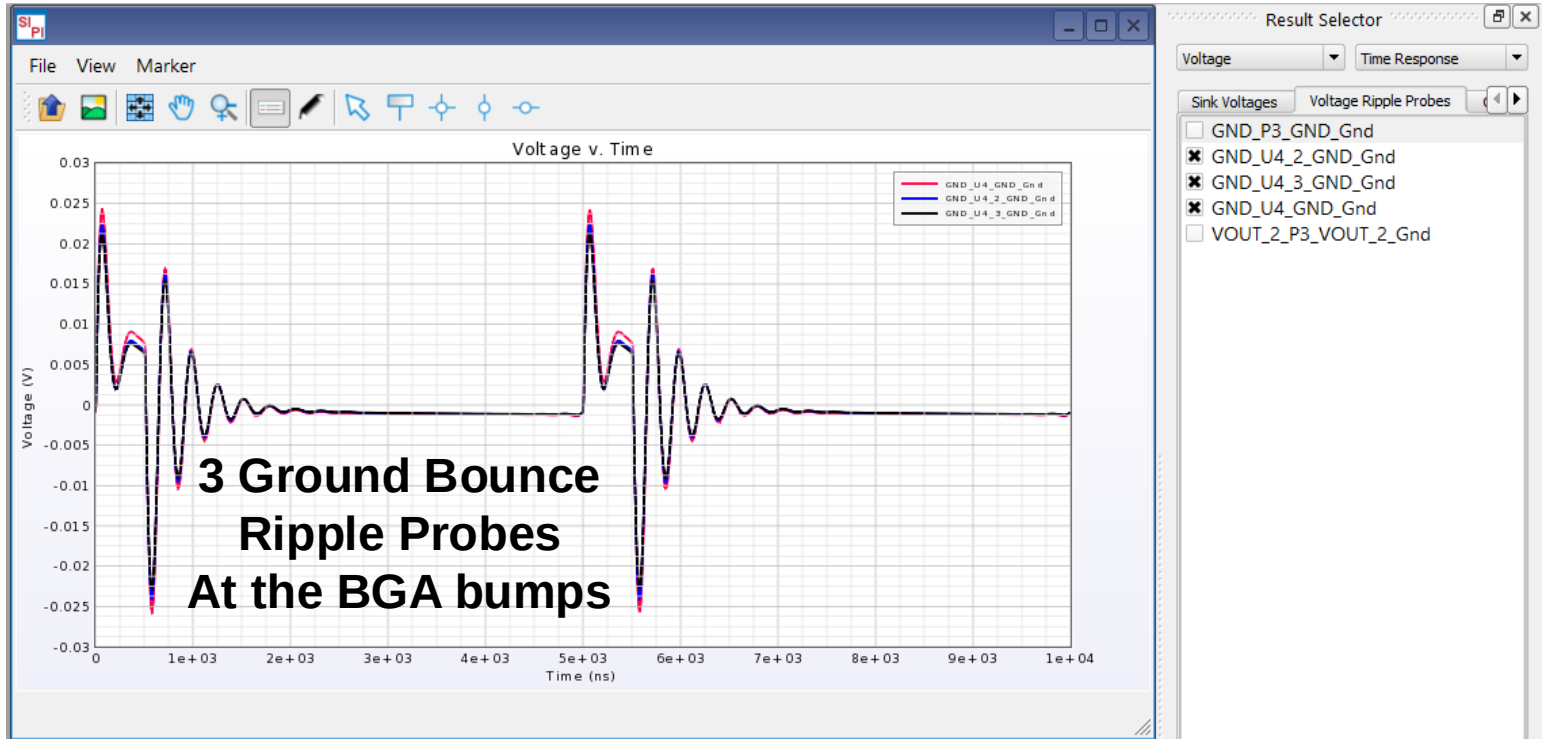




PIPro PIDS Ripple Probes Aggressor and Victim Ground Locations

Ground bounce is the noise ripple on a shared ground net caused by the aggressor return current. Voltage Ripple Probes make it possible to simulate Ground Bounce data.

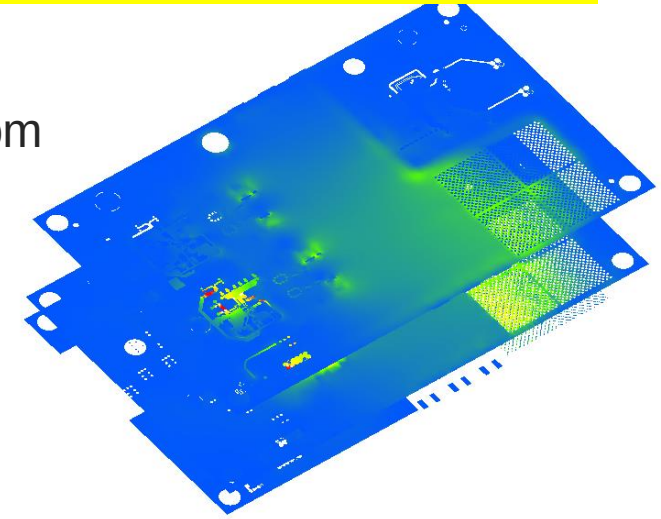




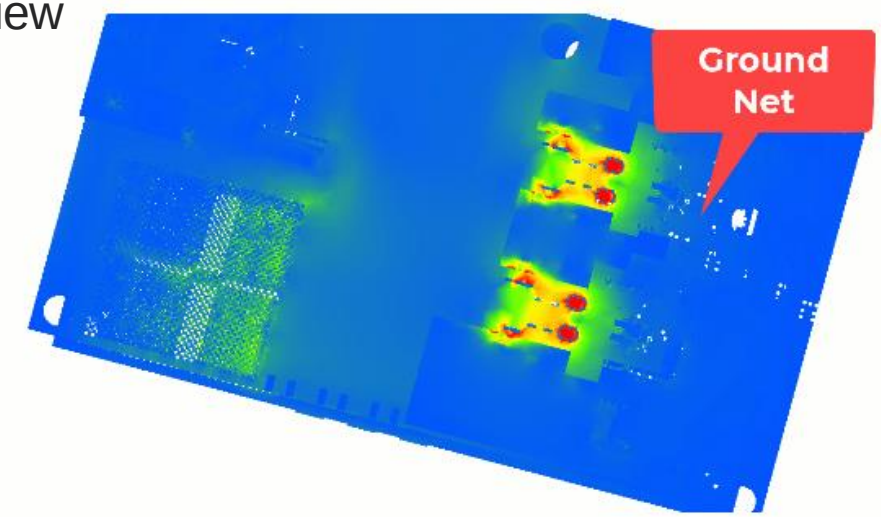
Power Integrity Dynamic Sink Ground Bounce

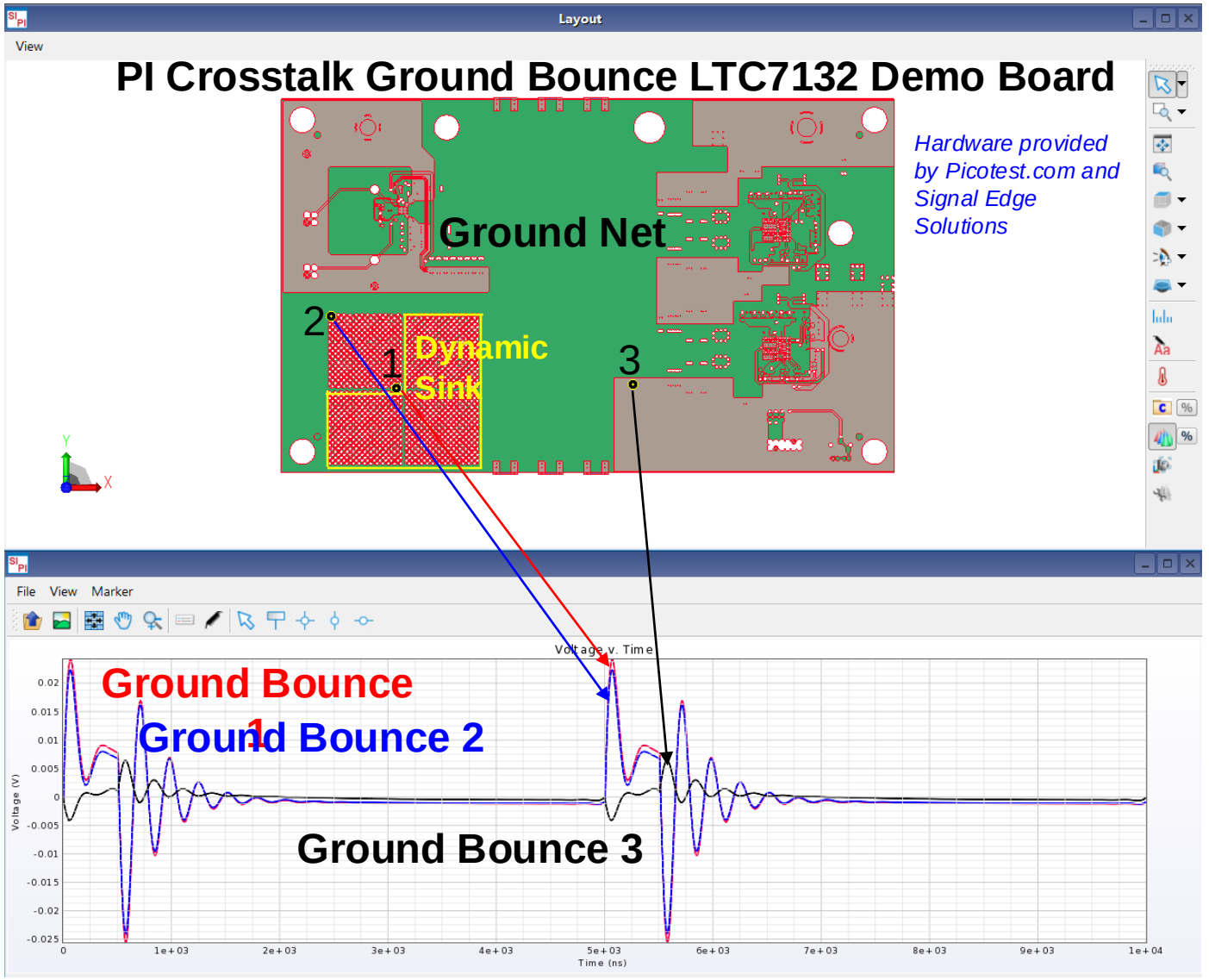
Field visualization helps locate worst case locations for ground bounce issues.

Bottom View



Top View

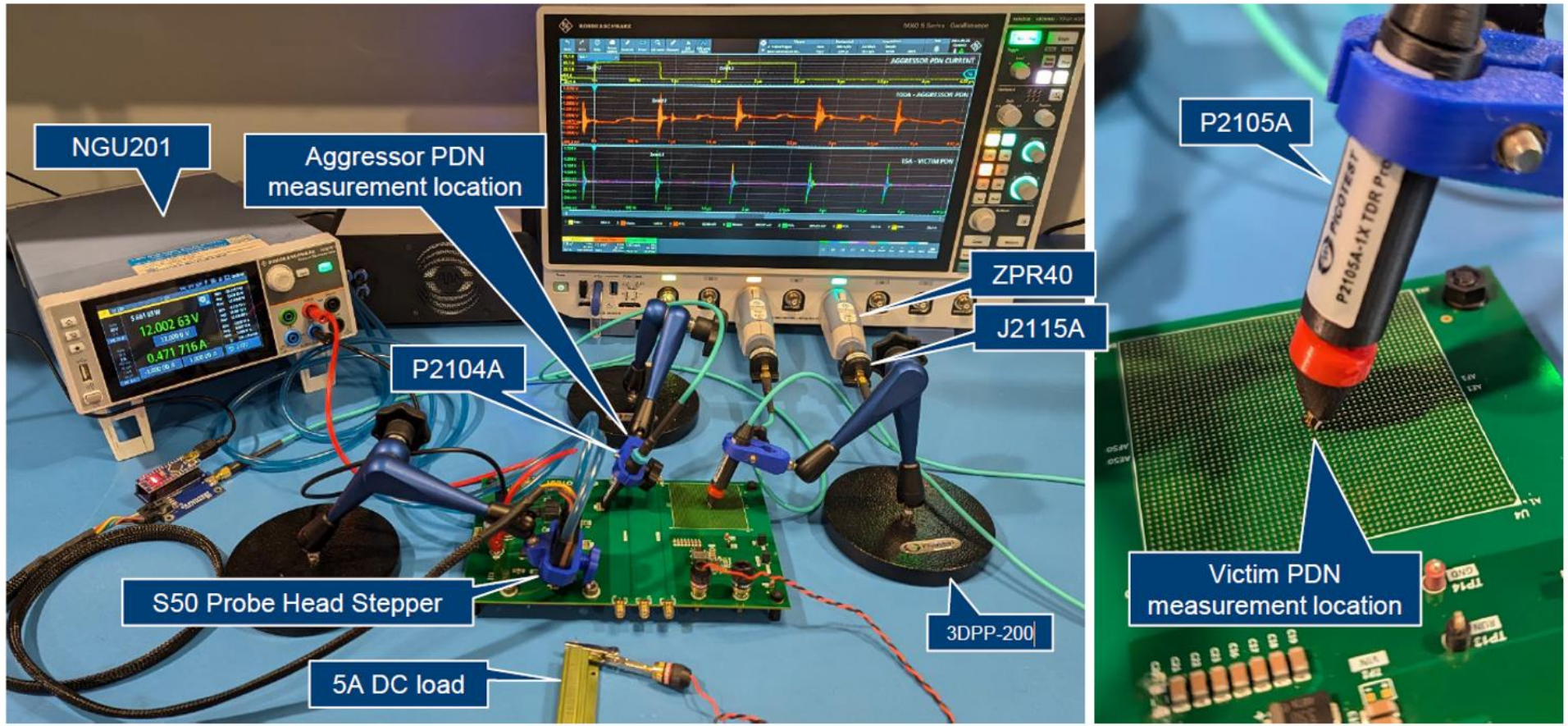




Measurement Setup by Signal Edge Solutions

Picotest Demo Board for Load Stepper Crosstalk Demonstration. Initial measurement done with S50 Current Injector at P1 Connector

PDN CROSSTALK MEASUREMENT SETUP

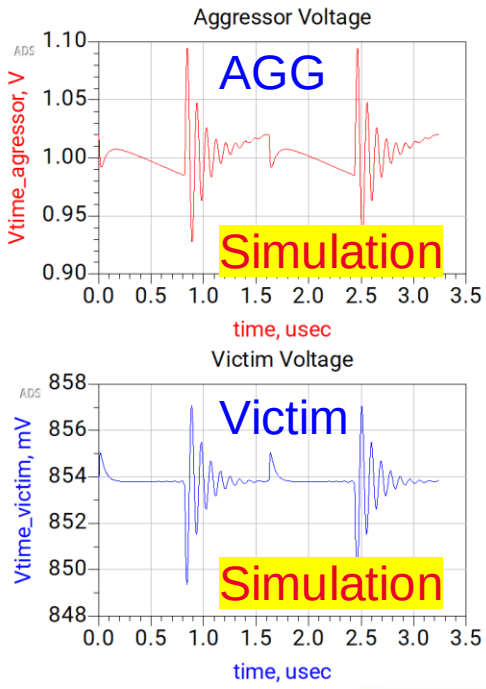


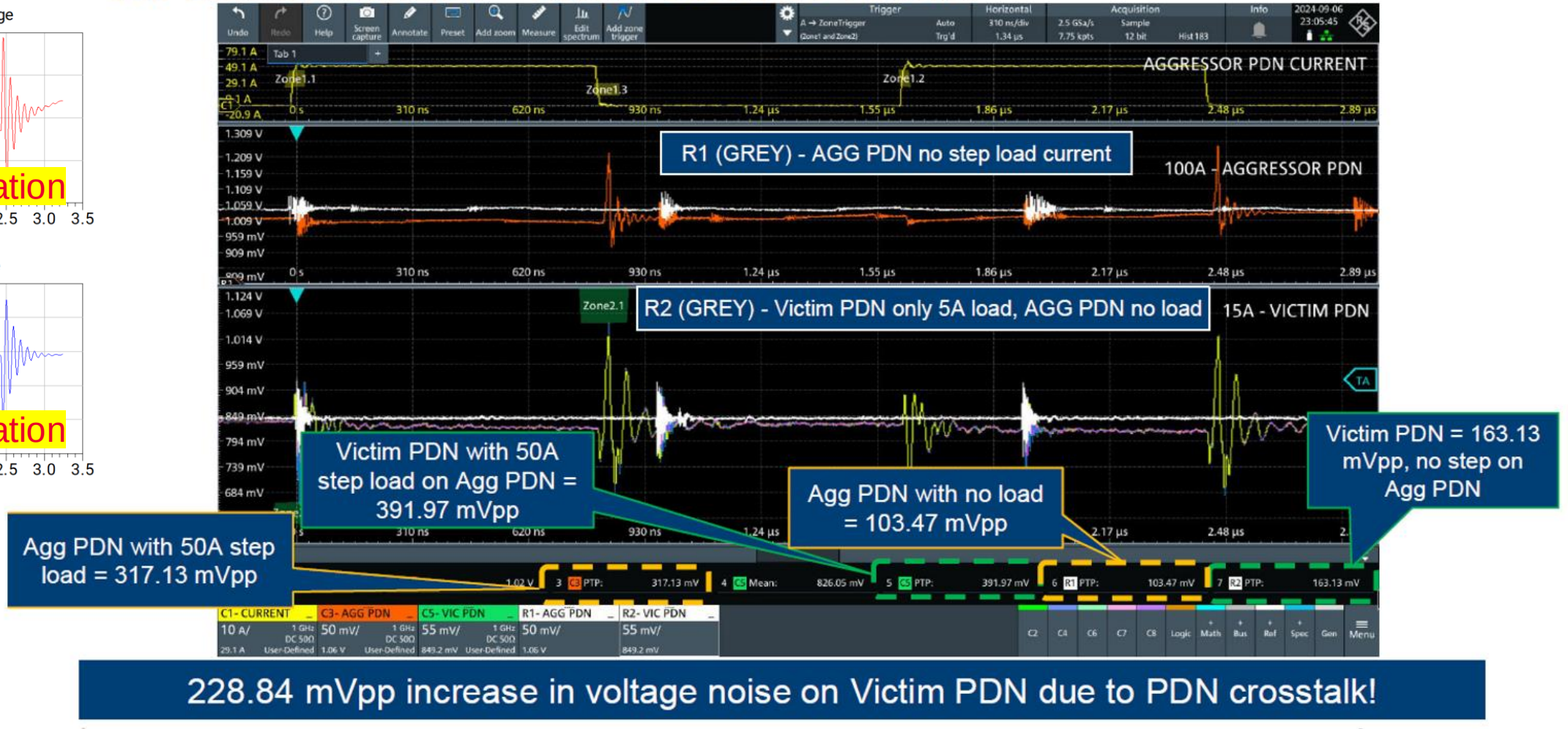
Picotest S50 Demo Board | Signal Edge Solutions

Measurement Results by Signal Edge Solutions

Simulation and Measurement agree worst case noise is at load current turn-off, not step load turn-on.

PDN CROSSTALK – 50A PULSED LOAD

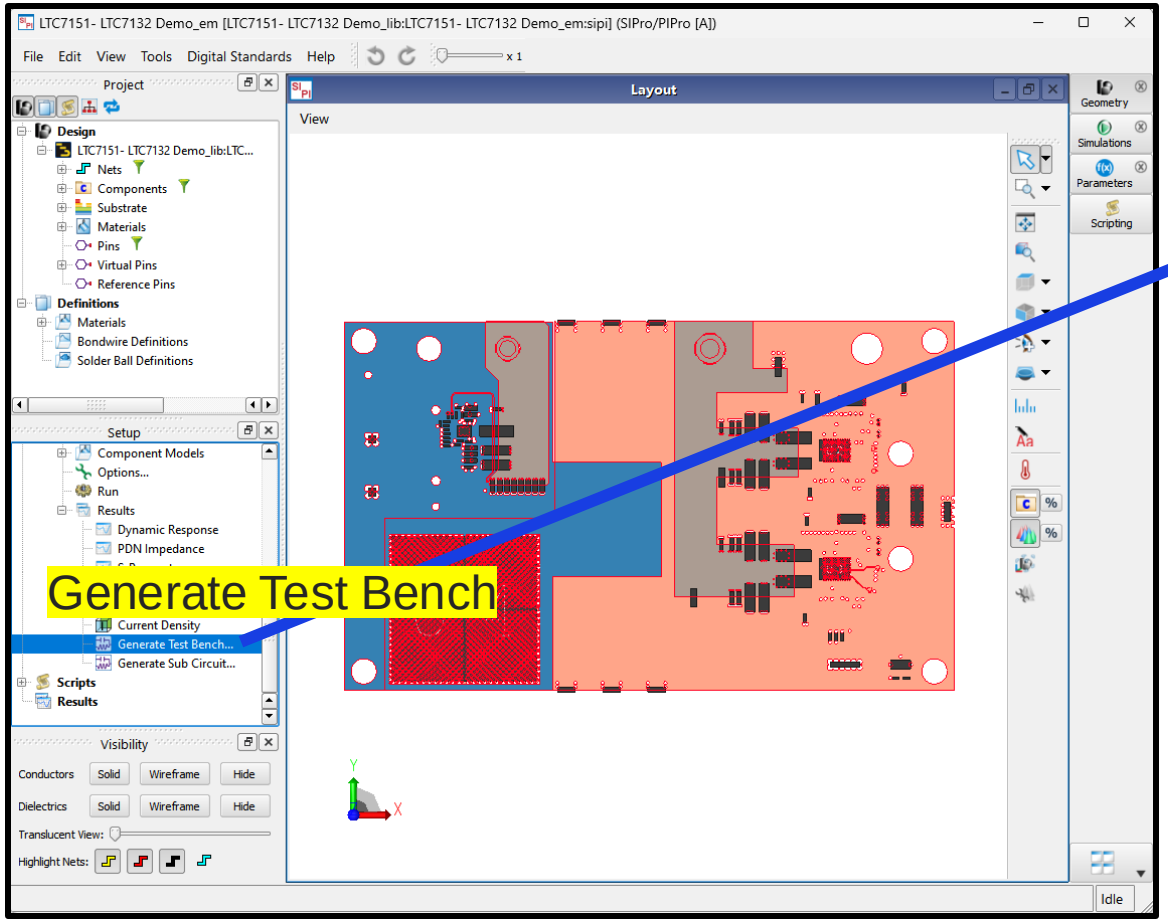




228.84 mVpp increase in voltage noise on Victim PDN due to PDN crosstalk!

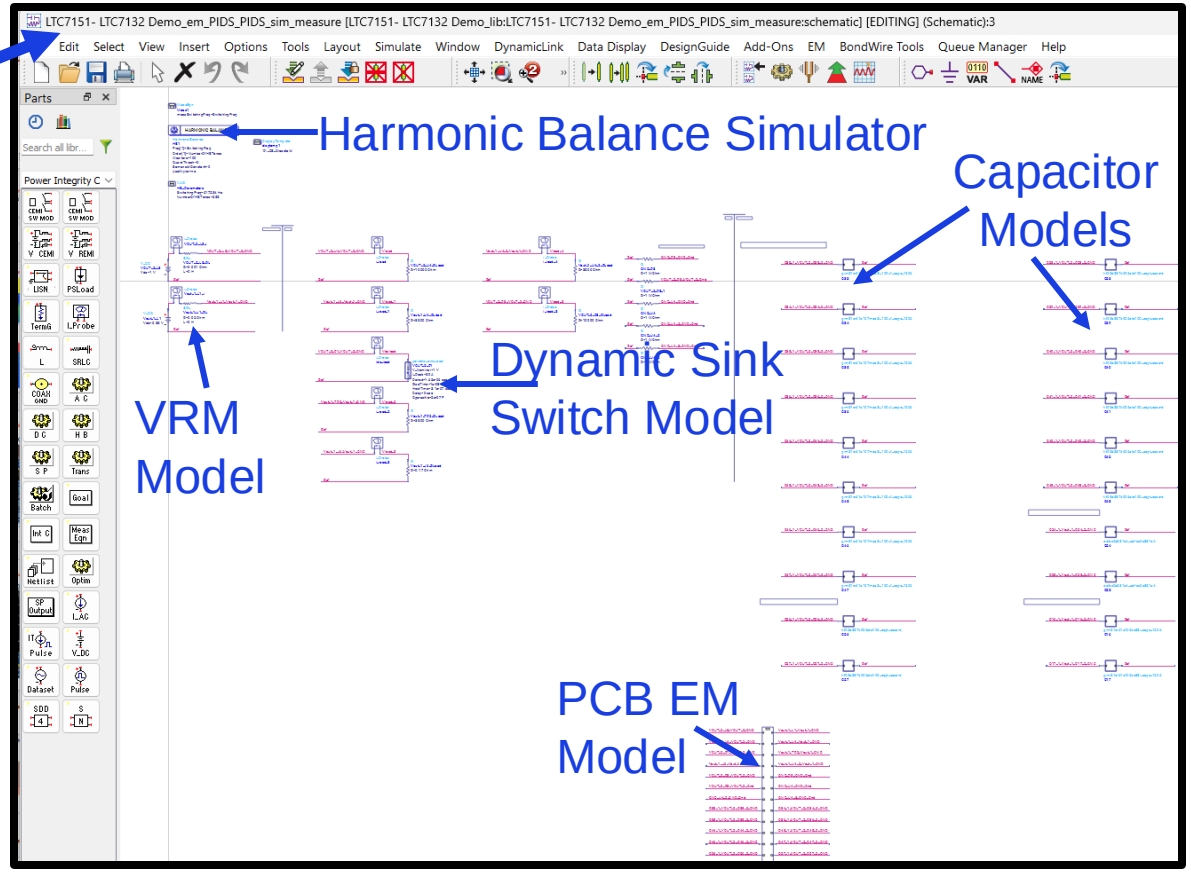
Bonus – PI-DS Analysis Exports a Test Bench to ADS Schematic

ADS PIPro EM Simulator



Auto-generated test bench in ADS schematic enables optimization and additional model flexibility.

ADS PI-DS Test Bench Schematic Simulation



SUMMARY

- **Digital Twin End-to-End Power Integrity Simulations**

  The next revolution of AI and Cloud Compute is accelerating the need for end-to-end digital twin PDN simulations that include dynamic sink simulations to look at crosstalk and ground bounce.

  - You learned how frequency domain harmonic balance is the fastest way to simulate non-linear power rail time domain noise with a digital twin schematic.

- **Automating the Switching Noise Conducted EMI Simulation**

  Common mode currents travel in the same direction on the power and ground nets resulting in EMI on the return path. “Ground is for potatoes and carrots; electrical currents have a return path”

  - You learned that automation has simplified the EM port setup and dc/dc switching noise source to automate the generation of a Conducted EMI Testbench with differential and common mode data.

- **Automating the Dynamic Sink Ground Bounce and Crosstalk Simulation**

  High di/dt 1000 Amp loads create crosstalk and ground bounce challenges with neighboring power nets and signal lines. Simulation saves time and money to avoid expensive hardware failures.

  - You learned the difference between net-to-net crosstalk and ground bounce for large di/dt step load transients.

Take the guesswork out of power delivery, test drive Keysight EDA ADS with PIPro today!

Basic Power Integrity Bundle W3623B

SI and PI Bundle W3626B

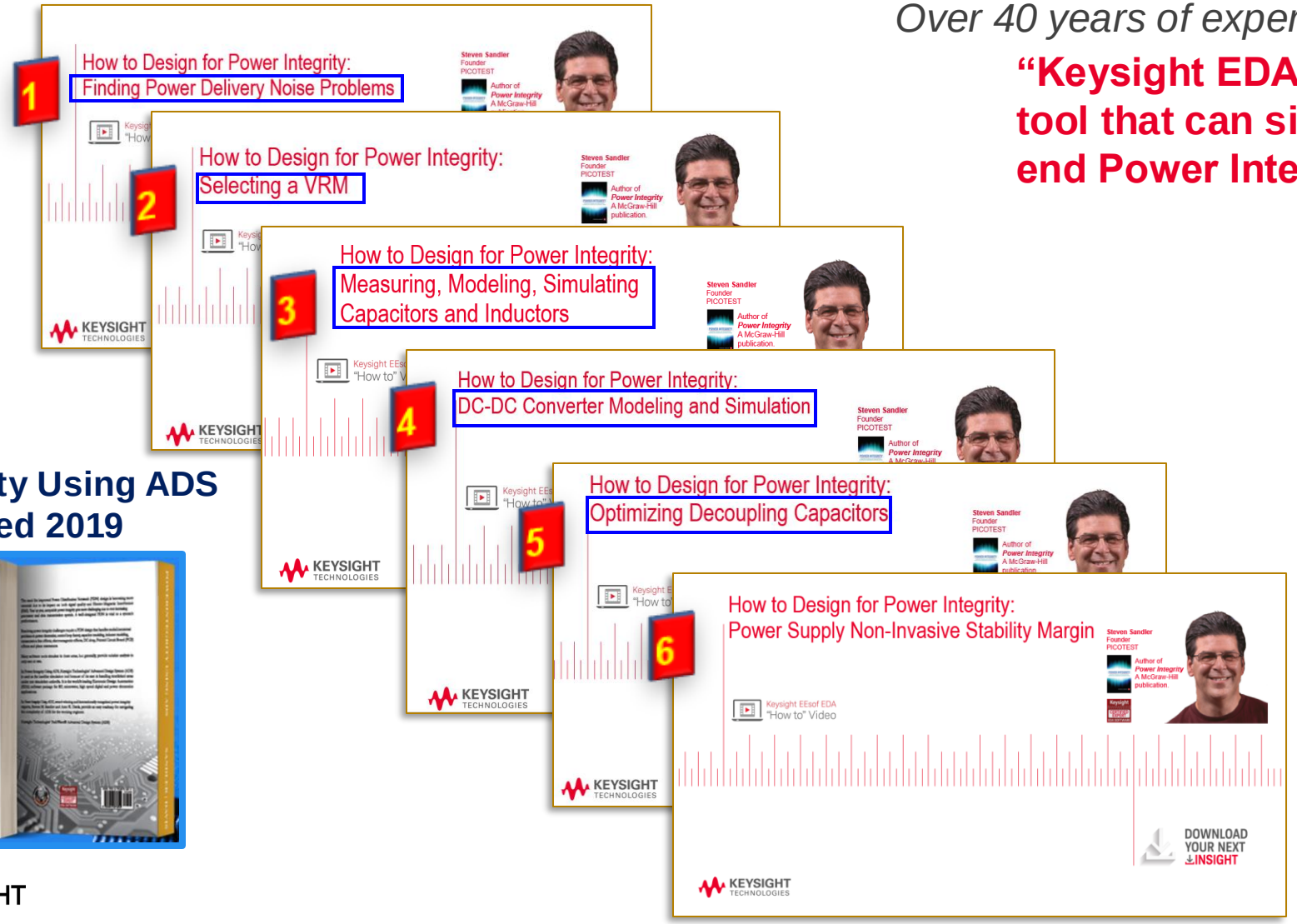
Conducted EMI Add-on for PIPro W3036E

PIPro Dynamic Sink Analysis starts shipping with ADS 2025 Update 2

ADS Power Integrity Keysight Learn Video Series with Workspaces

How to Design for Power Integrity

6 Part Series on YouTube



Steve Sandler, Founder of Picotest

Over 40 years of experience in Power Electronics

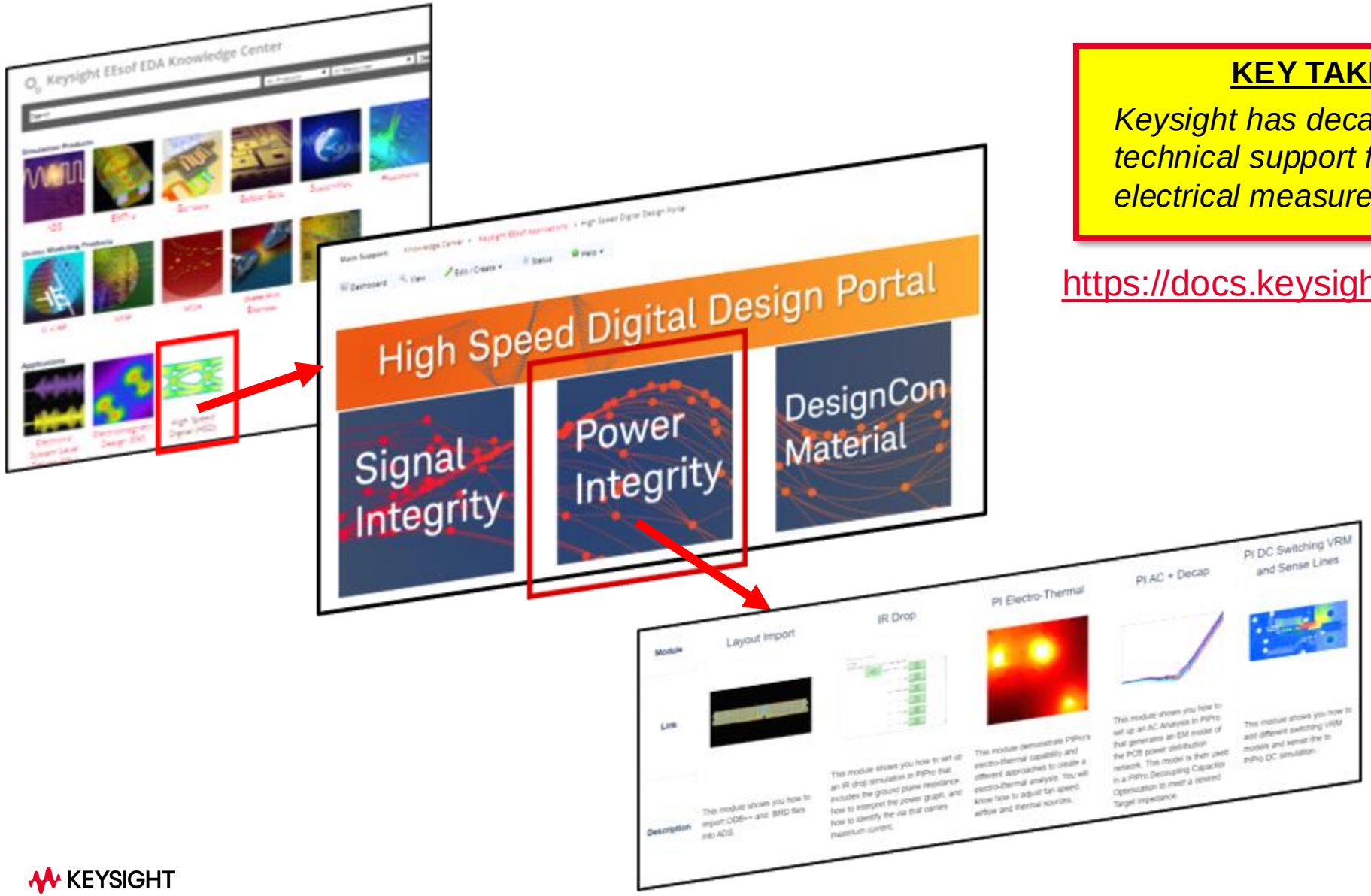
"Keysight EDA ADS is the only tool that can simulate the end-to-end Power Integrity Ecosystem"

Power Integrity Using ADS Published 2019

#6 NISM for 2023

KEYSIGHT

Knowledge Center Support for ADS Power Integrity



KEY TAKE AWAY

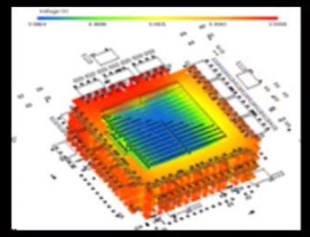
Keysight has decades of experience in technical support for EDA simulations and electrical measurements!

https://docs.keysight.com/display/support/KC

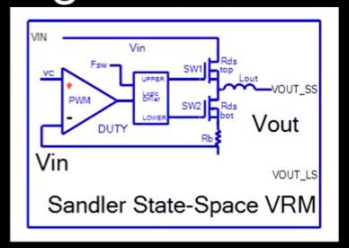
Power Integrity Digital Twin Workflow Automation

Automated Workflow with Dynamic VRM and Dynamic Sink Switching Noise Sources

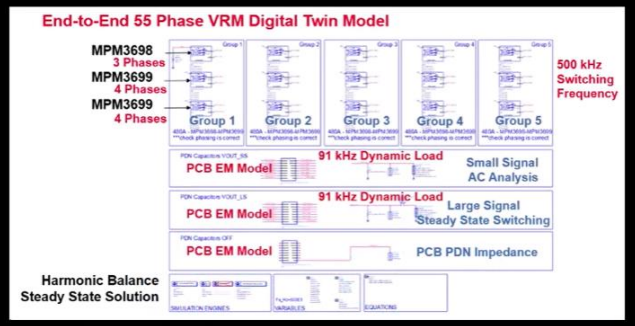
DC IR Drop



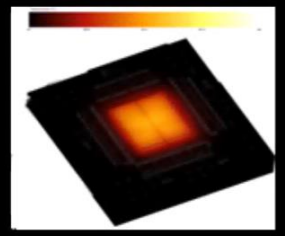
Regulator Model



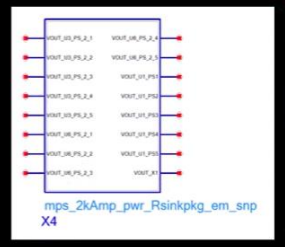
Power Delivery Digital Twin



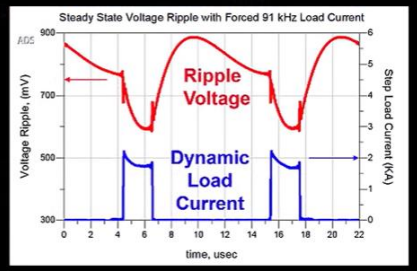
Electro-Thermal



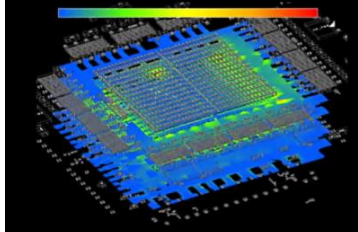
PCB EM Model



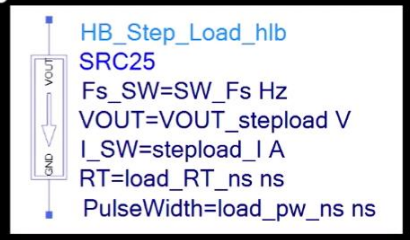
Worst Case Power Rail Ripple



Dynamic AC



Dynamic Load Model



Watch the short video

www.keysight.com/product/W3623B

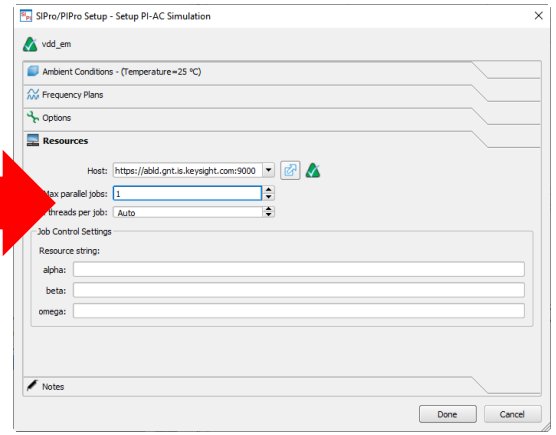
KEYSIGHT

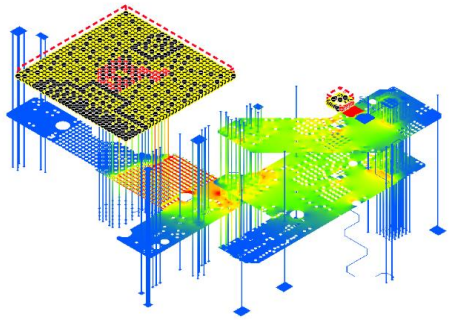
Thank you!

HPC Computing Works with PIPro AC

- Design: Xilinx ZCU104 board
- Setup:
  - VRM-VCCINT_L82, Sink-VCCINT_U1
  - Nets: GND, VCCINT
- Frequency Plan: Logarithmic – 10 kHz-300 MHz, 7/decade (33 Points)
- Threads per job = 16

PIPro Resources Setup





Metrics	Sequential	Parallel Jobs=2	Parallel Jobs=4	Parallel Jobs=8
Simulation Time (hh:mm:ss)	01:02:43	00:33:10	00:20:24	00:13:14
Factor	x	~2x	~3x	~4.7x

- *Data taken on ADS 2021 Update 2 (Turn-key Cloud Partner HPC)*
- *Sequential run computed on 512 GB, 16 core. (nc5)*
- *Parallel runs computed on 256 GB, 16 core for each parallel job. (n4)*
- *Master: 128 GB, 16 core. (ng2)*