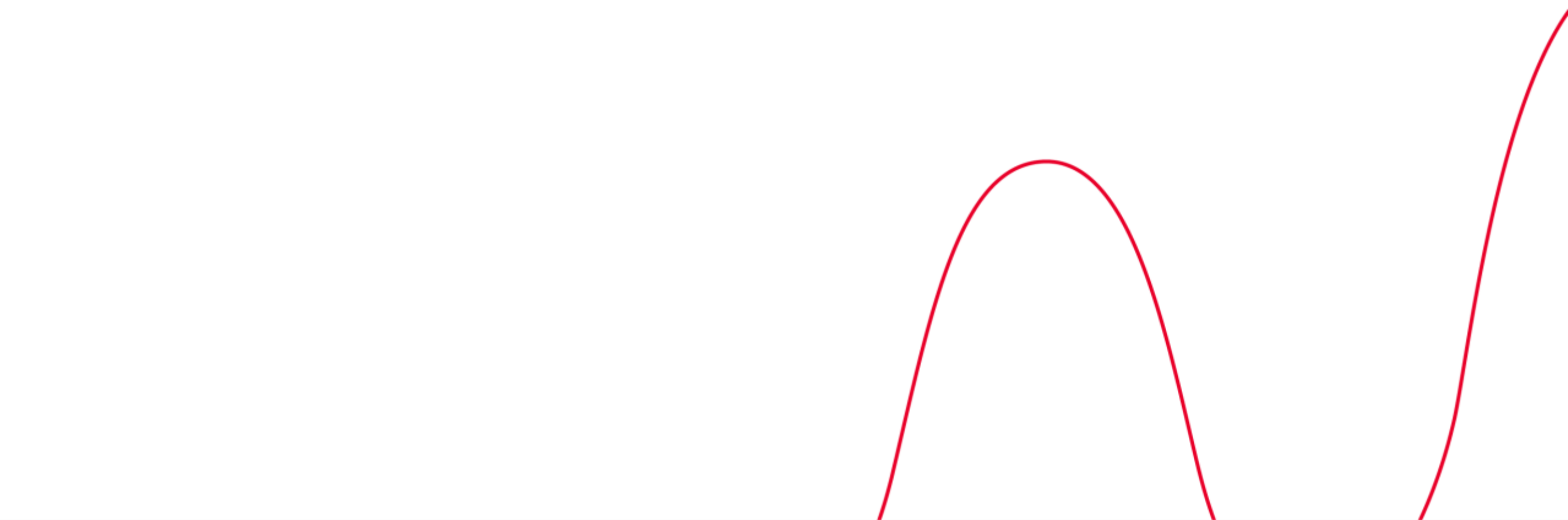


Validating Digital Error Performance of 1.6T Interconnects

A Framework for Success

September 2026

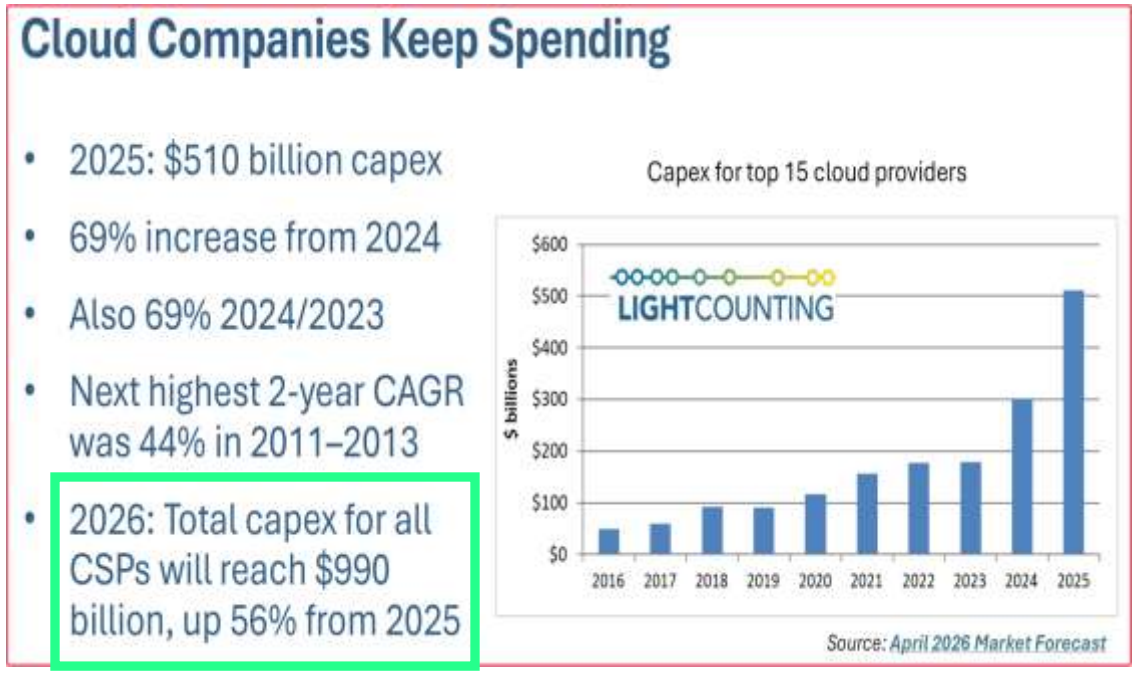
Market Trends and Drivers for High-Speed Interconnect Testing

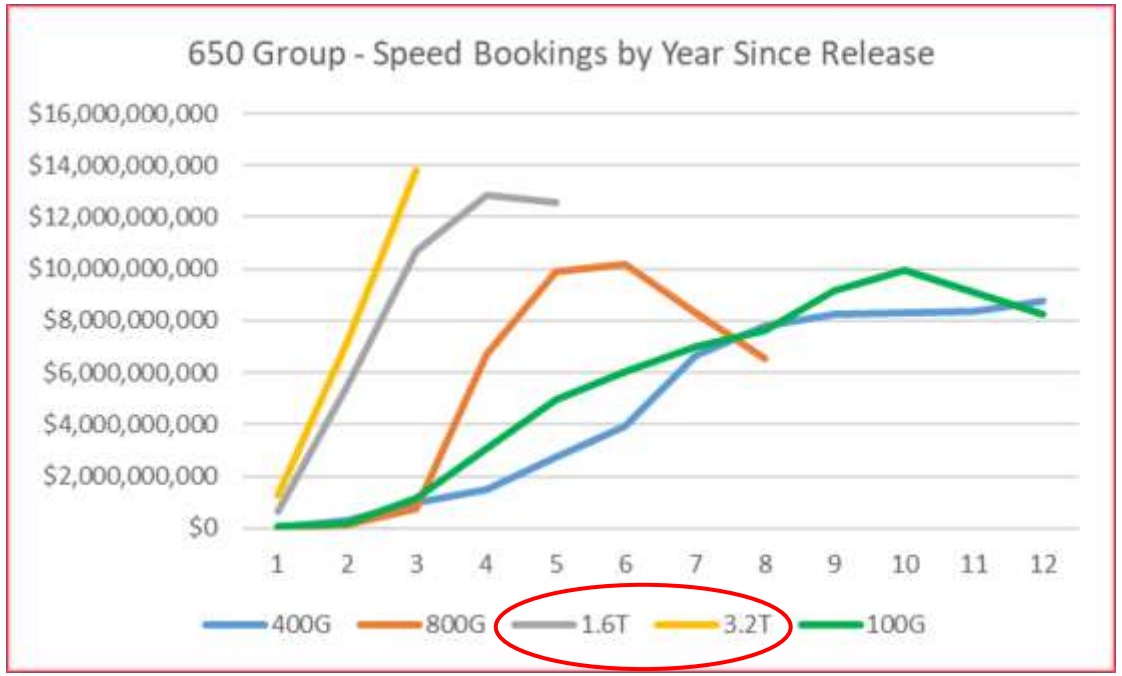


Interconnect Market Drivers

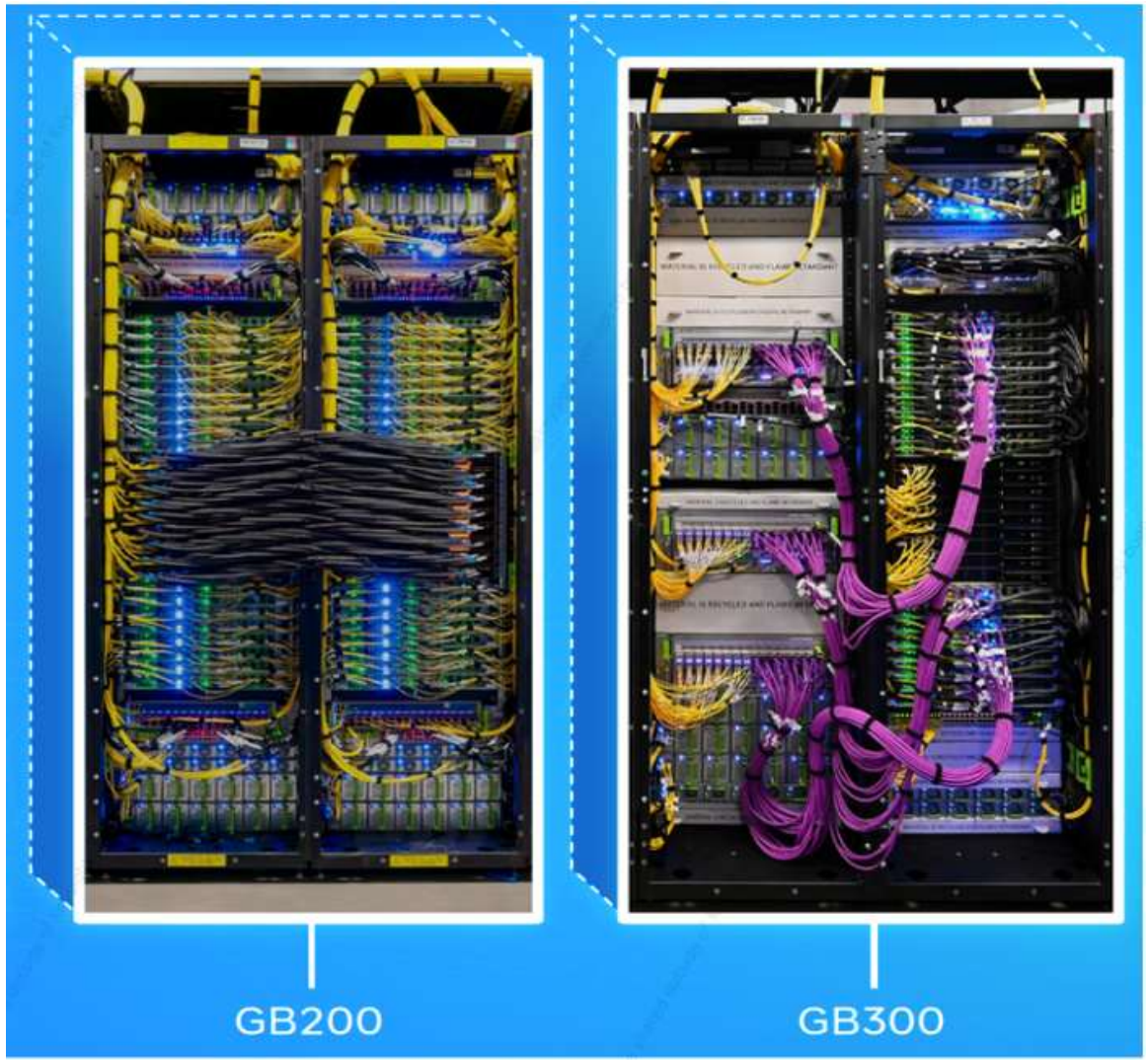
Networking Infrastructure and Equipment/Racks Require Interconnects at Massive Scale

- Historical CAPEX spend over the next 5 years
- Shorter deployment timelines
- Rapid technology adoption
- Overlap of 224G and 448G lane speeds





Every Rack Interconnect Requires Error-Performance Validation



Pluggable Optics

1.6T/3.2T transceivers for switch front panels, spine/leaf and scale-out networks

Active Optical Cable (AOC)

Optics embedded into cable assembly for longer-reach rack and cluster links

Active Electrical / Active Copper Cable (AEC/ACC)

Extends reach at lower cost with thinner cables than optics

Direct Attach Cable (DAC)

Lowest-power passive copper for the shortest in-rack links

Backplane

Dense board-to-board interconnects within rack-scale AI systems

Near-Chip Copper

Short flyover cables from the XPU/ASIC to the backplane or panel

Why Functional BER and FEC Validation is Mandatory at 224G

Component passes compliance

Complete S-parameters, eye, TDECQ Measurements — before error performance testing

Component assembly errors

Retimers, DSPs, CDRs & equalization converge differently across cables, connectors and backplanes

BER may not reveal all errors

BER may look “OK” until crosstalk or system-level defects cause bursty errors

System-Level performance

Customers care about system-level, error correction performance, link flaps, latency, and reproducible failure isolation

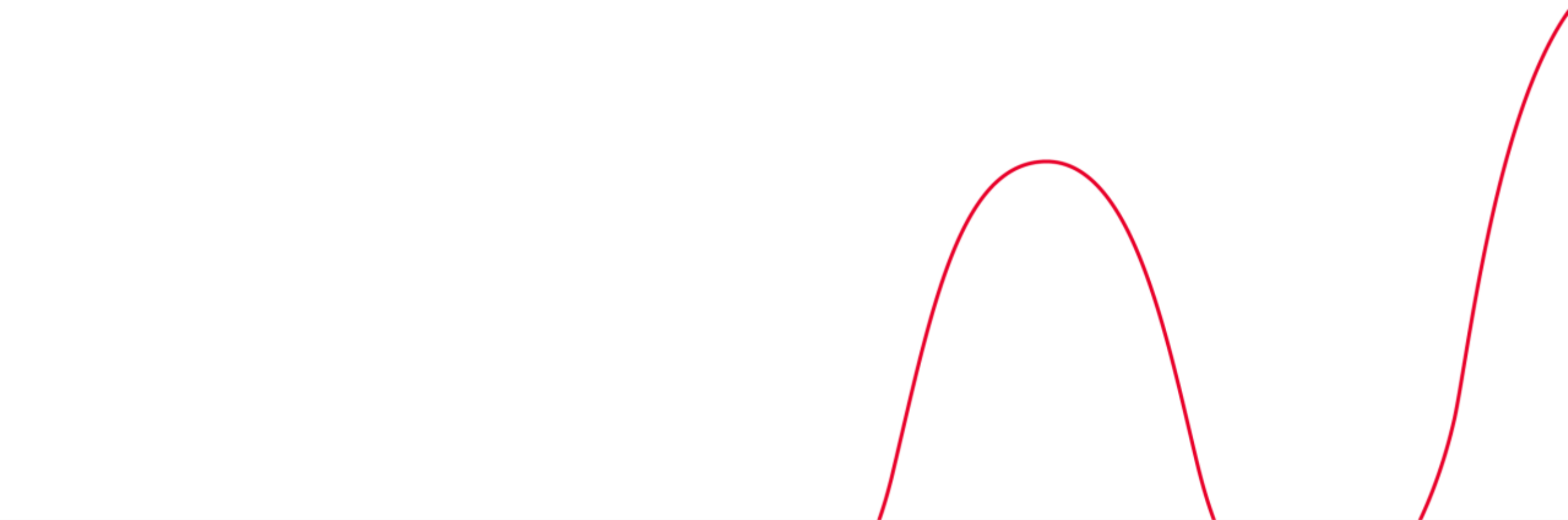
The test gap grows with 224G lane rates

- Less margin for insertion loss, skew, crosstalk and jitter
- Good S-parameters can make marginal links look “ok” until error-correction performance fails in the rack

Why system-level performance testing wins

- Test complete link behavior—not just standalone components
- Common pass/fail metrics across interconnects, backplanes and flyover cables
- Reproduce field failures in the lab

Challenges in Validating High-Speed Devices and Interconnect Performance



Top Challenge for Interconnects

Do your interconnects meet customer performance expectations?

High-speed interconnects require error performance validation using BER and Forward Error Correction to meet AI and data center application performance and reliability requirements.



KEYSIGHT

Top Challenge for Interconnects: Error Performance Validation

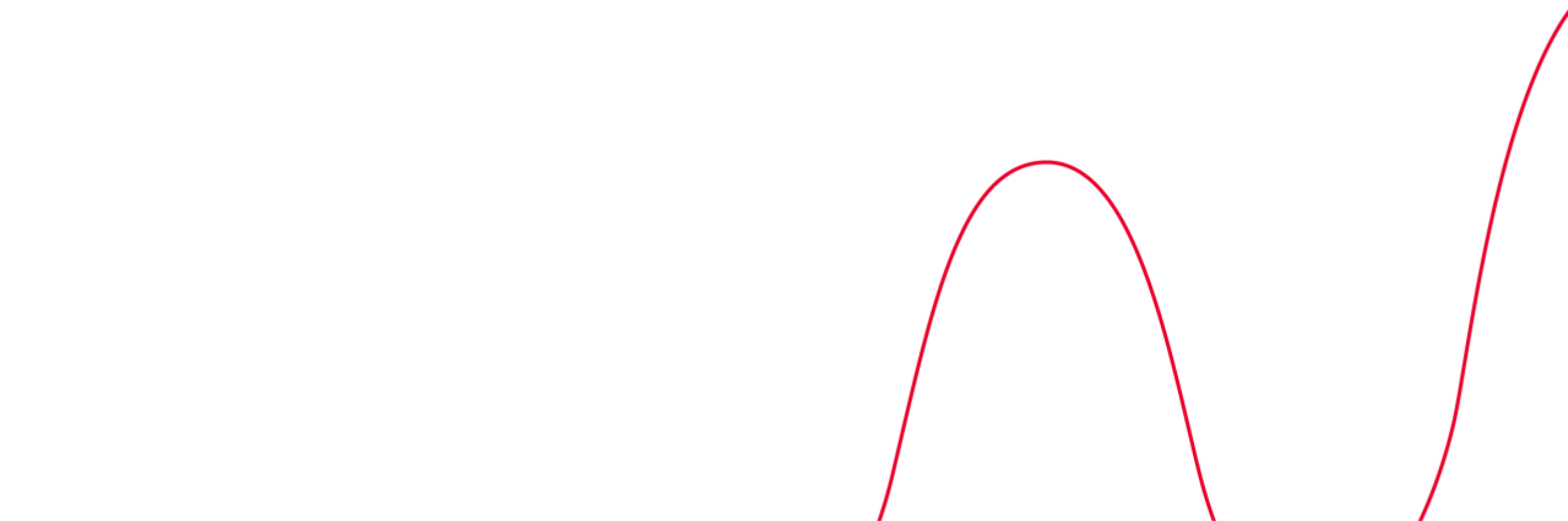
Testing High-Speed Interconnects with BER May Not Meet AI Data Center Performance Requirements

Four New Principles for Interconnect Validation
1. Testing PAM4 interconnects with only BER is not enough to predict system level performance
2. Interconnects in production networks must outperform industry standards by several magnitudes
3. It’s critical to test interconnects both standalone and when interoperating with networking equipment
4. System level interconnect performance testing is required in long duration tests

Implementing Interconnect Error Performance Validation Principles

Four new principles for interconnect test	How to implement these principles
BER alone can't predict system level performance	• Test interconnects with FEC running • Test at ALL Ethernet speed configurations • Test the interconnect as if it were installed in a real network under stress AND in live use conditions
Production network interconnects must outperform industry standards by several magnitudes	Customers demand better performance in: • BER – analog and digital • Pre-FEC BER • FEC symbol error correction and distribution • Frame Loss Ratio = 0.0E00 (customer expectation) • Block Error Ratio (BLER), new to IEEE802.3dj • FEC margin to allow bursty errors and still not have an uncorrectable FEC codeword • Interoperability with network devices and equipment
It's critical to test interconnects both standalone and when interoperating with networking equipment	Testing the interconnect by itself does not guarantee its performance in many network equipment systems
Interconnects require system level testing	Test the interconnect as if it were installed in a real network under stress and in live use conditions

Critical Measurements in Validating Error Performance

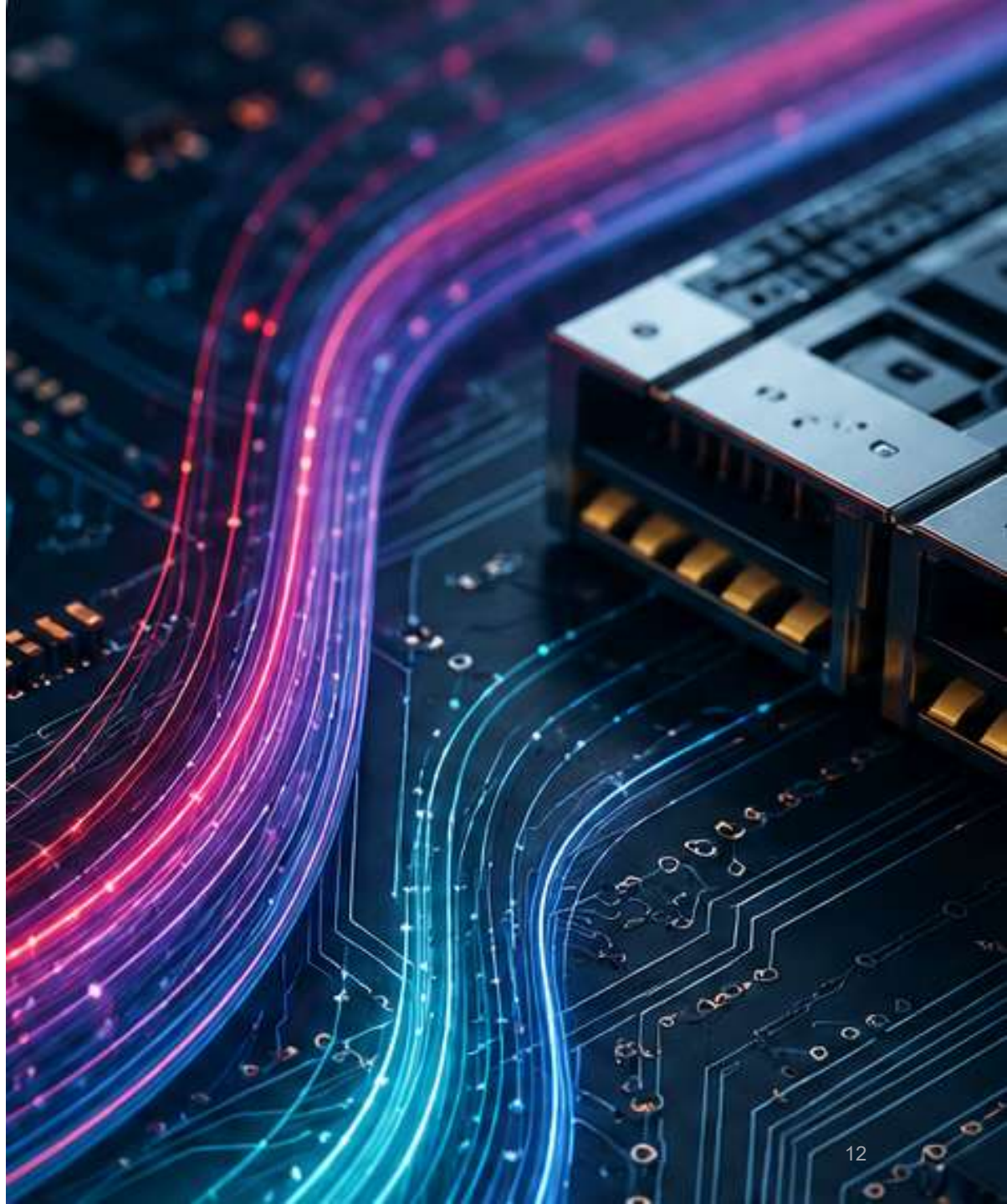


Critical Measurements for Validating Interconnect Error Performance

- **Measure BER at the digital layer,** testing all Tx and Rx lanes simultaneously
- **Evaluate FEC symbol error correction performance** on all electrical and optical lanes
- **Validate CMIS programming on the interconnect**
- **Test all Ethernet speeds supported by the interconnect**

Additional Measurements

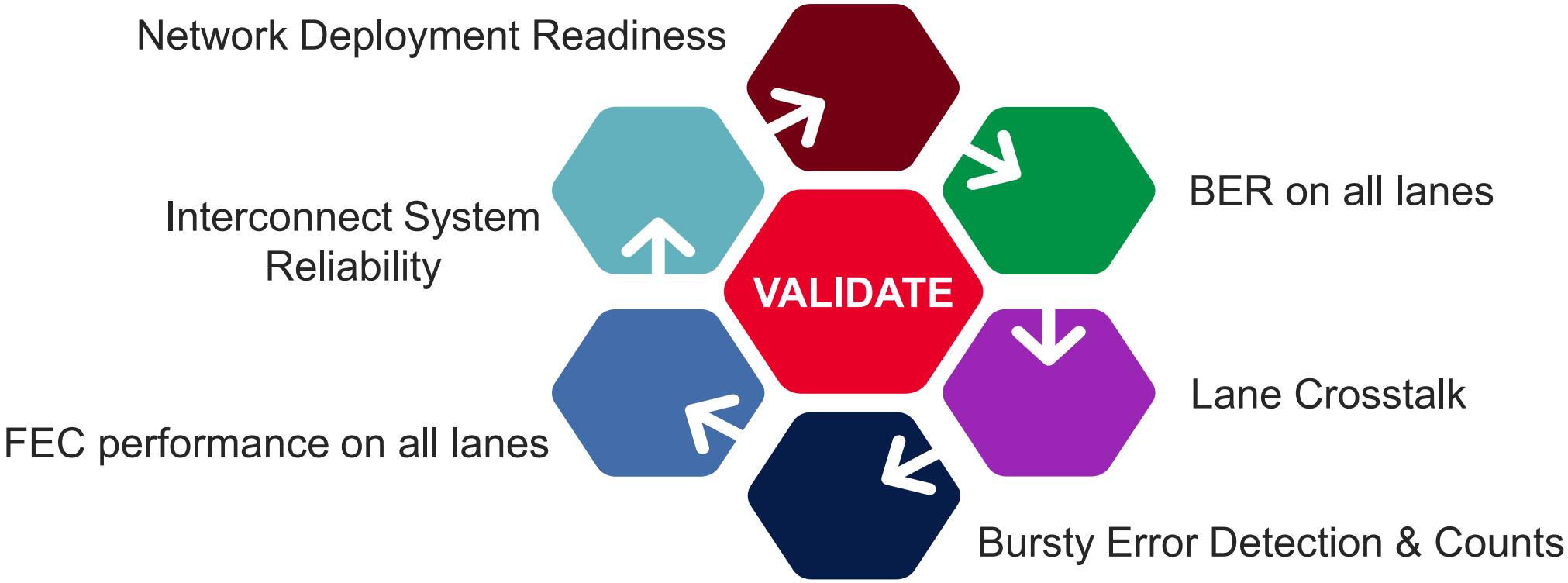
- Measure BER for physical-layer electrical and optical tests
- Generate Layer 2 Ethernet frame Tx and Rx traffic using the most stressful methods
- Assess system-level performance and multi-vendor interoperability
- Benchmark performance and conduct RFC stress testing in real server, switch, and router systems



KEYSIGHT

Functional BER & FEC Error Performance Validation

PAM4 Interconnects Require Error Correction + Performance Measurements for R&D and System-Level Applications



Functional BER & FEC Error Performance Validation in Manufacturing

Critical PAM4 Interconnect Measurements are Required in Specific Production Applications

- Use Windows GUI for quick pattern generator setup and BER validation
- Automate test scripts with SCPI API
- Auto-Tune PAM4 eye using a Keysight Digital Communications Analyzers (DCA)
- Use FEC performance to debug lanes
- Measure BER on all lanes for pass/fail checks
- Detect sub-assembly failures
- Stress assemblies in temperature chamber for pass/fail BER performance

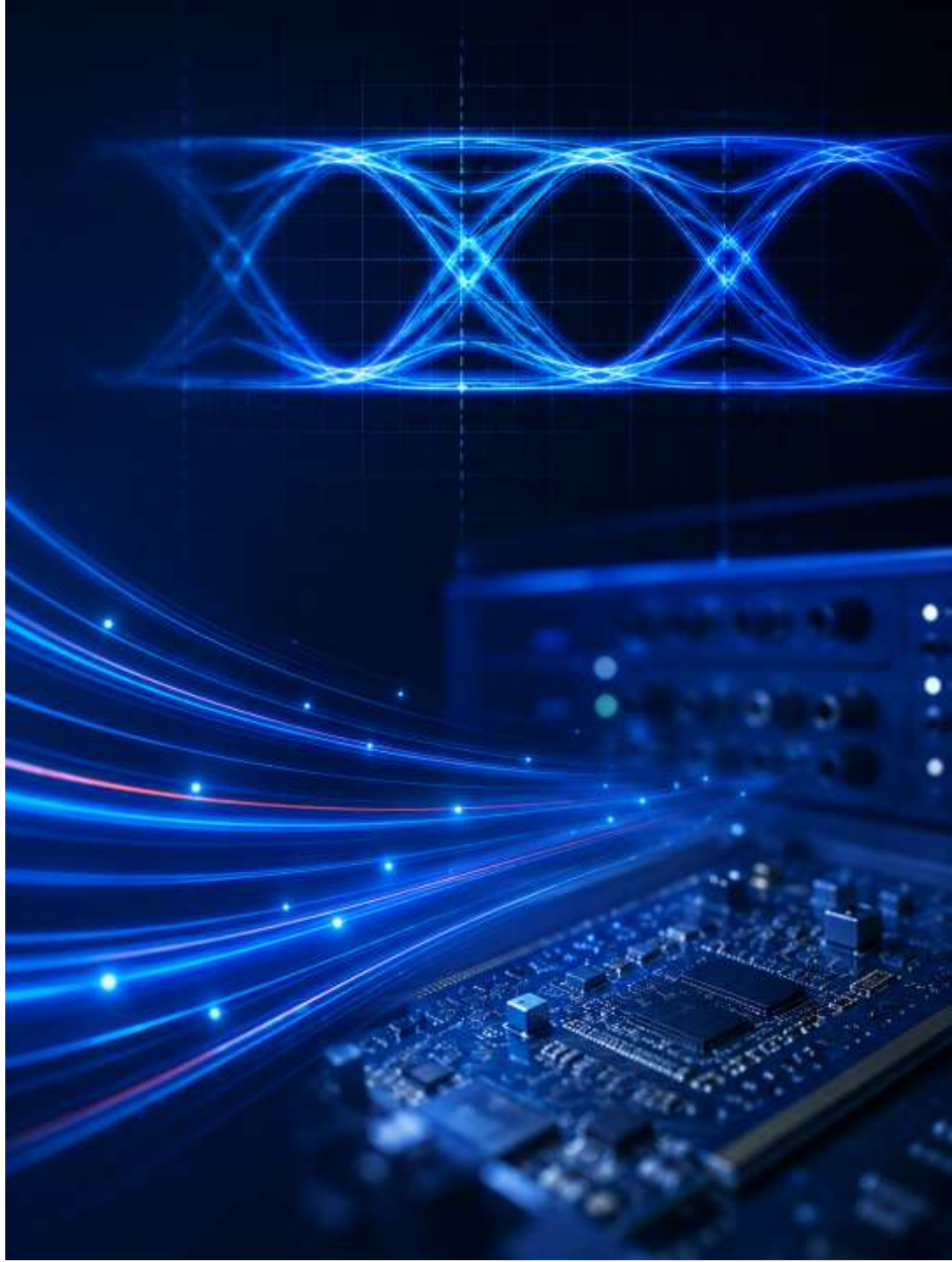
CMIS Validation is Important for Error Performance of all Configurations

Validate CMIS programming on the interconnect:

- Read vendor registers (identify the interconnect)
- Read Application Selection Code
  - Conduct BER and FEC tests with all the supported configurations for error correction performance

Digital Optical Monitoring (DOM)

- Provide information from the interconnect
- Check device status, electrical power, temperature
- Check Power class, laser power and various Loss of Lock (LOL) and Loss of Signal (LOS) thresholds
- Check alarms and thresholds settings

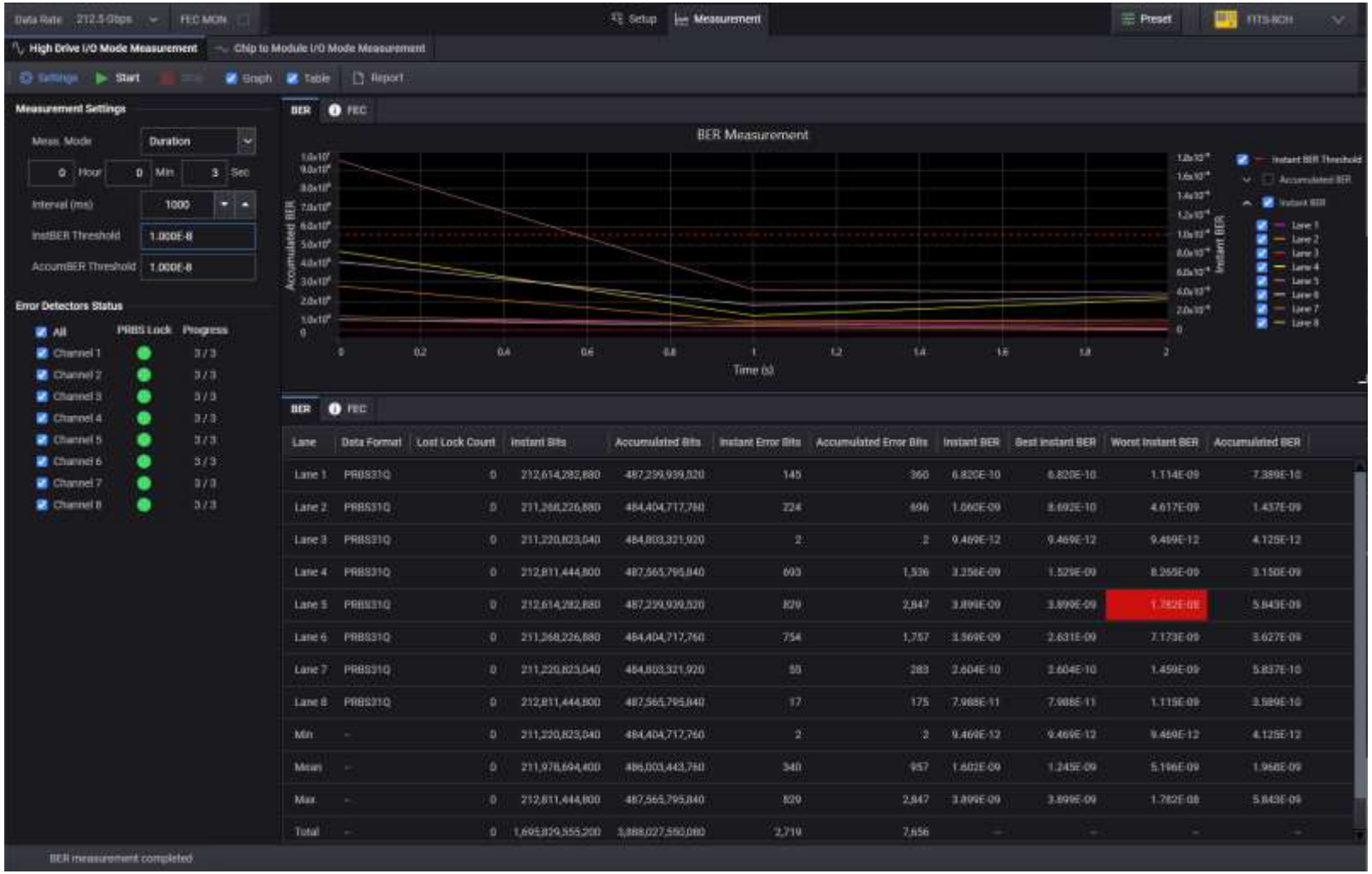


KEYSIGHT

FITS GUI – BER Testing

Measurements on All Lanes with Pass/Fail Indication

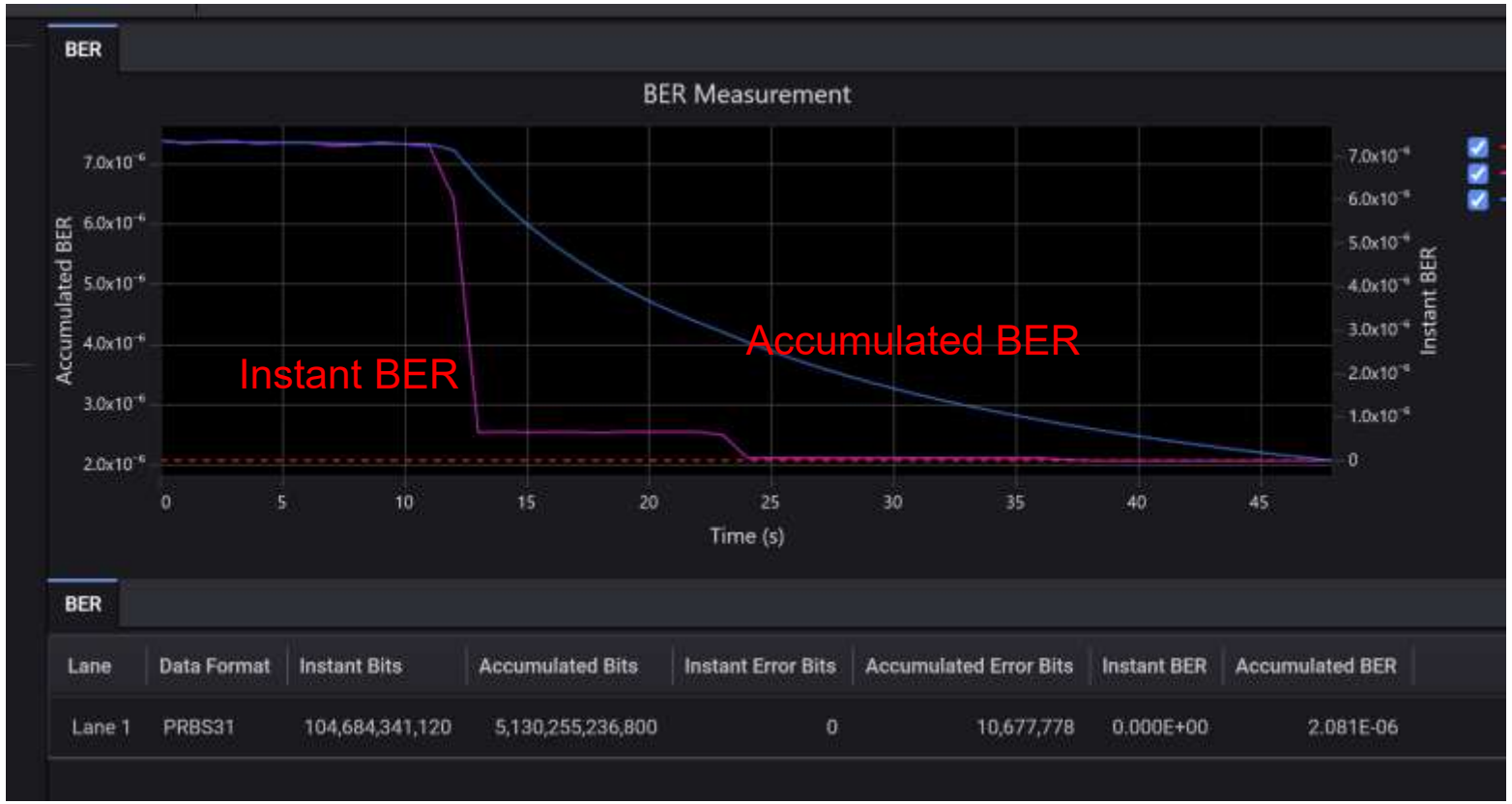
- Specify the measurement duration/count and the interval between samples
- Note PRBS Pattern lock LED
- Two main types of statistics:
  - Instant (“rates”)
  - Accumulated
- Pass/fail criteria is based on these test limits per lane:
  - Worst Instant BER
  - Accumulated BER



FITS GUI – BER Testing

Why Instant Error and Instant BER Counters?

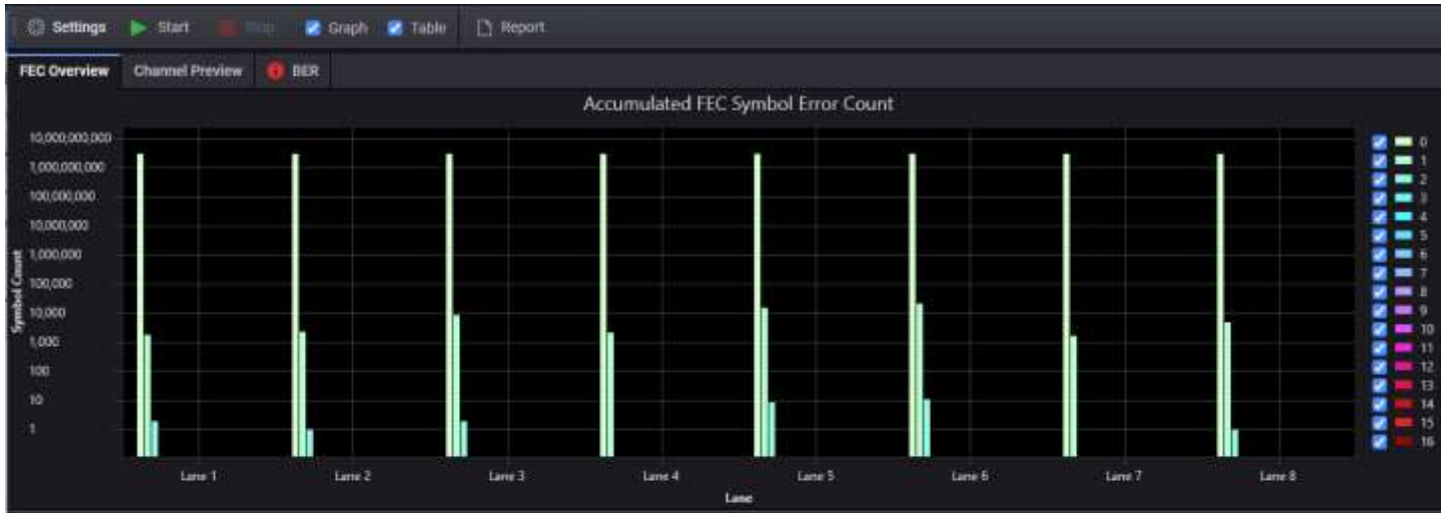
- Instant BER is useful for debugging in real time
  - Example: A single lane of Rx stats where the Tx FIR taps were optimized on the fly from a second FITS-8CH Tx



FITS GUI – FEC Monitoring

FEC Measurements on All Lanes

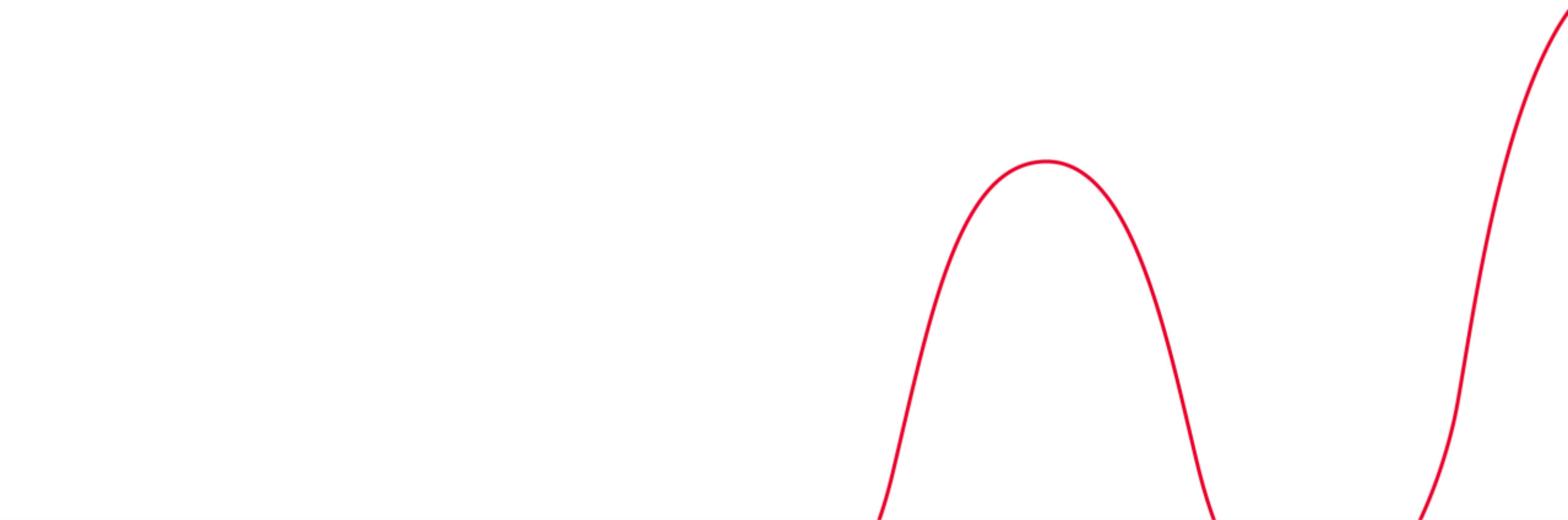
- FEC Monitoring mode produces FEC error distribution statistics
- FEC graphs are available per lane
- PDF and Excel *csv reports are available with graphs and data tables



FEC Overview | BER

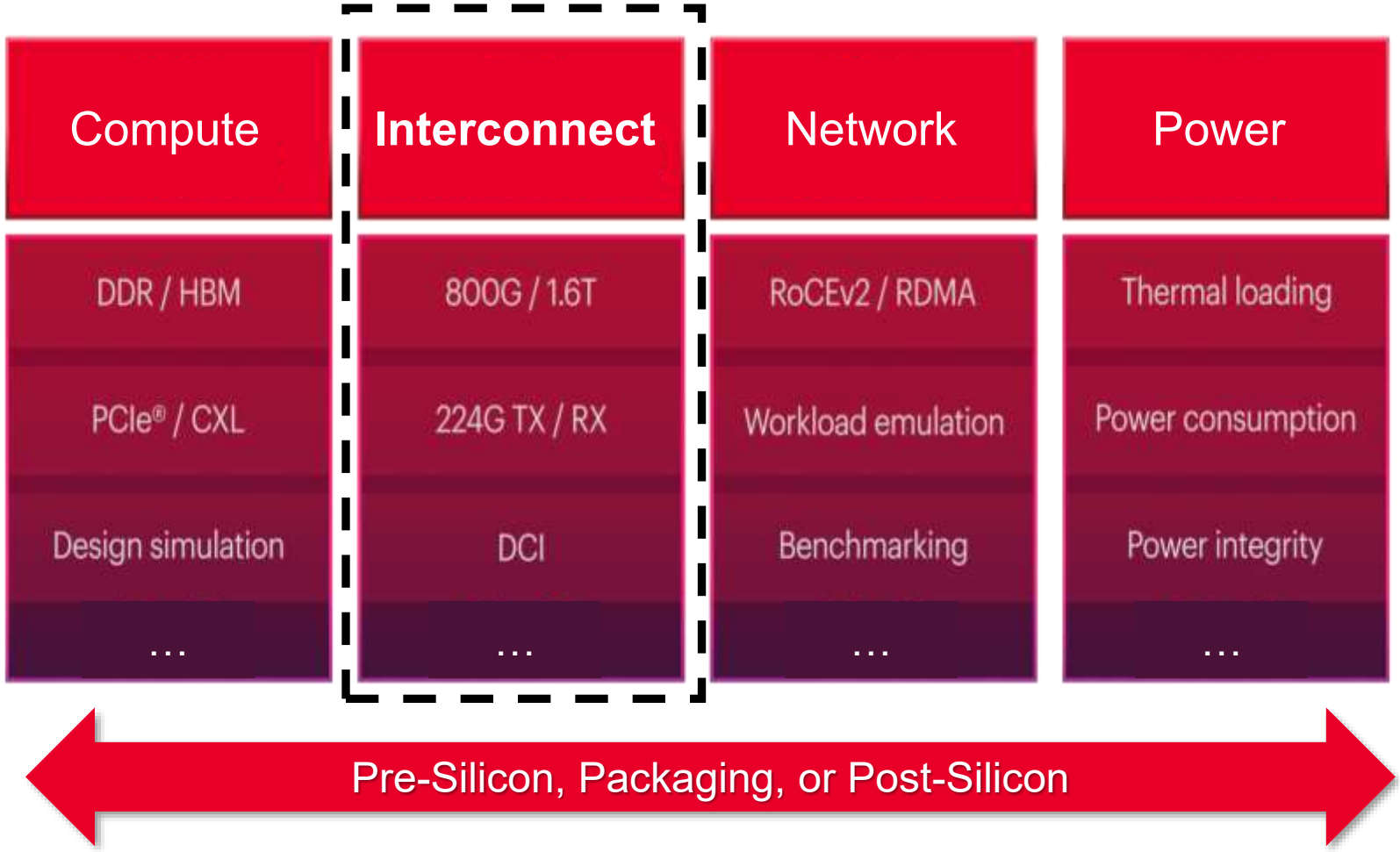
Metric	Channel 1		Channel 2		Channel 3		Channel 4		C
	Count	Rate	Count	Rate	Count	Rate	Count	Rate	Count
Pre-FEC BER	1.203E-10	–	1.474E-10	–	5.509E-10	–	1.434E-10	–	9.764E
Post-FEC BER	0.000E+00	–	0.000E+00	–	0.000E+00	–	0.000E+00	–	0.000E+
FEC Frame Loss Ratio (FLR)	0.000E+00	–	0.000E+00	–	0.000E+00	–	0.000E+00	–	0.000E+
FEC Max Symbol Error Bin	2	–	2	–	2	–	1	–	
FEC Margin	86.7%	–	86.7%	–	86.7%	–	93.3%	–	86.
Received Bits	16,803,671,292,16(	279,191,364,480	16,808,382,843,52(	279,191,005,440	16,813,247,209,92(	279,191,016,320	16,818,259,778,24(	279,191,854,080	16,825,222,575,
Total Bit Errors	2,021	40	2,477	48	9,262	156	2,412	46	16,4
Total Symbol Errors	1,864	37	2,302	46	8,908	153	2,180	41	15,0
Corrected Codewords	1,862	37	2,301	46	8,906	153	2,180	41	15,0
Total Received Codewords	3,088,910,164	51,321,942	3,089,776,258	51,321,876	3,090,670,443	51,321,878	3,091,591,871	51,322,032	3,092,871,7
Codewords with 0 Symbol Errors	3,088,908,302	51,321,905	3,089,773,957	51,321,830	3,090,661,537	51,321,725	3,091,589,691	51,321,991	3,092,856,7
Codewords with 1 Symbol Errors	1,860	37	2,300	46	8,904	153	2,180	41	15,0
Codewords with 2 Symbol Errors	2	0	1	0	2	0	0	0	
Codewords with 3 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 4 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 5 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 6 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 7 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 8 Symbol Errors	0	0	0	0	0	0	0	0	
Codewords with 9 Symbol Errors	0	0	0	0	0	0	0	0	

Functional Interconnect Test Solutions (FITS) Capabilities and Benefits



Keysight Artificial Intelligence - New Family of Interconnect Validation

Expanding Keysight's Reach into High-Speed Interconnect BER and FEC Performance Validation



New Interconnect Validation

Keysight adds new products to increase the library of high-speed AI interconnect validation solutions!

Interconnect Test Solutions – Error Performance Validation Products

FITS-8CH



- **8 Tx/Rx channels**
- Optics, AOC, AEC
- High Drive & C2M channels
- FITS GUI – BER / FEC
- Auto lane tuning w/DCA
- SCPI API
- Report Generation PDF, *.csv

FITS-16CH



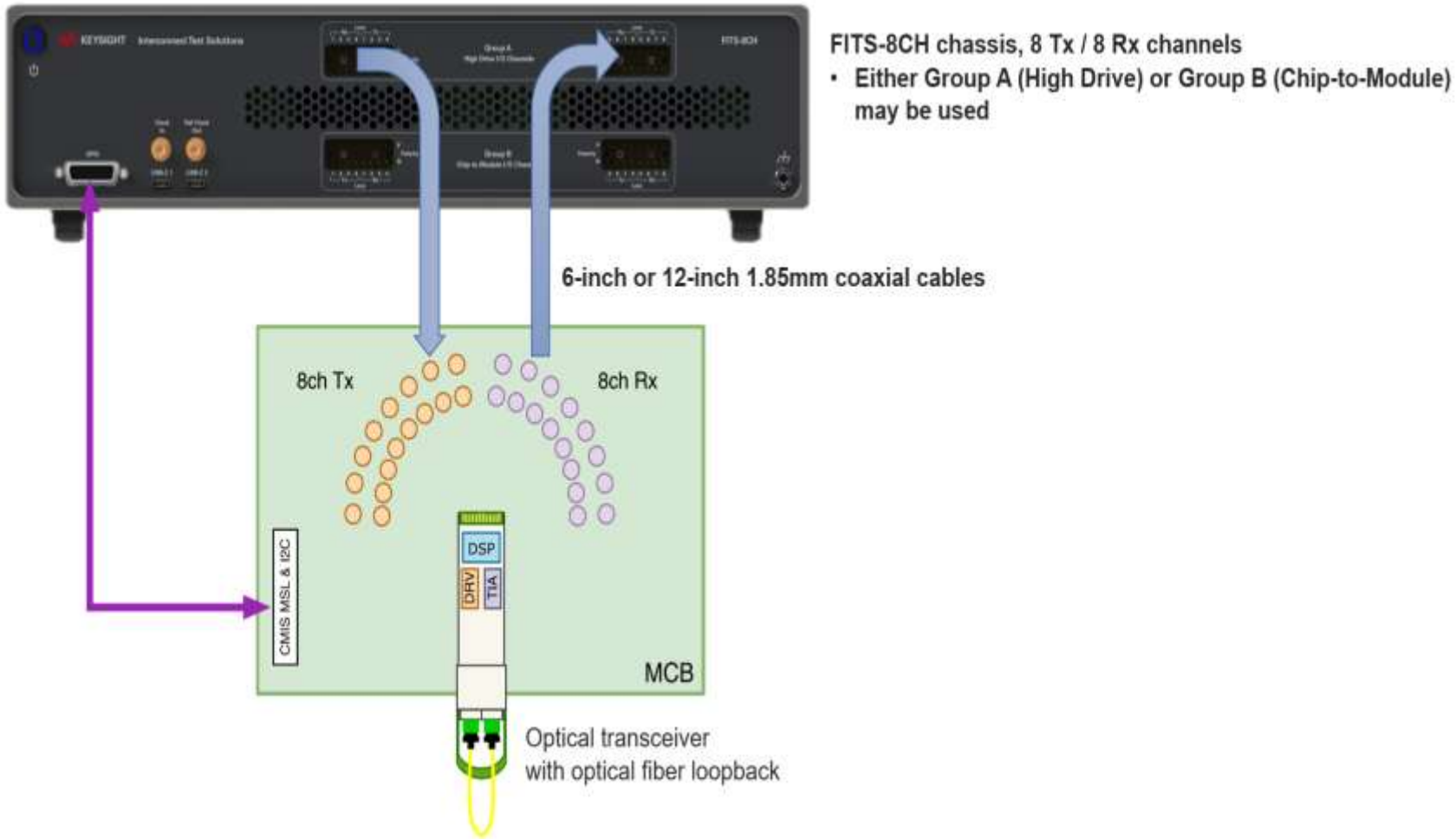
- **16 Tx/Rx channels**
- Optics, AOC, AEC, ACC, DAC
- Supports (2) MCBs
- FITS GUI – BER / FEC
- Auto lane tuning w/DCA
- SCPI API
- Interconnect Test System SW
  - Extensive CMIS & Reporting

ITS-1600GE-COAX



- **16 Tx/Rx channels**
- Optics, AOC, AEC, ACC, DAC
- Trigger IN/OUT
- Interconnect Test System SW
  - Ethernet Traffic Generation
  - FEC traffic & error insertion
  - Extensive CMIS & Reporting
  - REST API/Python

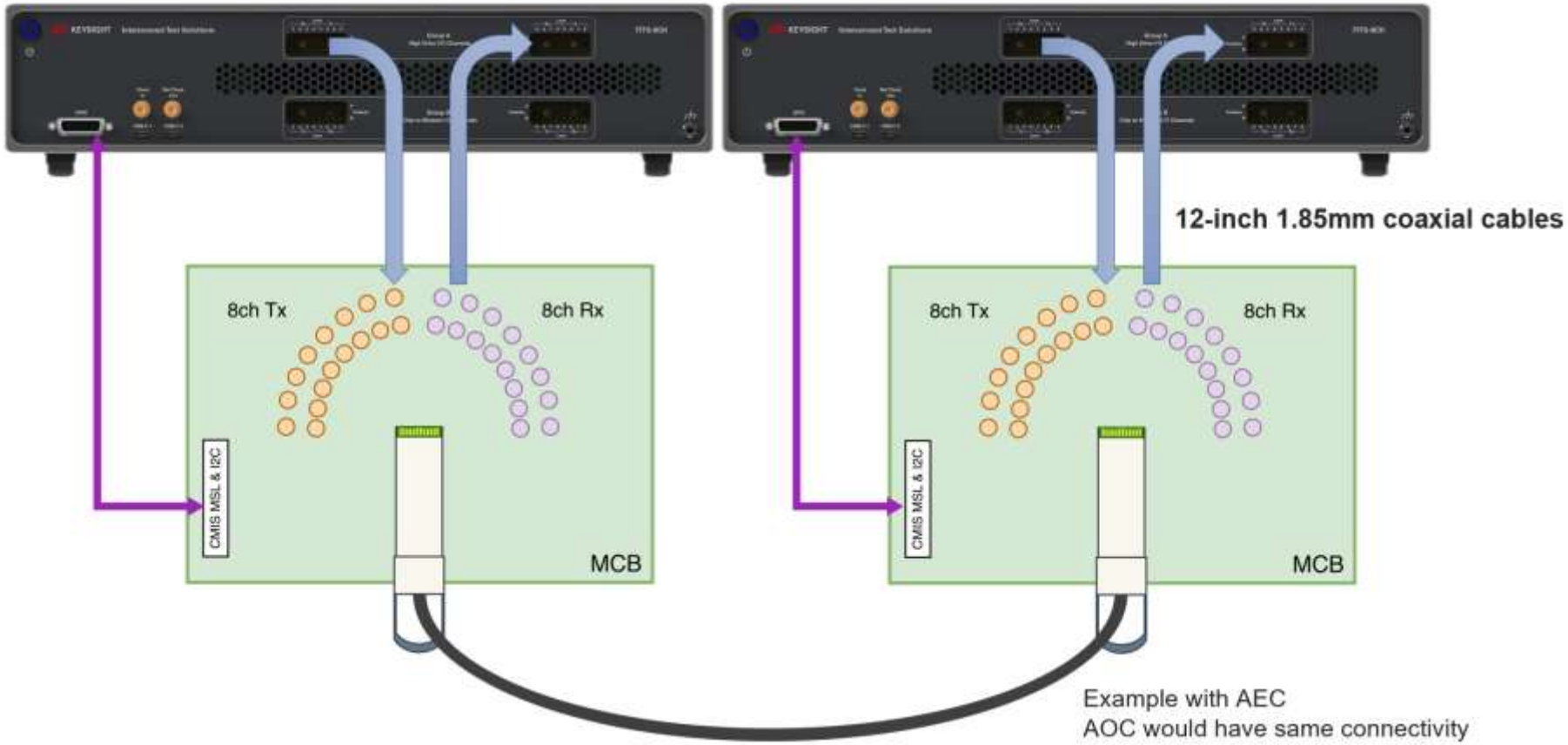
FITS-8CH Use Case - Optical Transceiver BER and FEC Performance



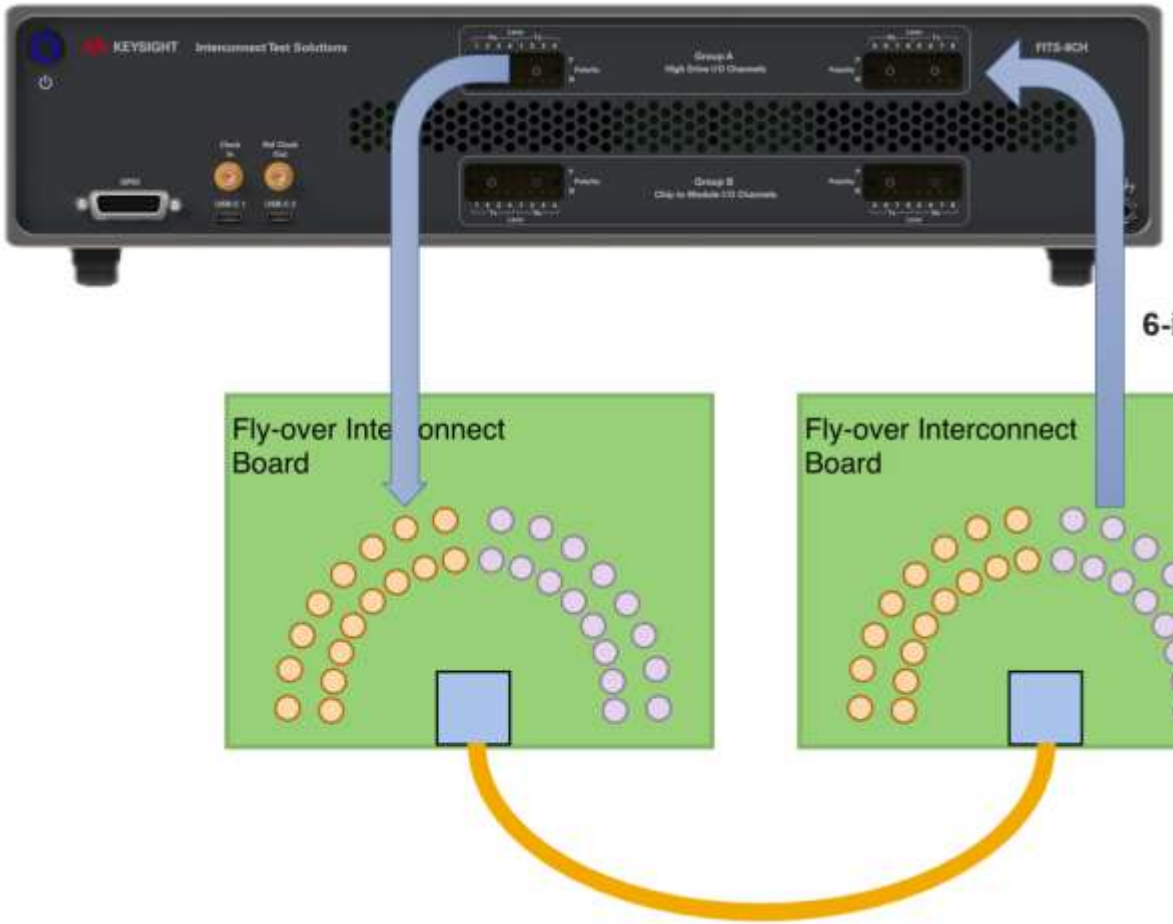
FITS-8CH Use Case - AOC, AEC, ACC, DAC BER and FEC Performance

Dual FITS-8CH chassis, 8 Tx / 8 Rx channels per MCB

- **Either Group A (High Drive) or Group B (Chip-to-Module)**



FITS-8CH Use Case - Flyover Cable BER and FEC Performance



FITS-8CH chassis, 8 Tx / 8 Rx channels

- Group A (High Drive) to compensate for insertion loss at the PCB and perform Tx FIR auto-tuning with DCA.

6-inch or 12-inch 1.85mm coaxial cables

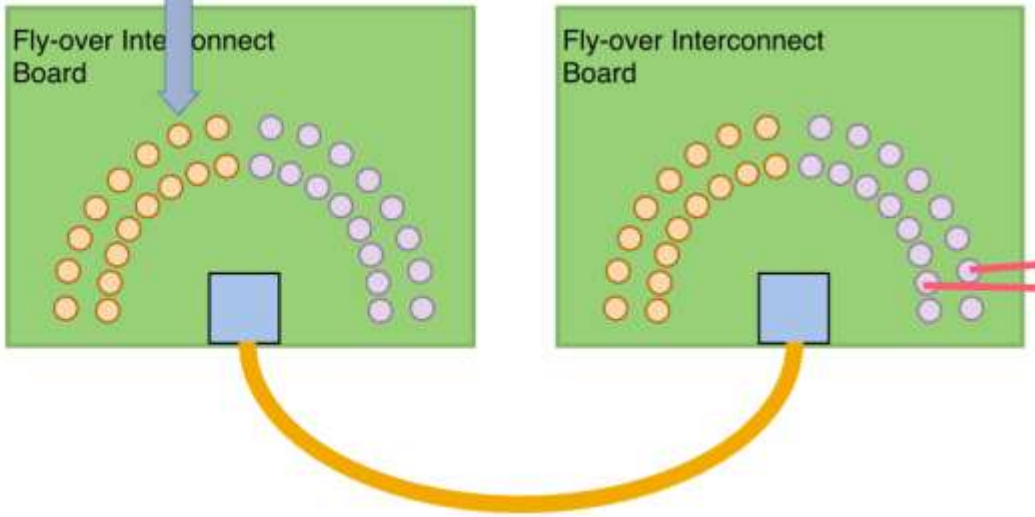
Use Case - Flyover Cable BER & FEC Performance with Auto Lane Tuning



FITS-8CH chassis, 8 Tx / 8 Rx channels

- Group A (High Drive) to compensate for insertion loss at the PCB and perform Tx FIR auto-tuning with DCA.
- Lane auto-tuning is automated from within the FITS-8CH UI.

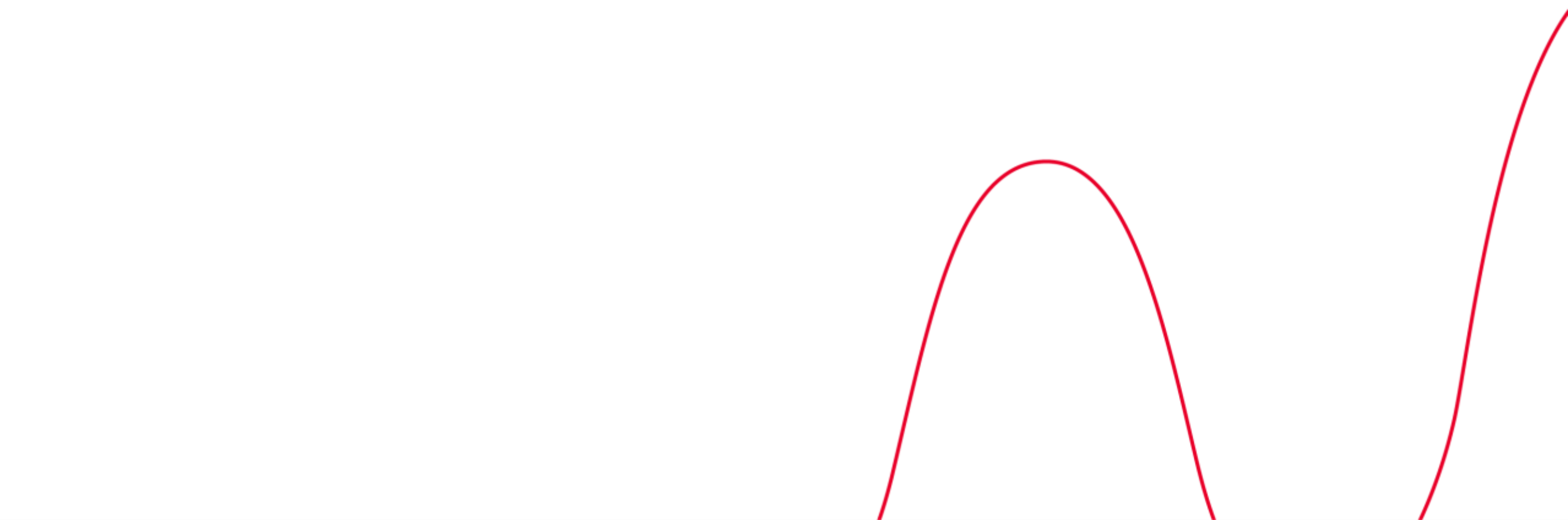
6-inch or 12-inch 1.85mm coaxial cables



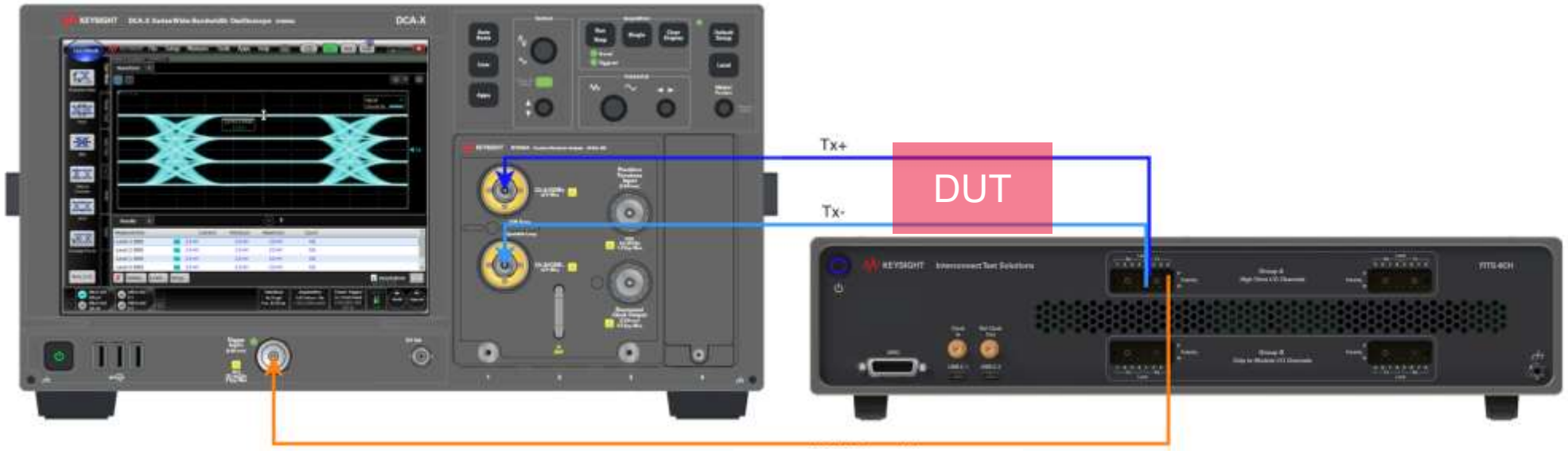


DCA-X with N1060A module

Demonstration: Automated Lane Tuning to Improve Error Performance Validation



FITS-8CH Auto Lane Tuning with N1060A – Example Topology



Data Rate	Baud Rate	Mainframe	Module	Data Connection from FITS-8CH	Trigger Connection from FITS-8CH	Automated Eye Tuning Support?
212 Gbps	106 GBaud	N1000A	N1060A	Tx+/- to N1060A Ch A&B	SQR Wave to N1000A Front Panel Trigger	Yes: select Clock Source=Trigger In
106 Gbps	53 GBaud	N1000A	N1060A	Tx+/- to N1060A Ch A&B	SQR Wave to N1000A Front Panel Trigger	Yes: select Clock Source=Trigger In

FITS-8CH - Auto Lane Tuning with Difficult Channel





300mm (12”)
1.85mm coaxial cables

Fly-over Interconnect Board

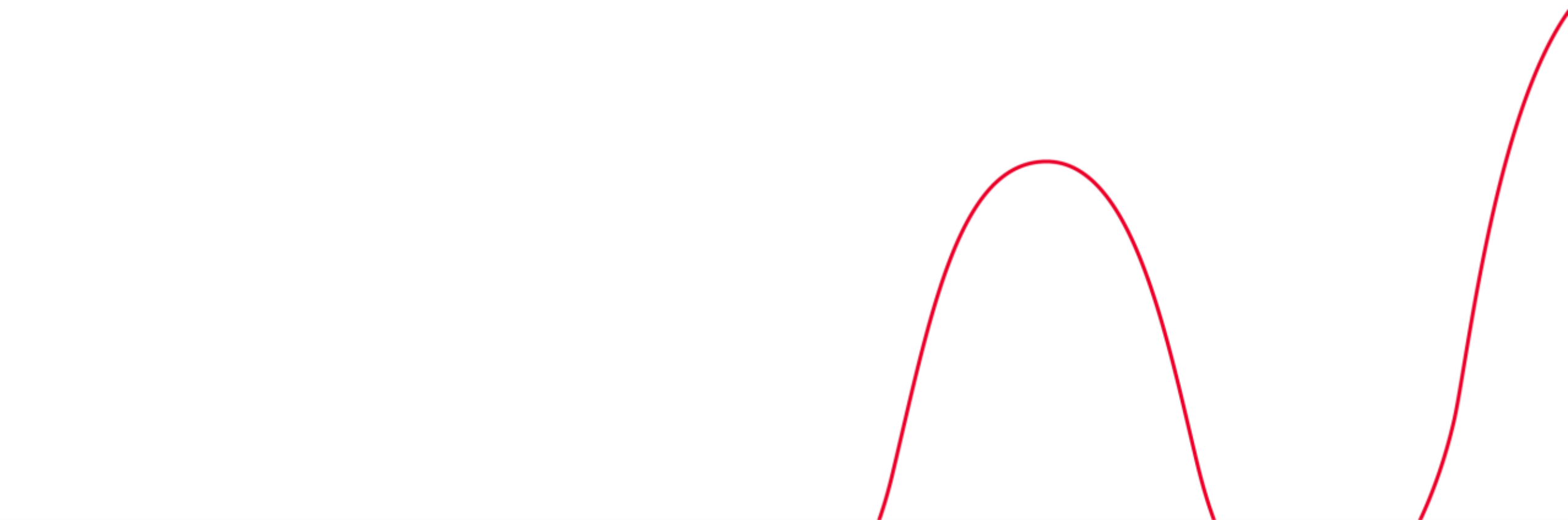
Fly-over Interconnect Board



Square Wave from FITS-8CH

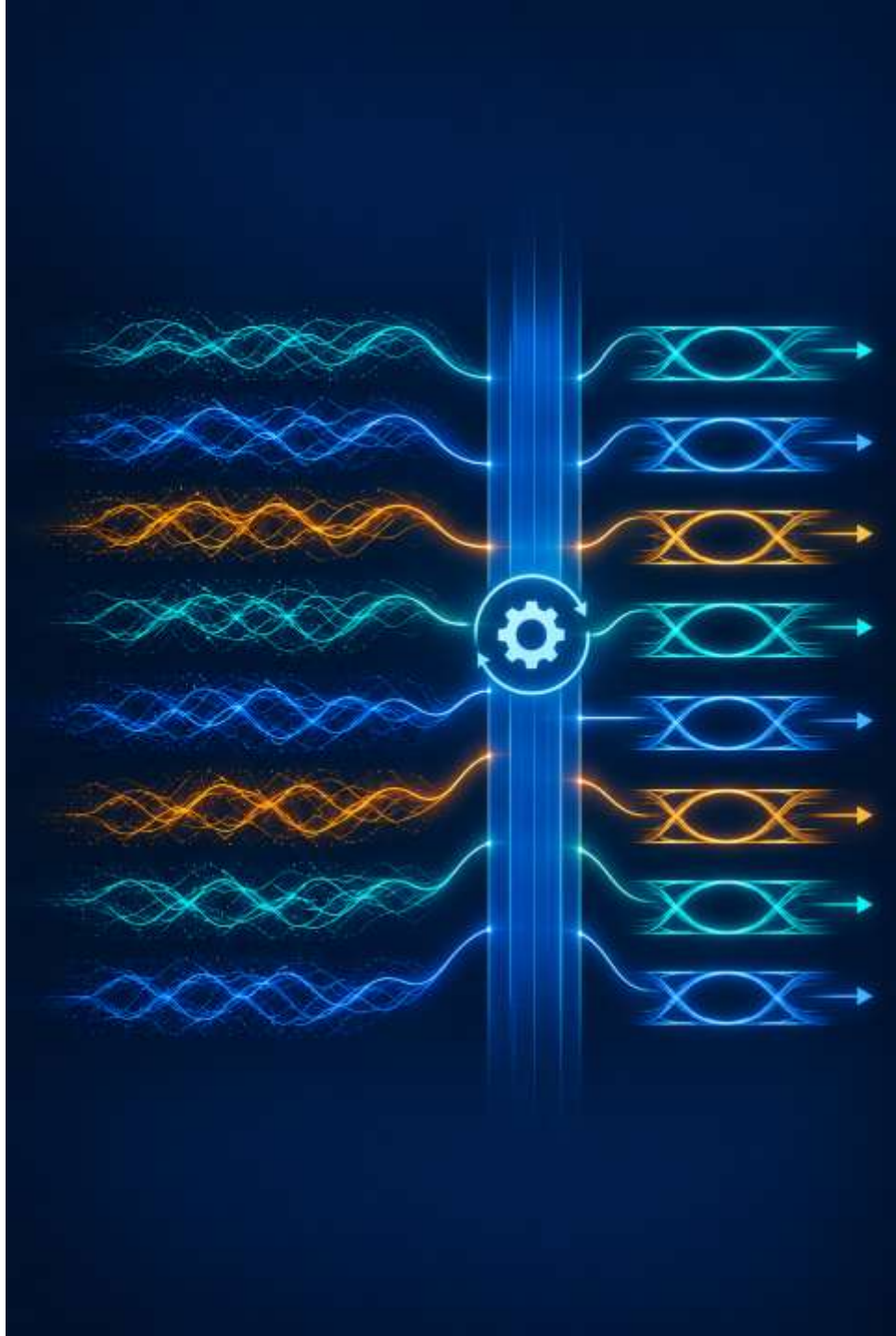
1 meter coax (impairment for demo)

The Benefits of Using This Technique



FITS-8CH – Automated Lane Tuning Benefits

- FITS-8CH provides optimized Tx FIR defaults for MCB operation:
  - For example, when using retimed optics or AECs
- Custom evaluation boards (EVB's) or passive fixtures may require different Tx FIR taps
  - Very time consuming and frustrating
- Electrical auto-lane tuning provides a good starting point!
  - Fast and repeatable process
  - Once completed, you can start testing immediately
  - Quickly optimize the Tx FIR taps further if necessary



Wrap-Up and Key Takeaways

- BER alone is not enough for high-speed interconnect validation
- Validate error performance with BER and FEC simultaneously on all lanes
- It is critical to test interconnects as they perform in real networking systems
- Measure the performance metrics your customers depend on
- System-level validation is essential for reliable interconnect performance

Additional Resources

FITS Product Page

FITS Data Sheet

FITS Solution Brief

FITS 8-CH
Press Release

Simplify 1.6T Ethernet
Testing Webinar