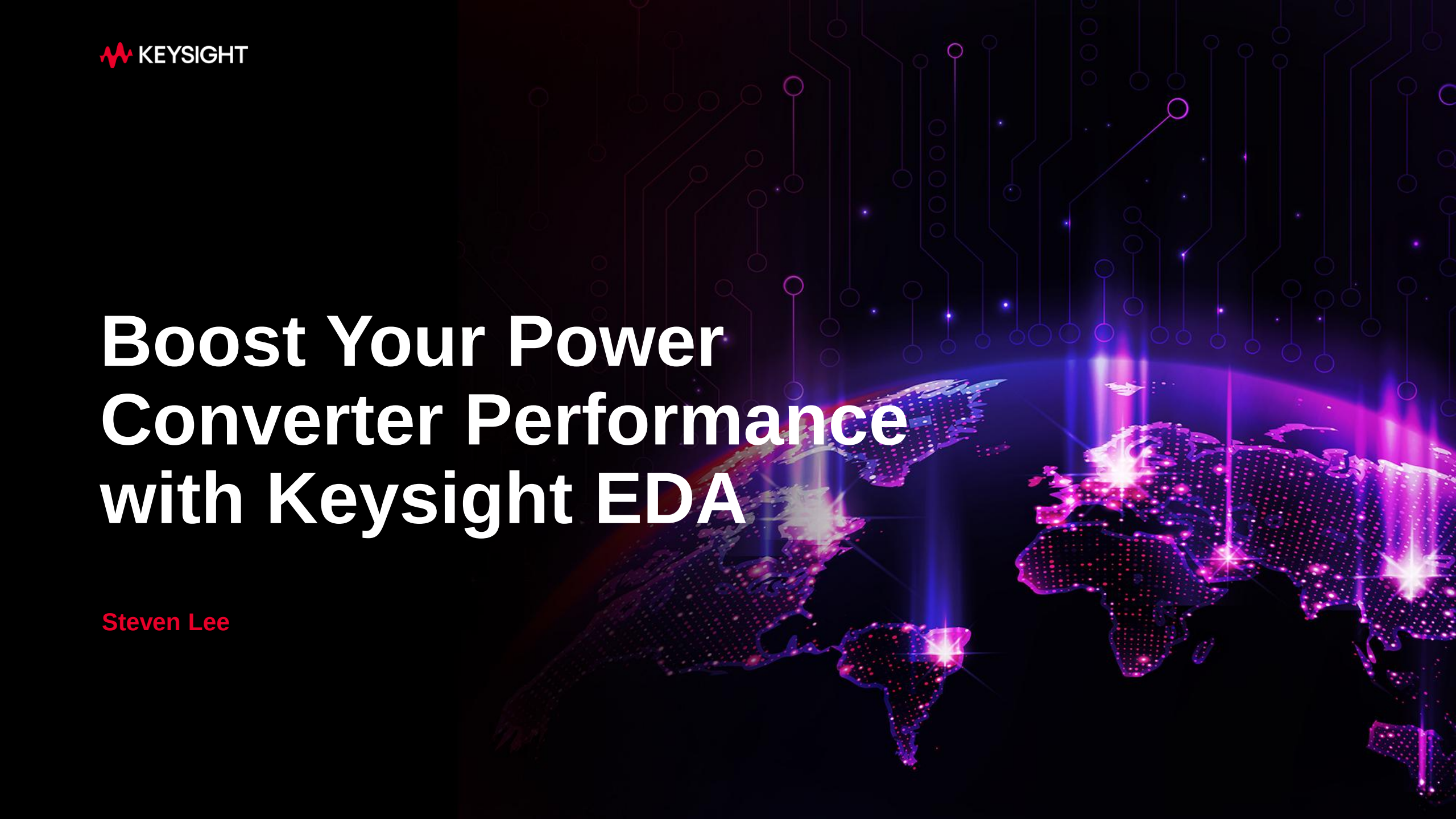
KEYSIGHT

Boost Your Power Converter Performance with Keysight EDA

Steven Lee



Objective

Objective:

Learn a more advanced design and simulation workflow for power converter design incorporating post-layout simulation techniques. See how it generates higher accuracy simulation results which will boost your power converter performance

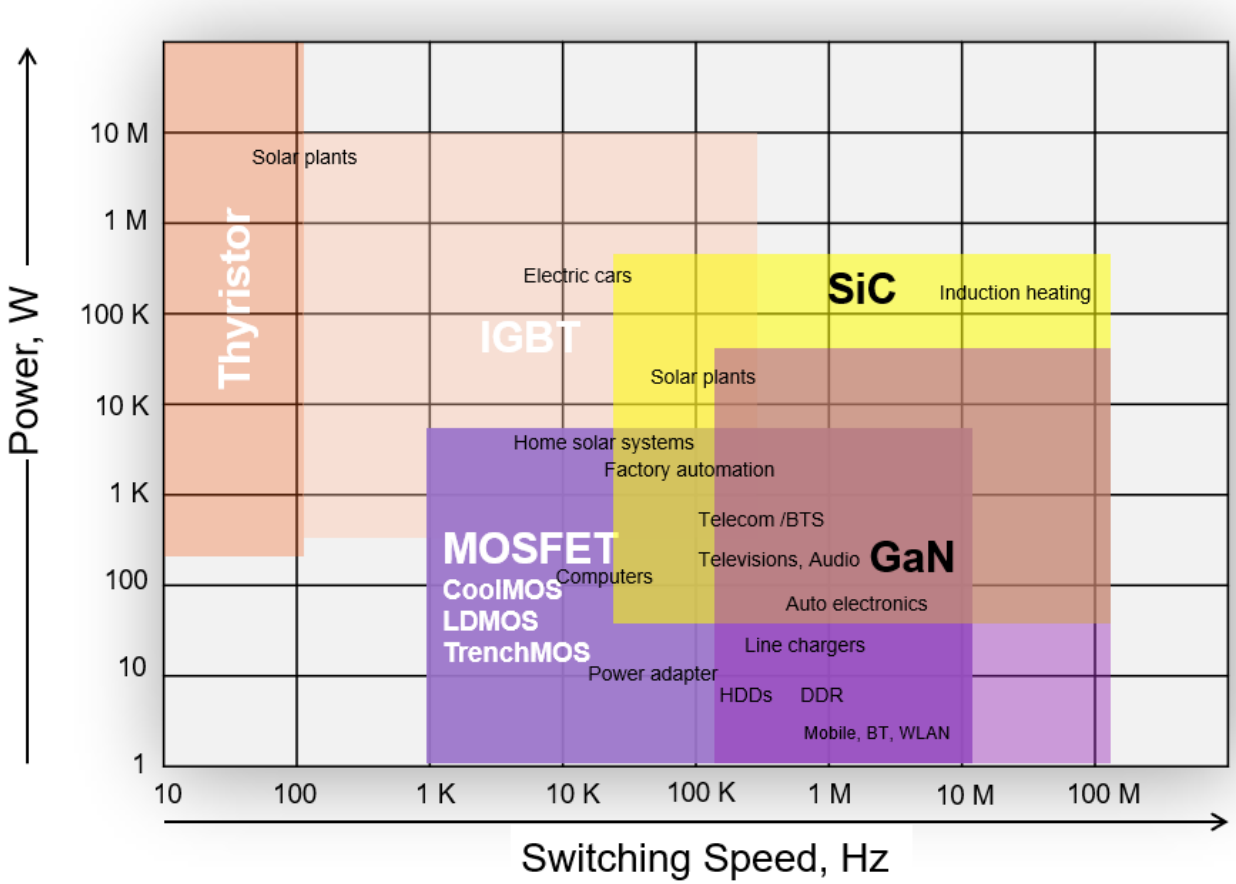
Agenda

- **Trends and Challenges in Power Converter Design**
- Keysight ADS and PEPro Electromagnetic Simulation Solution
- Demo
- Summary

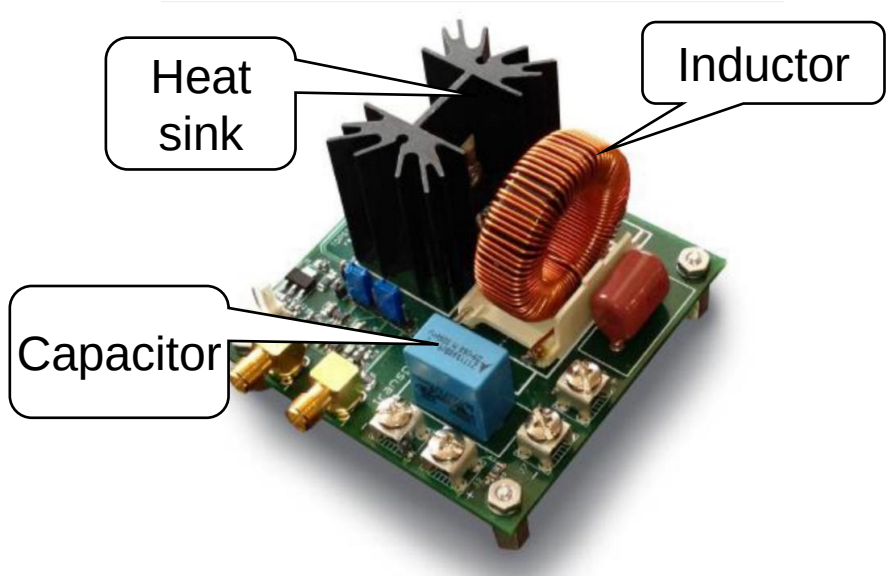
Trends in Power Electronics

The rise of wide bandgap technologies

- Wide Bandgap (WBP) semiconductors such a SiC and GaN are emerging technologies
- WBG technology enables many benefits to power conversion
  - Higher power levels
  - Greater efficiency
- Industries such as electric vehicles and renewable energy are key drivers in power electronics advancement



Trends in Switched-Mode Power Supplies



Consumer demand for:

- lower cost
- smaller size
- lighter weight

…is driving the industry to higher switching speeds “high di/dt”

Traditional (cut-and-try) design methods don’t work for high di/dt

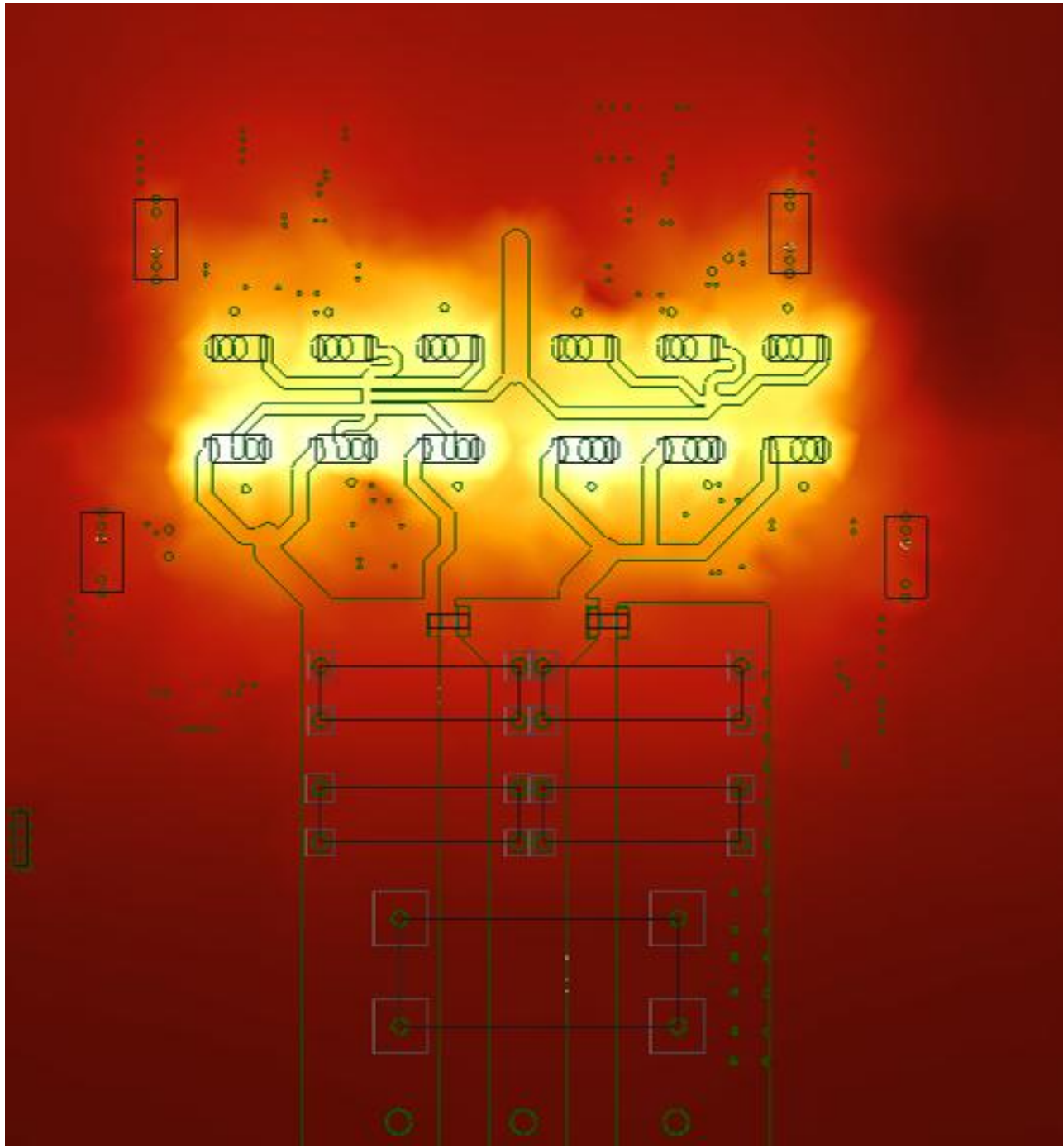
- $V_{spike} = L_{parasitic}\, di/dt$

- Need to add a field solver to extract layout parasitics into an EM-based model

Thermal Challenge

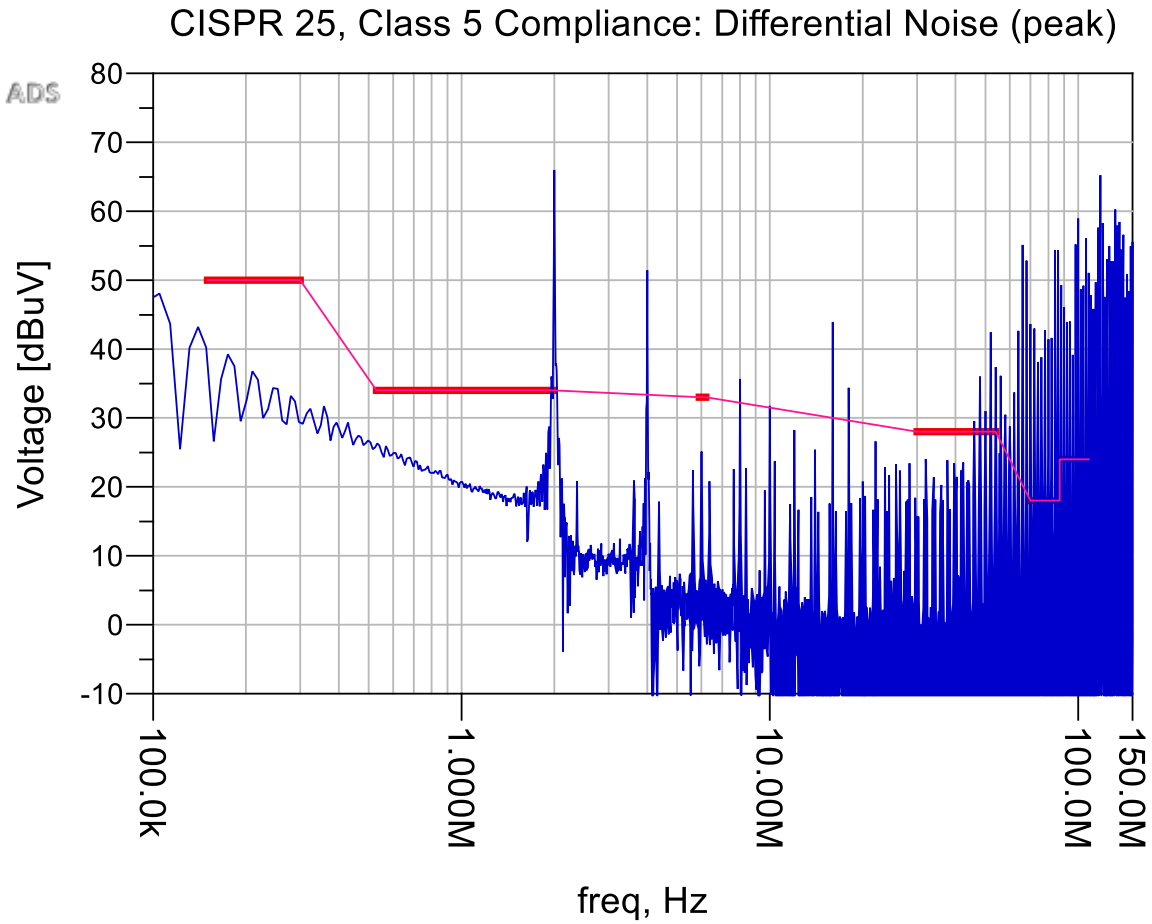
Higher Temperatures

- Power semiconductor device selection
- Heat sink design
- Thermal interface material
- Thermal modeling and simulation
- Operating conditions



EMI Challenge

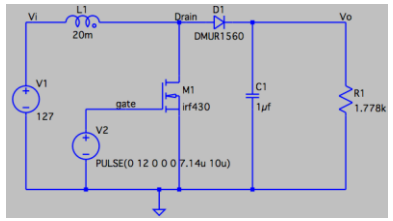
- Switched-mode power supplies produce noise and EMI that can interfere with other electronics and degrade performance and/or reliability. EMI is not easily understood or predicted.
- Spinning designs and pre-compliance testing is a costly and time-consuming process. In the past, this has largely been the process used to reduce EMI.



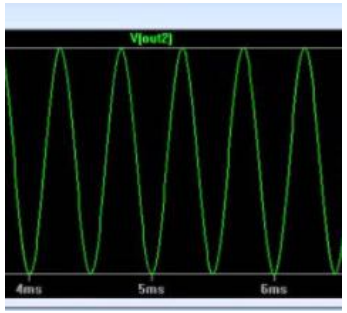
Traditional Approach

2-6 spins per design

Schematic
(Ideal)

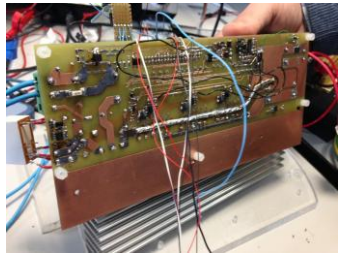


Draw circuit in schematic



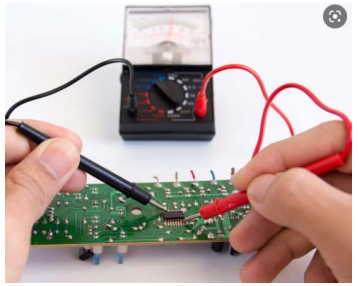
Simulate ideal conditions

Prototype
(Real World)



2-6 spins
$6k-$60k/spin
3-8 weeks/spin

Test/Debug
Validation
(Real World)



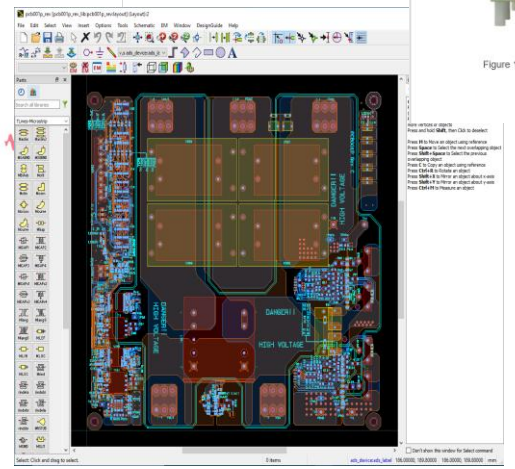
Agenda

- Trends and Challenges in Power Converter Design
- **Keysight ADS and PEPro Electromagnetic Simulation Solution**
- Demo
- Summary

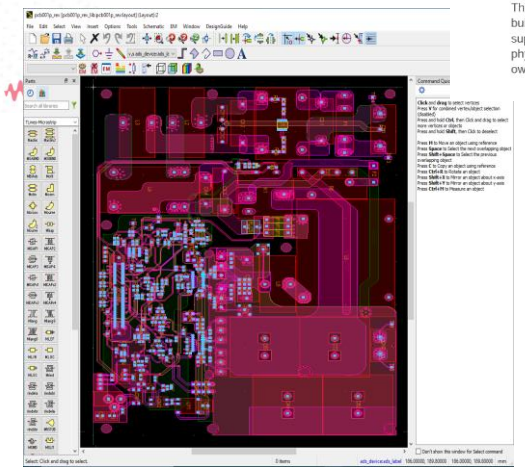
Who have partnered with Keysight EDA in power electronics?

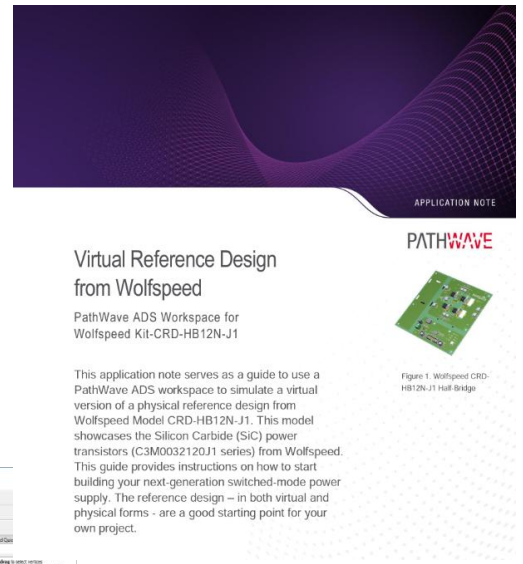
Reference Design

[ROHM]



[Transphorm]





[Wolfspeed]

Who have partnered with Keysight EDA in power electronics?

Other Projects

pcim EUROPE

An ANN Assisted Reverse Recovery of Diode Model for Switching-on Characteristics of IGBT Devices

Huaiyuan Zhang[1], Abby Shih[2], Stefan Haensel[3], Zeeshan Umar[3], Steven Lee[1], Felix Zeyss[3]

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[2] Keysight Technologies, Germany
[3] Siemens, Germany

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Speaker: Abby Shih, abby.shih@keysight.com

The Power Point Presentation will be available after the conference.

Abstract

This paper presents a new Artificial Neural Network (ANN) assisted in reverse recovery of a diode model for insulated-gate bipolar transistor (IGBT) devices at the turn-on process. The dependence of both carrier lifetime (τ) and diffusion transit time (T_M) on current, voltage and temperature in a diode model is modeled by ANN after a training process. The proposed diode model implemented in the Keysight IGBT model can accurately fit the transient i_C of an IGBT at a turn-on process for a wide range of currents at three voltages (100, 500 and 600 V) and three temperatures (25, 75 and 100°C). With a new parameter extraction workflow for transient simulation, an overall good fitting of the switching-on characteristics is achieved for an IGBT power module.

1 Introduction

IGBT power modules are widely used in power converters due to its simple gate driver, high switching frequency and optimal capacity with high current and voltage [1–3]. The development of power electronic modules with parallel chips will be very time consuming, if the switching behavior cannot be predicted. In contrast, unlike only one or several bias conditions that are provided and fitted for the transient waveform in most literature, such as [4–11], an accurate fitting of the transient waveform for an IGBT power module is required over a wide range of currents and voltages. This challenges both the stability and accuracy of an IGBT model.
The switching characteristics are measured with a double pulse testing (DPT) setup for IGBT devices

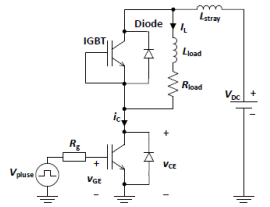
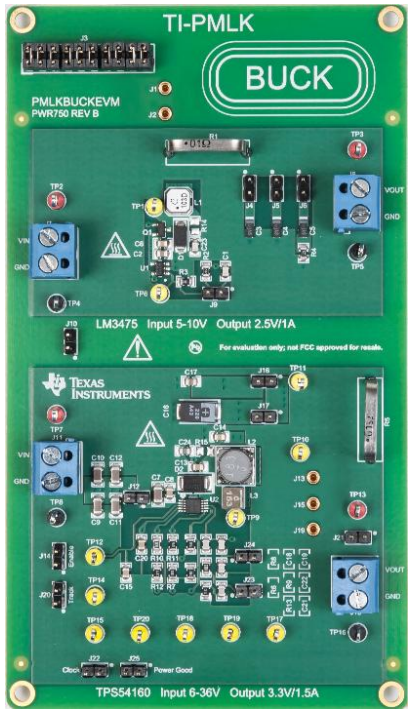


Fig. 1: The equivalent DPT circuit for IGBT transient turn-on simulation.

Siemens



Power Electronics EMI Laboratory

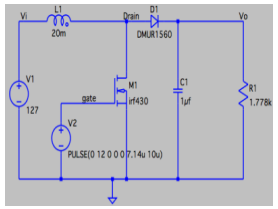
eBooks

Curated for power electronics engineers, this guide provides a hands-on learning experience to solve electromagnetic interference (EMI) challenges in next-generation power electronics design for electric vehicles, aerospace & defense, and new energy systems. It combines theoretical knowledge with practical experiments designed by Prof. Giulia Di Capua and Prof. Nicola Femia from the University of Salerno, Italy, offering a robust exploration of power electronics EMI fundamentals.

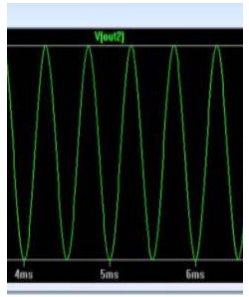
Texas Instruments / IPERA

Add Post-Layout Simulation

Schematic
(Ideal)

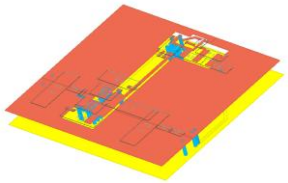


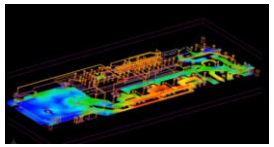
Draw circuit in schematic



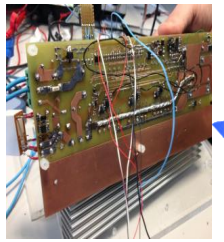
Simulate ideal conditions

Post-Layout Simulation
(Real World Effects in simulation)



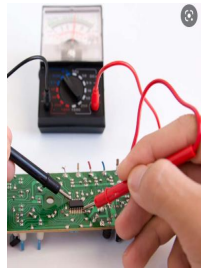


Prototype
(Real World)



1-2 spins
$6k-$60k/spin
3-8 weeks/spin

Test/Debug Validation
(Real World)



Switched-Mode Power Supply Design Workflow

Models

- SPICE Import
- PE Model Builder
- ADS Models

Schematic

- Thermal
- SMPS Performance Test Bench
- Transient PE
- Controllers for Closed Loop Design

Post-Layout

- Parasitic Extraction
- Thermal
- Conducted/Radiated EMI
- 3D Power Module

Power Electronics Models

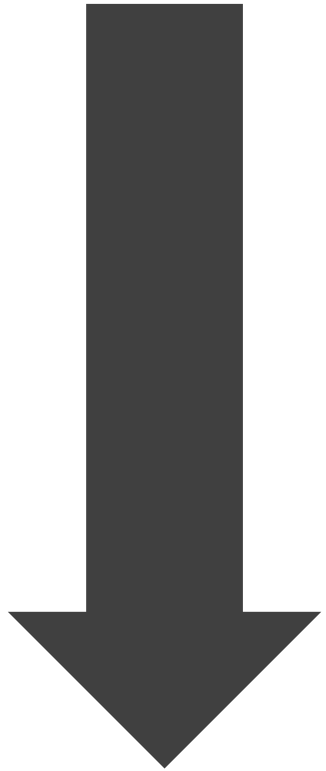
5 ways to build PE models in ADS – Huge Differentiation

- **Generic – Power Electronics Library**
- **LTspice/Pspice Import *(Vendor Model)***
- **Power Electronics Model Builder**
- **Measured Data (ICCAP, PEMG)**
- **Symbolically Defined Devices (SDD) / Verilog A**

EASY

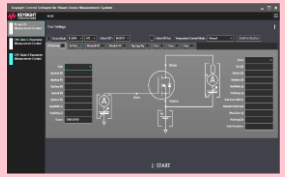
MEDIUM

HARD



Keysight PE Measurement and Modeling Solution

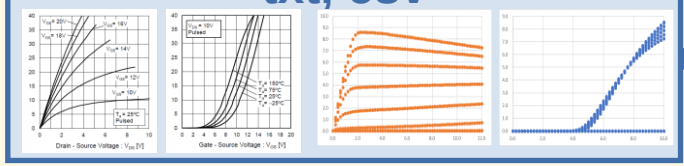
Control software : PD1000A



I-V & C-V : B1506A
S-parameter :
ENA+B2902+Bias-T

Switching : PD1500A

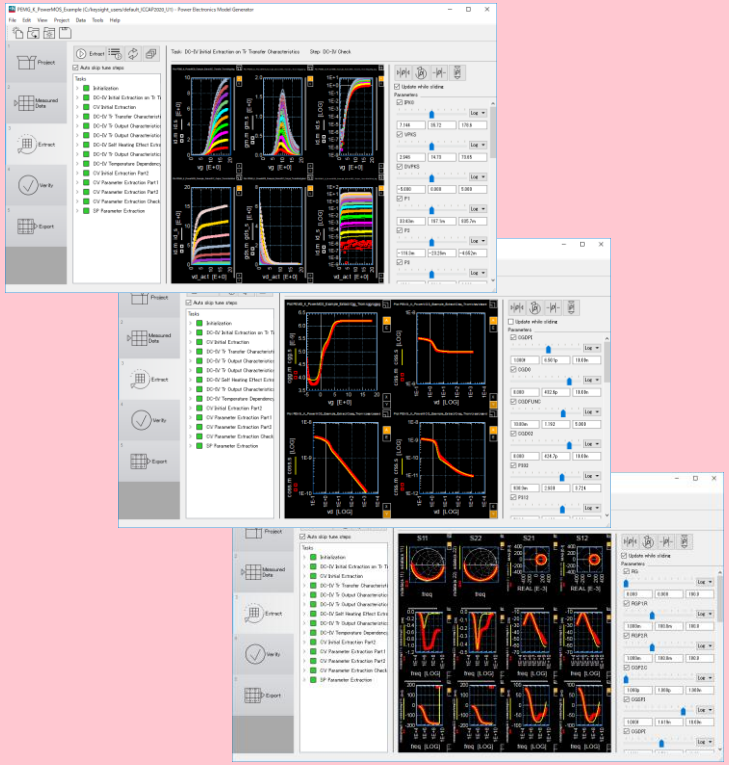
txt, csv

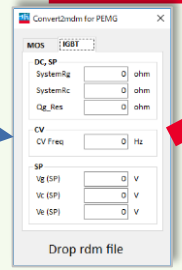


Measurement
(Supported by hardware team)

Meas File
.mdm

IC-CAP PEMG





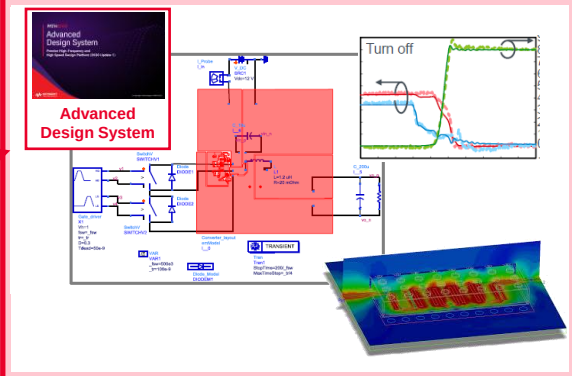
.mdm

Device Modeling
(Supported by EDA team)

Model Parameter
ADS

Model Parameter
PSPICE

ADS PEPro



PSPICE

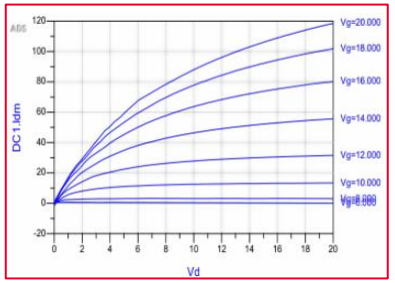
Circuit/EM simulation
(Supported by EDA team)

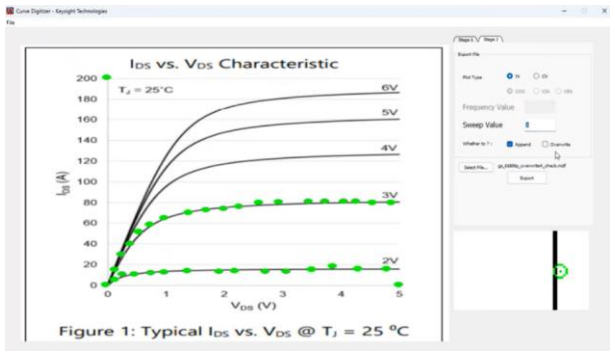
Power Electronics Model Builder

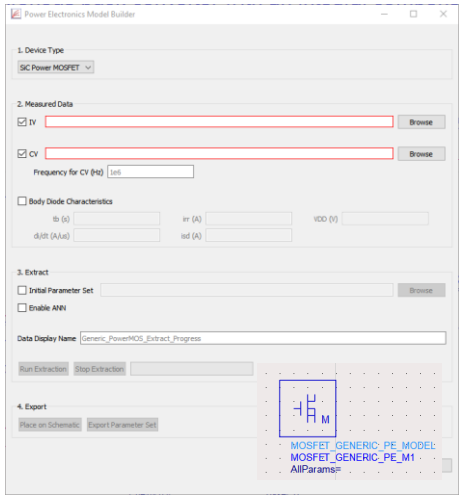
Digitize CV and IV Curve to Generate Switch Model

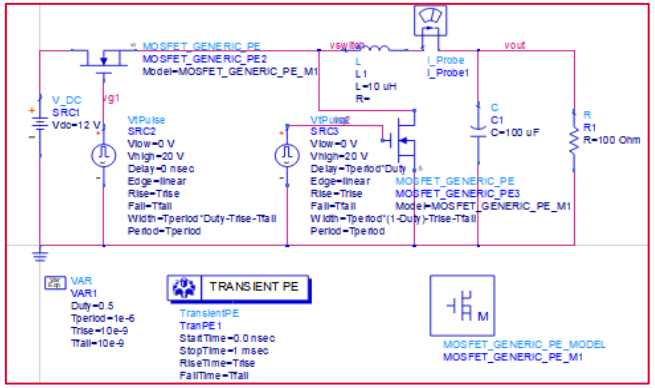
- Build the model directly from the datasheet: Si, Sic, IGBT, GaN

Input IV and CV Curve Image → CurveDigitizer extracts curve data → PEMB to extract model card → Use model in schematic

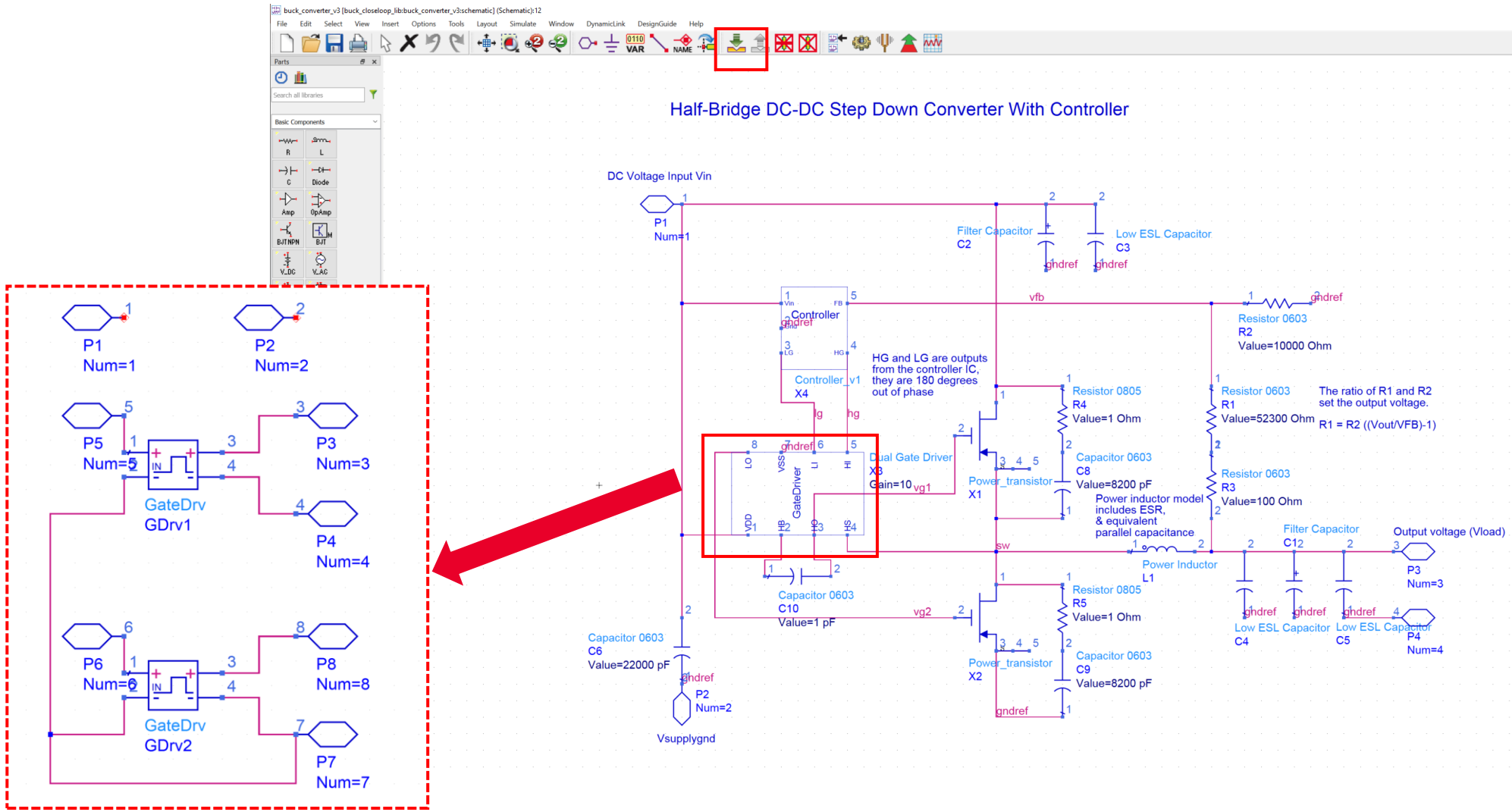






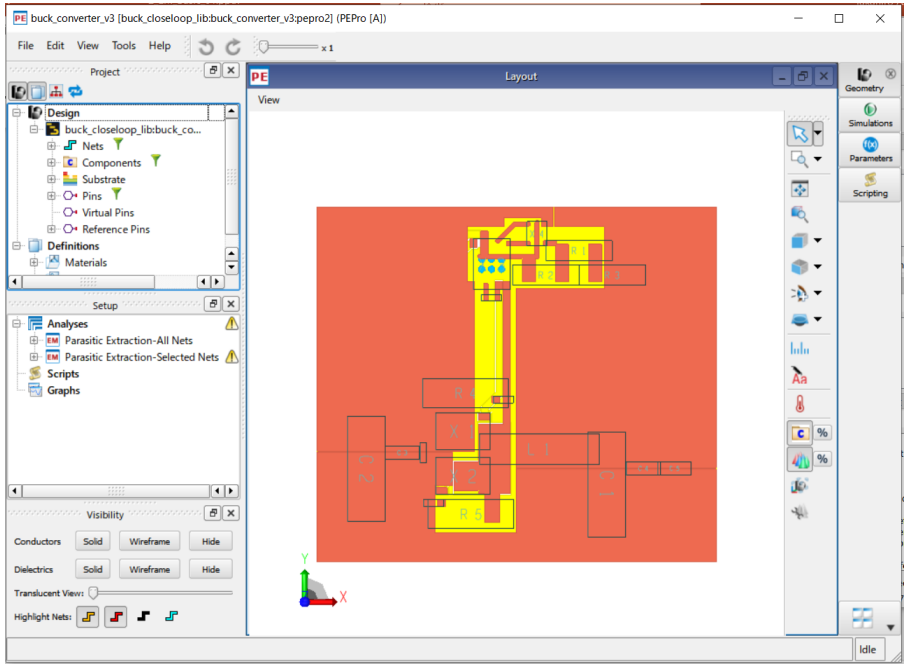


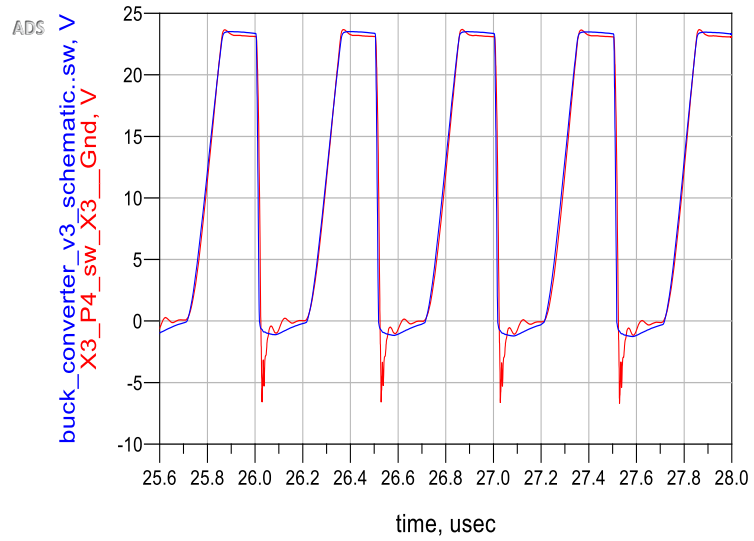
ADS Schematic Design Example



Analyze Effects of Parasitic Components

- Compare the presence or absence of the layout of the switching waveform inside the converter (effect of layout).

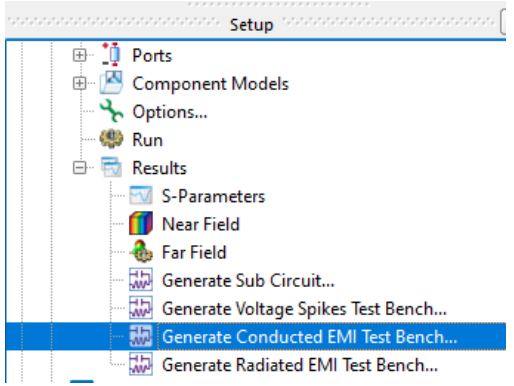


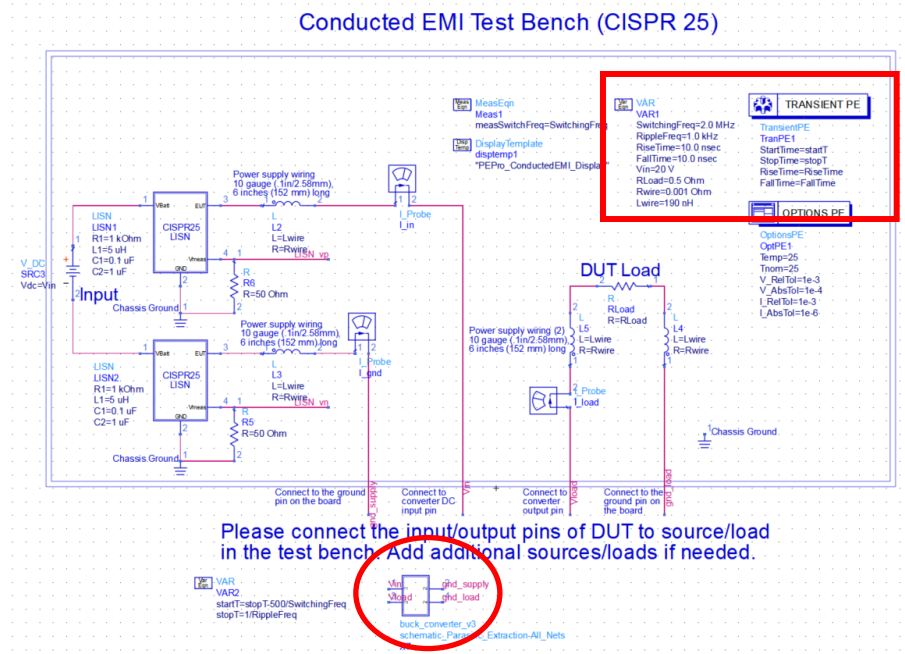


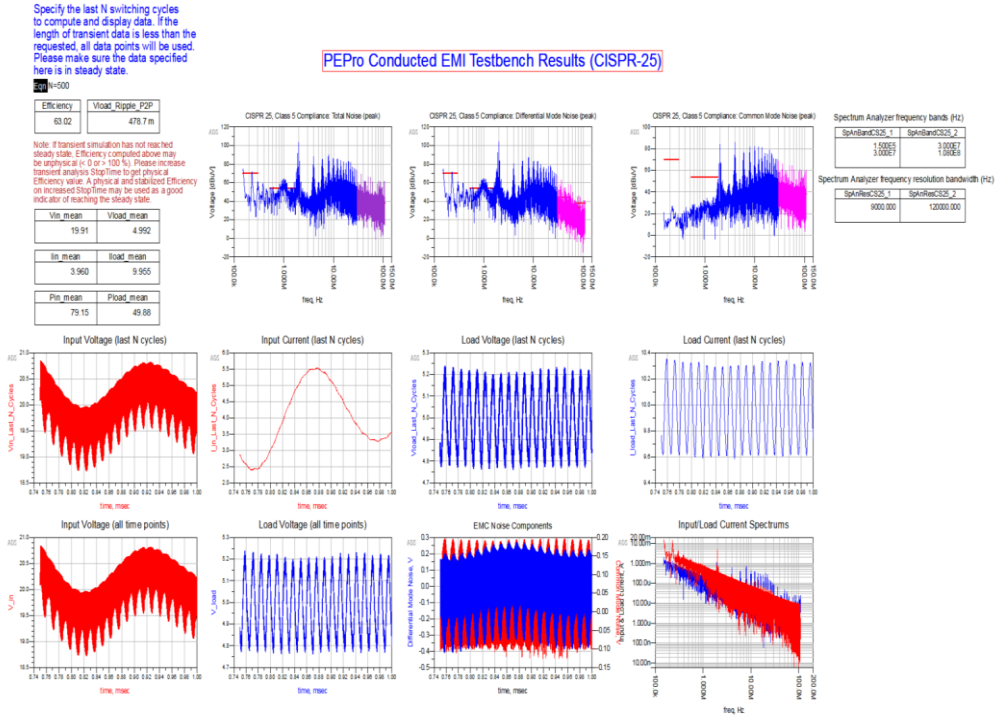
Blue lines: pure schematic simulation
Red lines: EM-transient co-sim

Conducted EMI Test Bench

- For this controller, the RiseTime and FallTime in Transient PE are from PEPro SMPS frequency plan.
- The Data Display shows the peak spectrum (total, differential / common mode noise) of SMPS noise calculated from the Linear Impedance Stabilization Network (LISN) output according to the CISPR-25 requirements of the frequency range and spectrum resolution RBW.



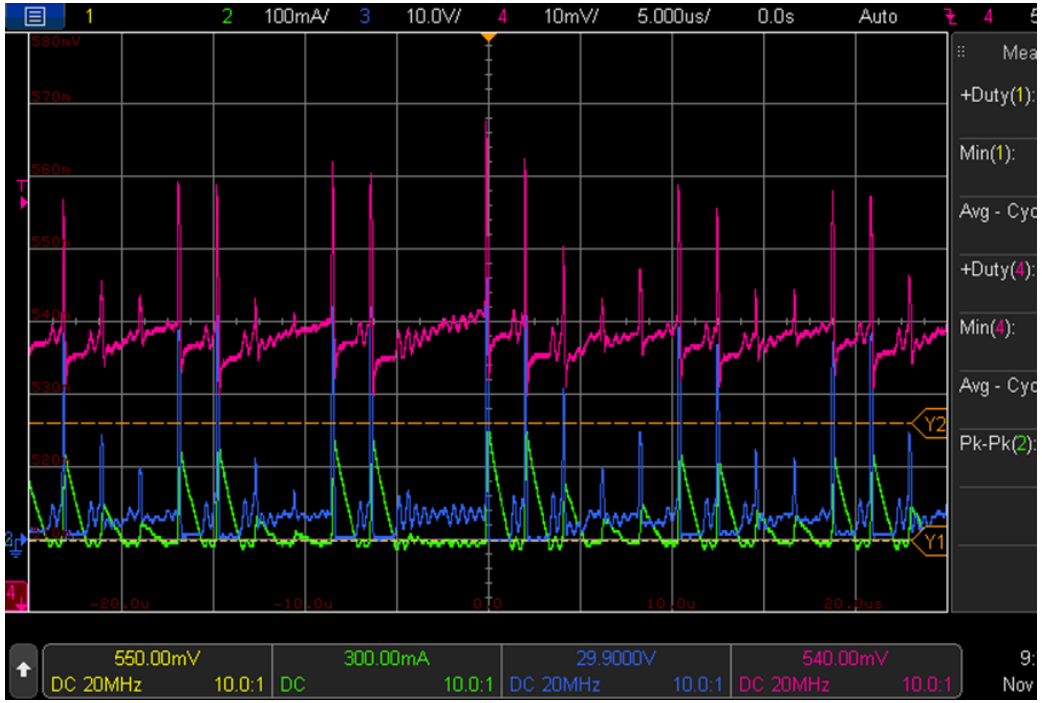


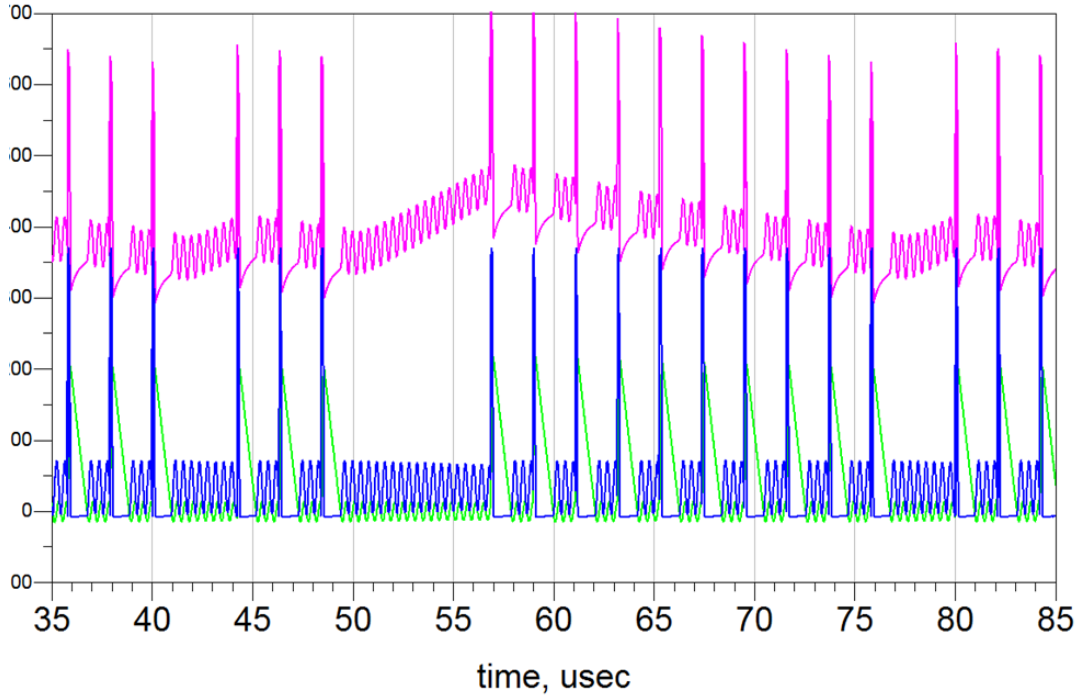


The EM analysis result of the board and the mounted parts are automatically placed as a sub circuit.

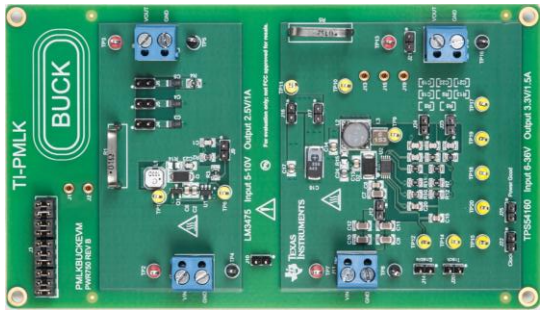
Measured vs. Simulated Example

Crosstalk on TI PMLK-BUCK Reference Board



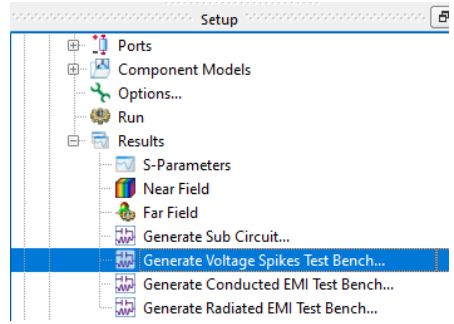


■ = switching node voltage, ■ = inductor current, ■ = error amplifier output



Voltage Spikes Test Bench

- A display plot of the pins on the net set as the "switching net" is automatically created after the simulation.



Last N Cycles

EqnlastNCycles = 2

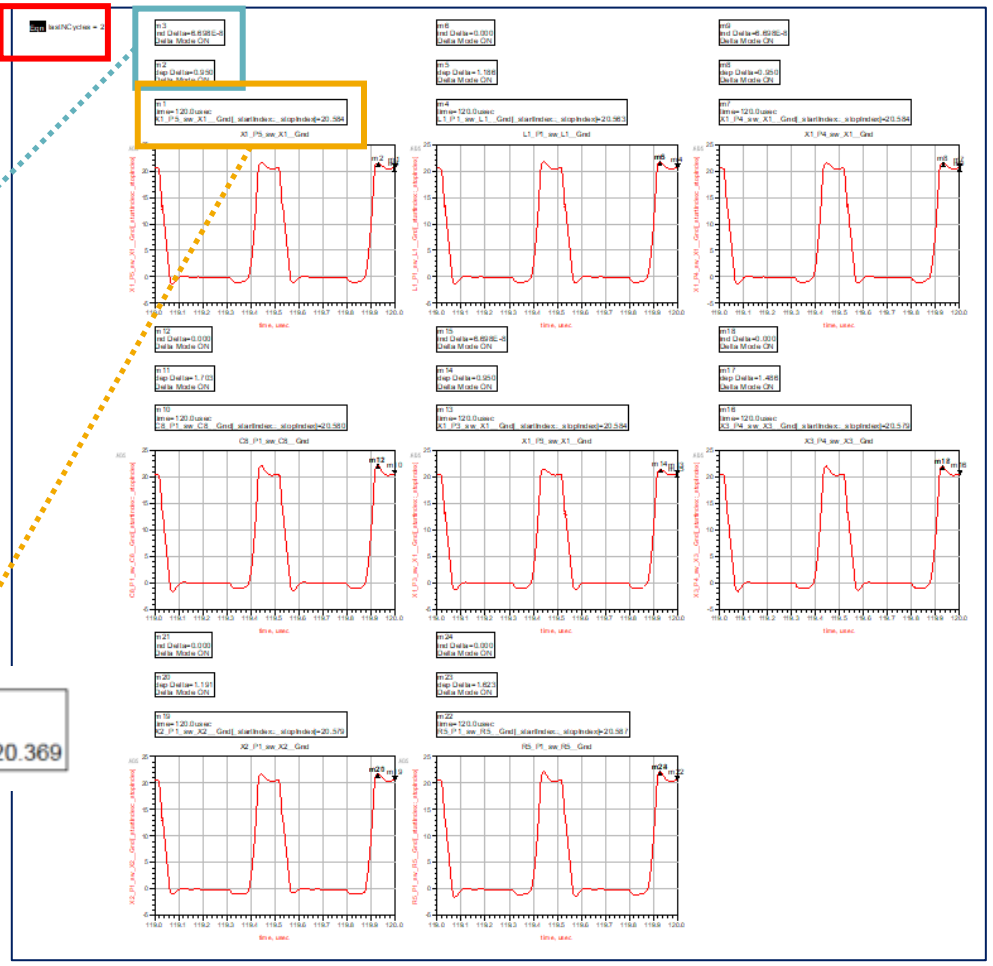
First Peak Marker
Second Peak Marker

m3
ind Delta=0.000
Delta Mode ON

m2
dep Delta=1.572
Delta Mode ON

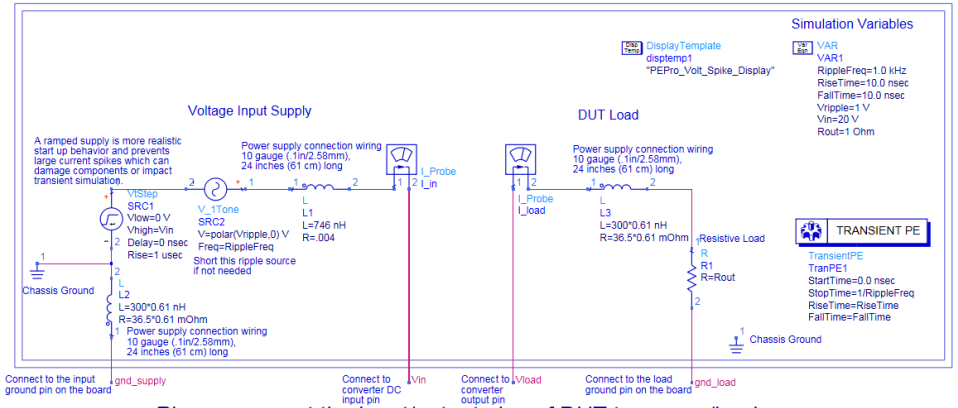
Baseline Marker

m1
time=120.0 usec
R5_P1_sw_R5__Gnd[_startIndex::_stopIndex]=20.369

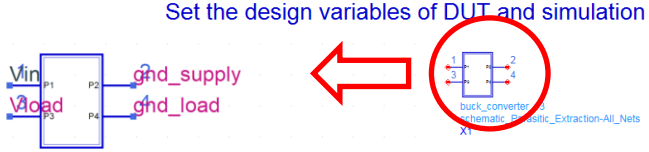


DC-DC Converter Test Bench

This testbench is used to test the voltage spikes appearing in the design during a normal startup condition. Transient controller has been set up to simulate using the user input value in PEPro. Please connect the device-under-test (DUT) to the source and load before starting the simulation. The present testbench is for single input and single output board design. If multiple inputs/outputs are present, please add additional source/load accordingly.



Please connect the input/output pins of DUT to source/load in the test bench. Add additional sources/loads if needed.
Set the design variables of DUT and simulation variables if needed.

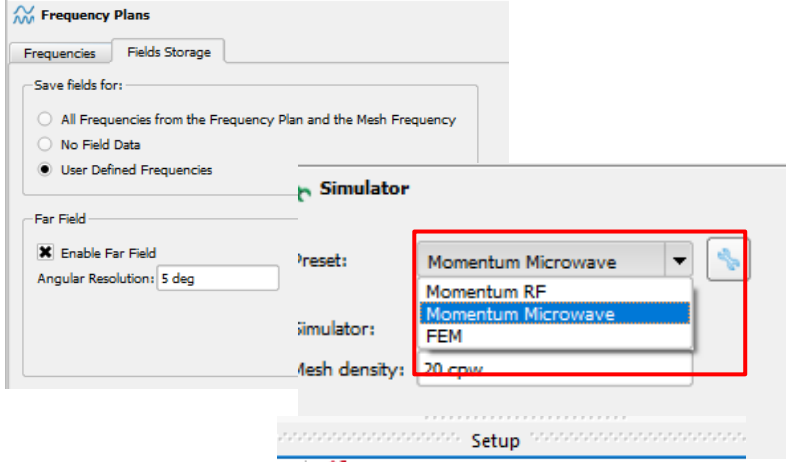


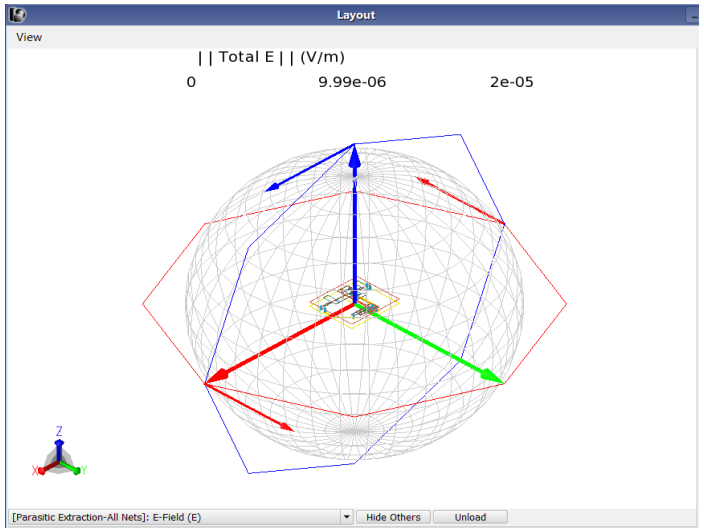
buck_converter_v3
schematic_Parasitic_Extraction-All_Nets
X2

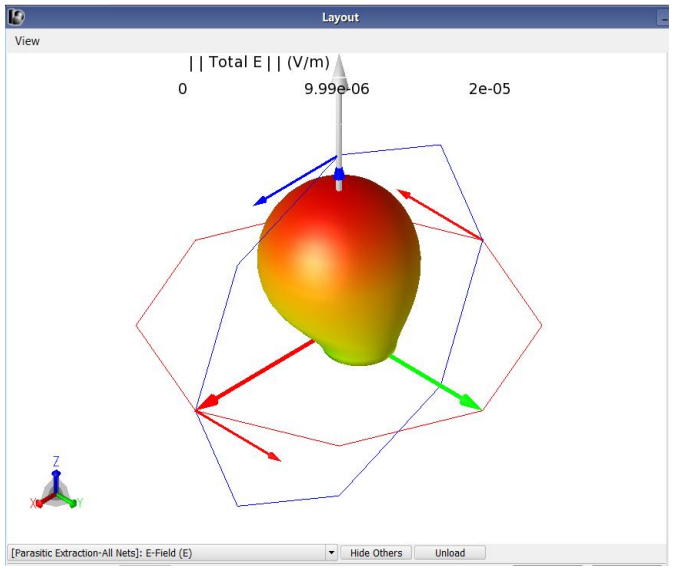
The EM analysis result of the board and the mounted parts are automatically placed as a sub circuit.

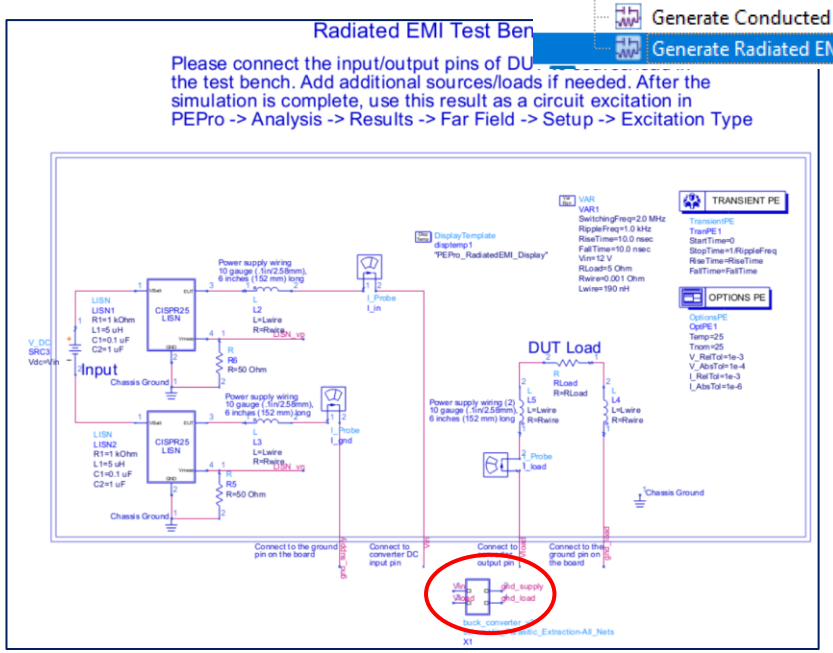
Radiated EMI Test Bench

- You need to check Enable Far Field in the Field Storage tab of Frequency Plans in Options and select Momentum Microwave or FEM in Preset of Simulator.
- The built-in far-field solver in PEPro can help user obtain far-field radiation patterns under specific excitation. The far-field data, including electric field strength and radiation power, can be examined directly in PEPro.

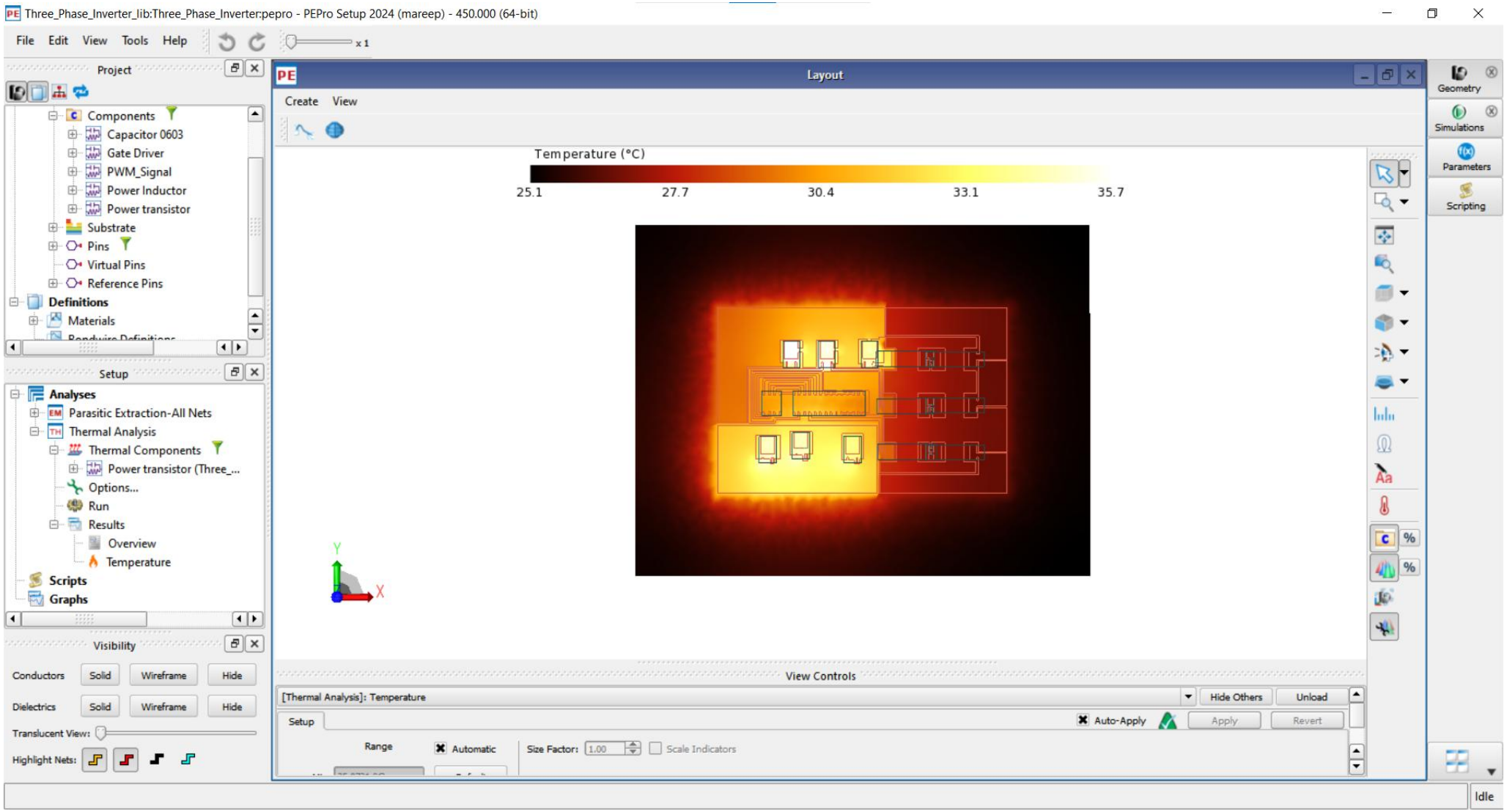






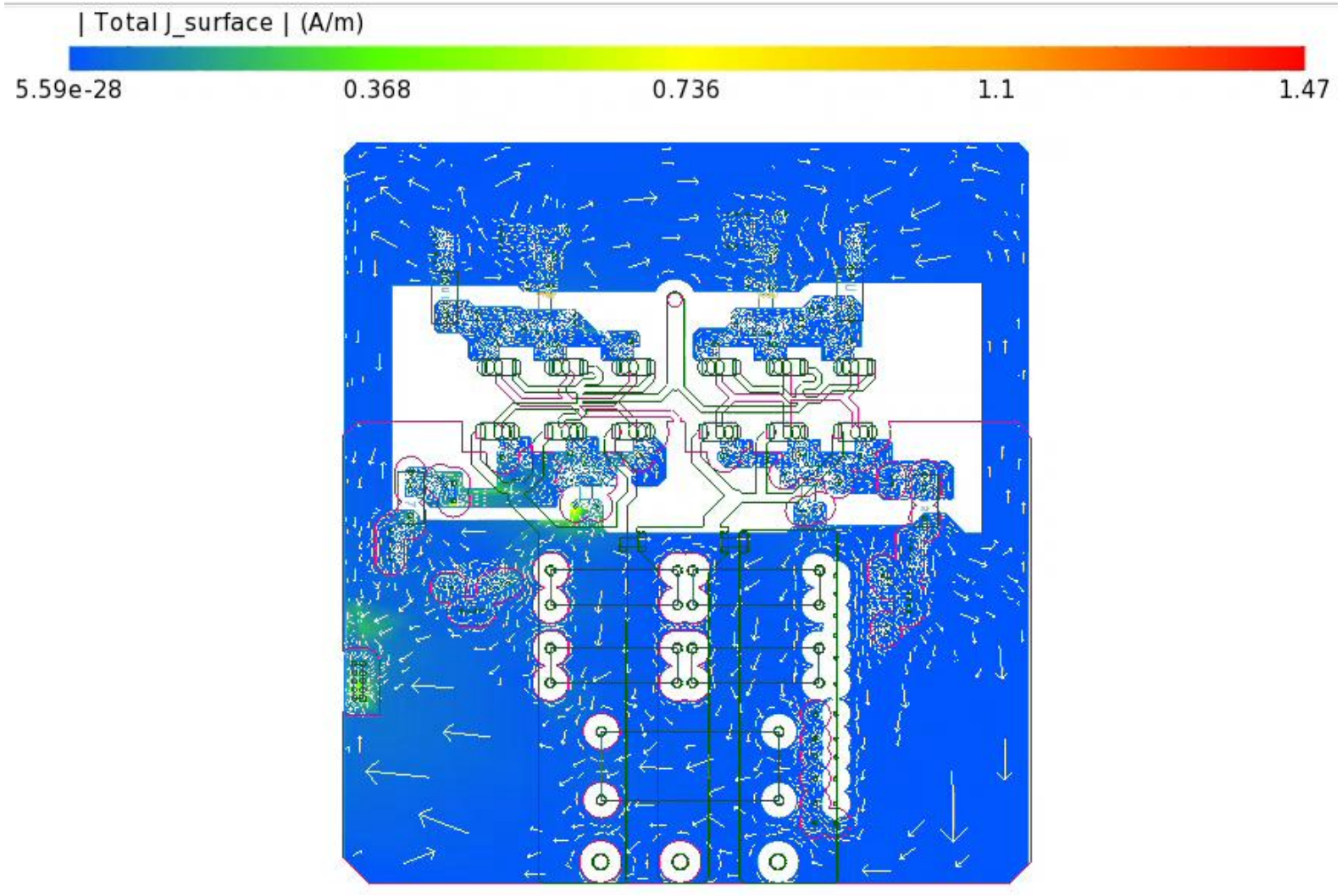


Thermal Analysis in PEPro



Surface Current Density

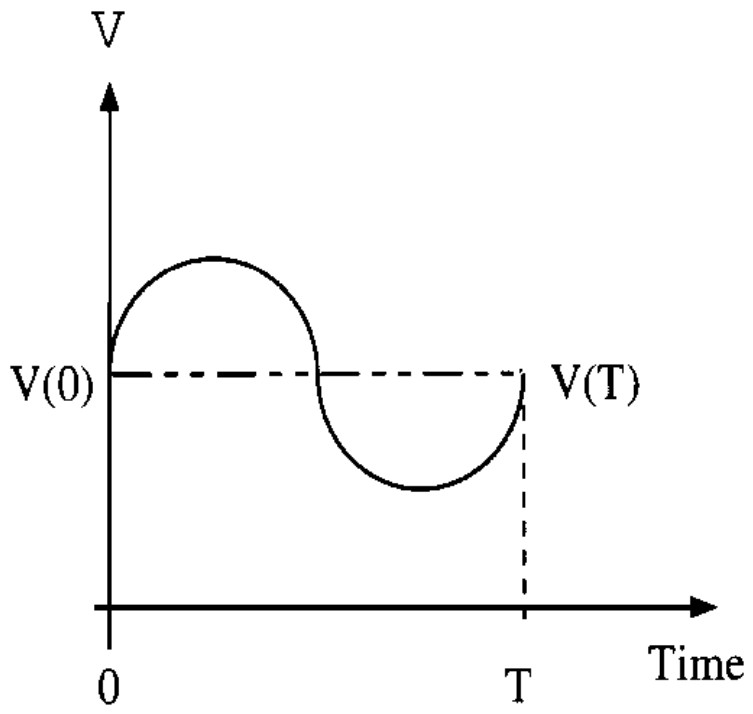
Identify areas of current crowding



Steady State Analysis

Shooting Newton

- Shooting analysis is a method to find steady state of circuits in time domain.
- Its counterpart in frequency domain is Harmonic Balance.
- In simple words:
  - Shooting runs transient for a period
  - Check if the final state at the end of a period same as the initial state.
  - If not, make some adjustment to initial state and run a period again.
  - If yes, steady state is found.

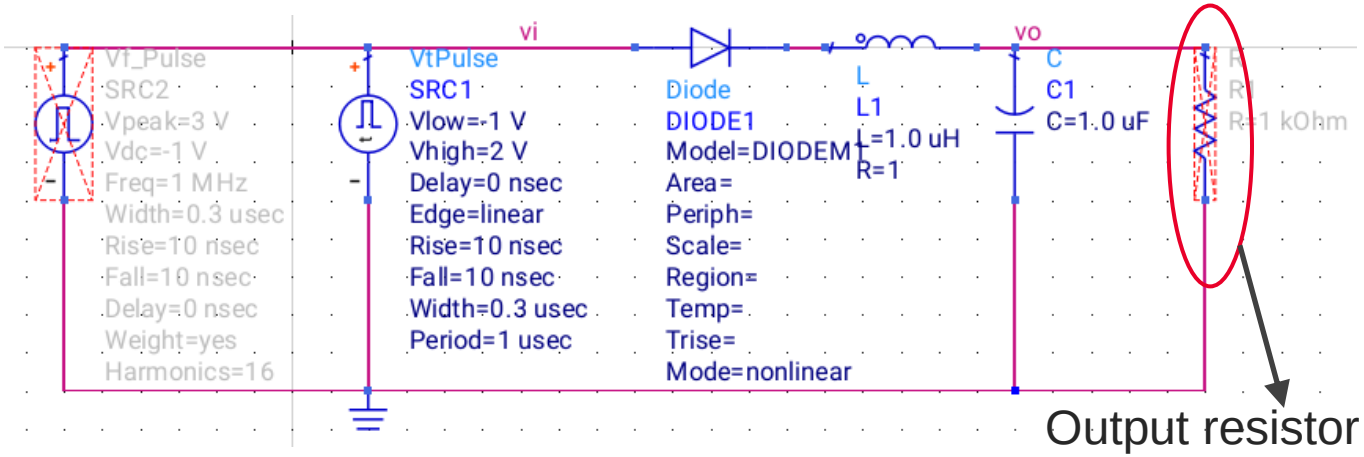


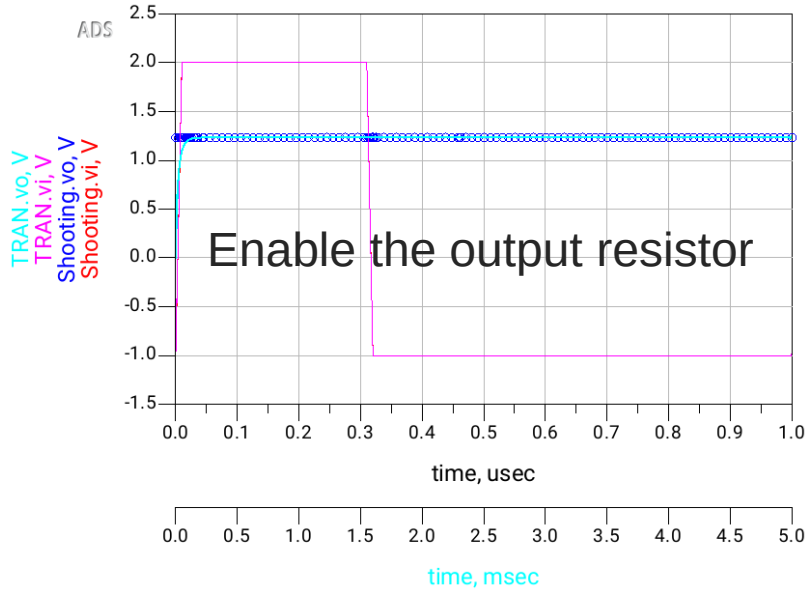
RC charging circuit

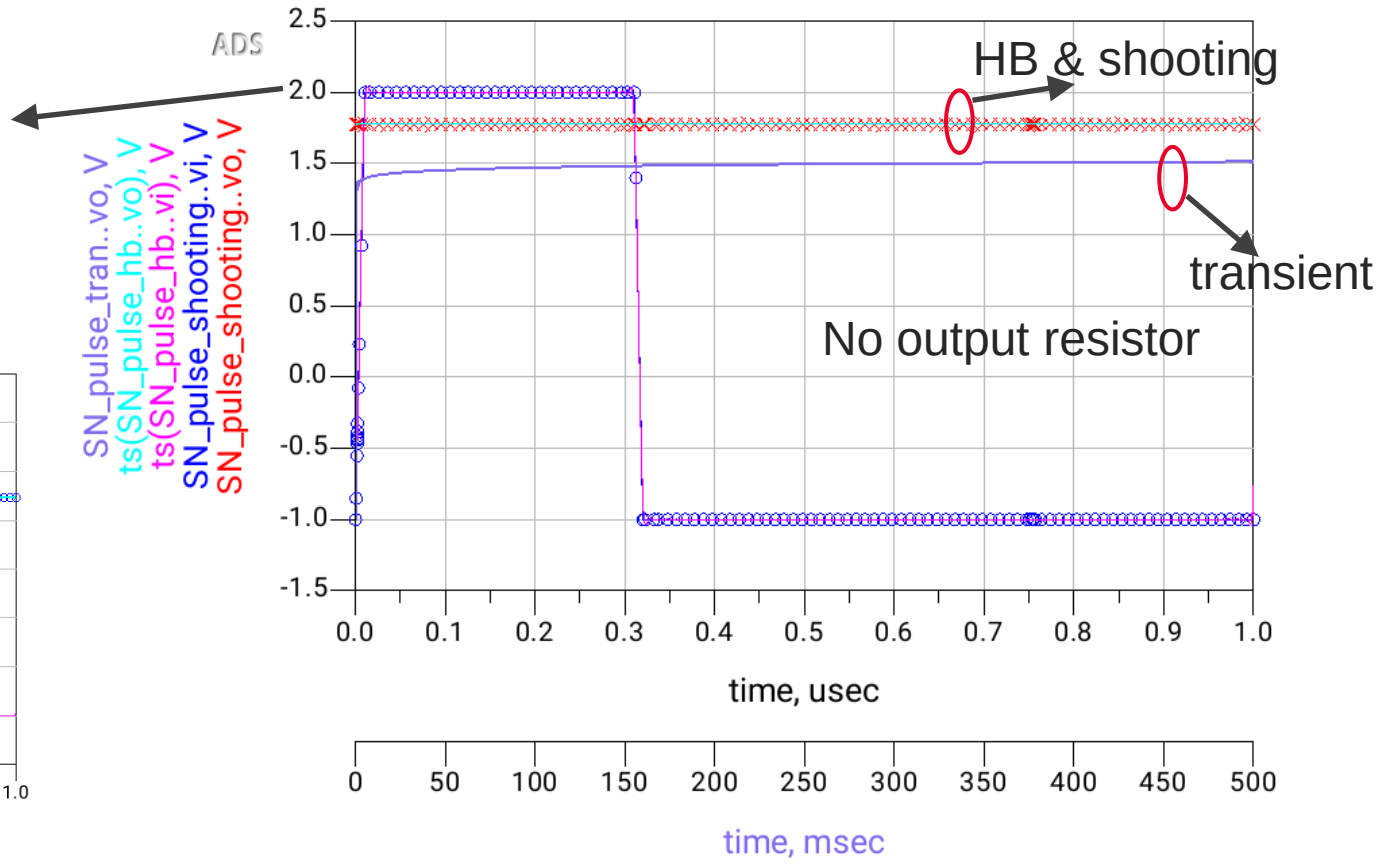
A simple test case for Shooting Newton

- Charge a large capacitor through a diode.
- Simulation without output resistor (linux RHEL8):

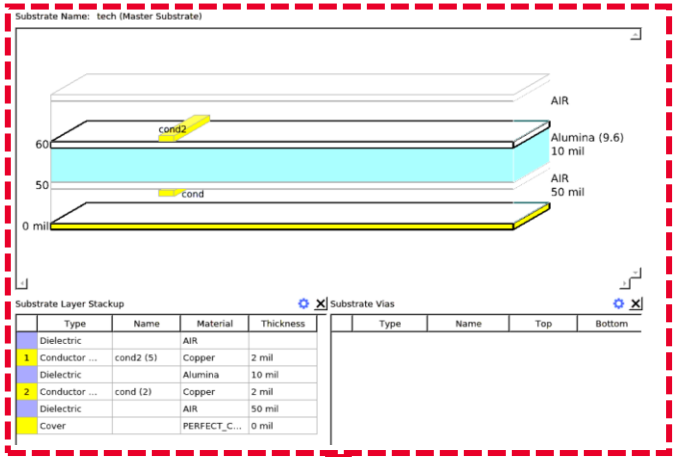
	Transient	Shooting
Simulation time	98.44s	0.79s



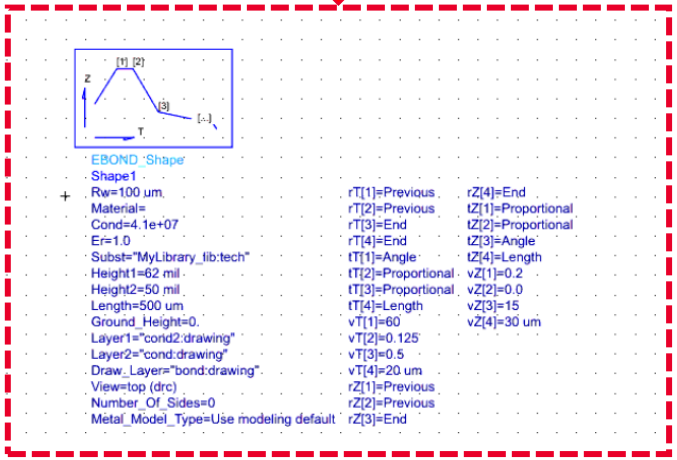




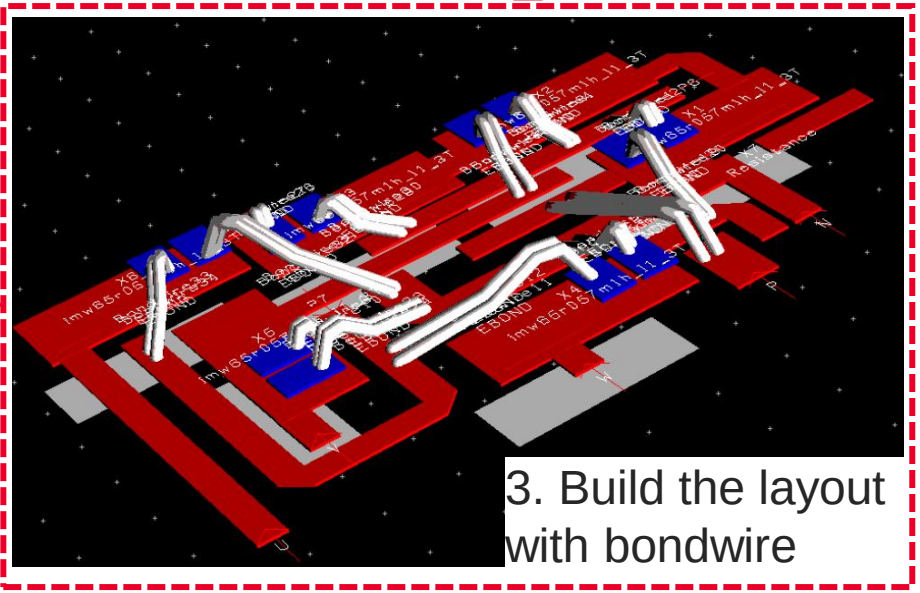
3D Power Module Workflow



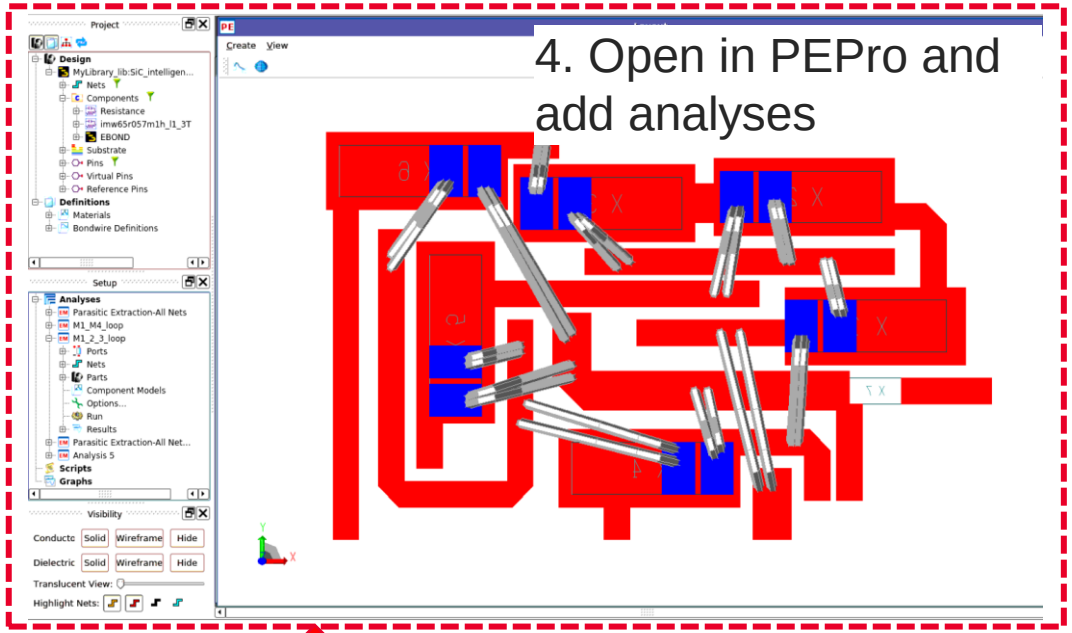
1. Setup the substrate



2. Setup the Shape of the bondwire

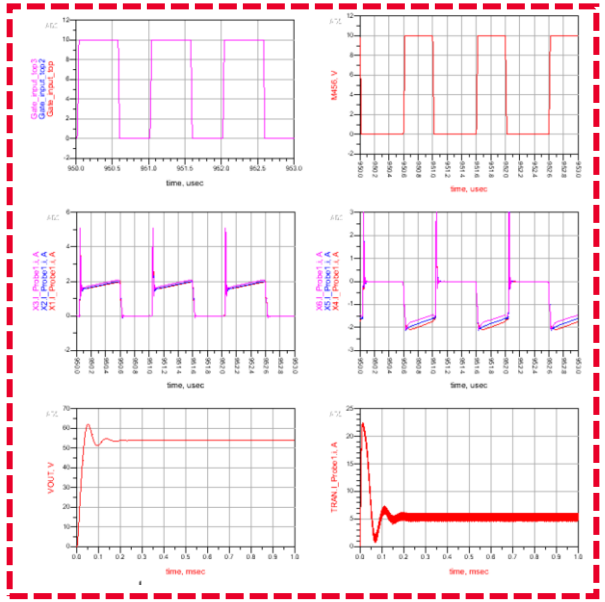


3. Build the layout with bondwire



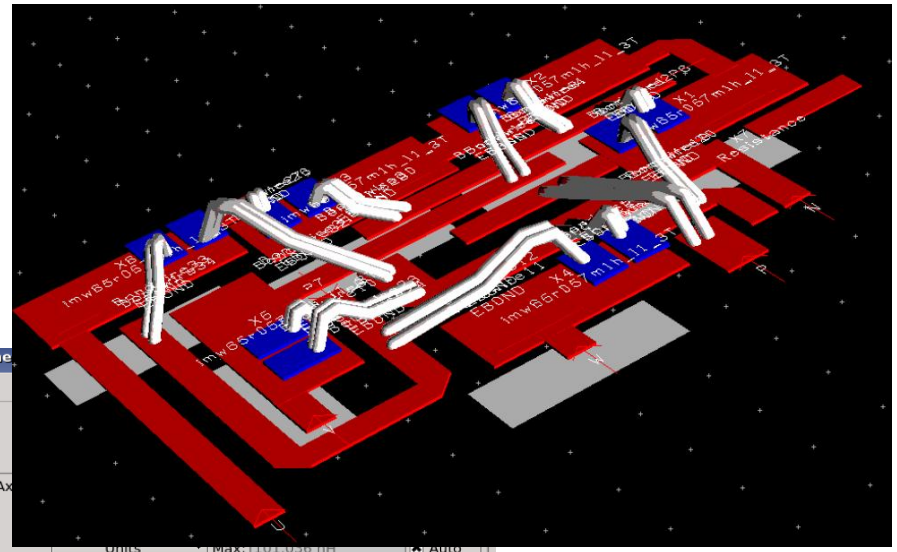
4. Open in PEPro and add analyses

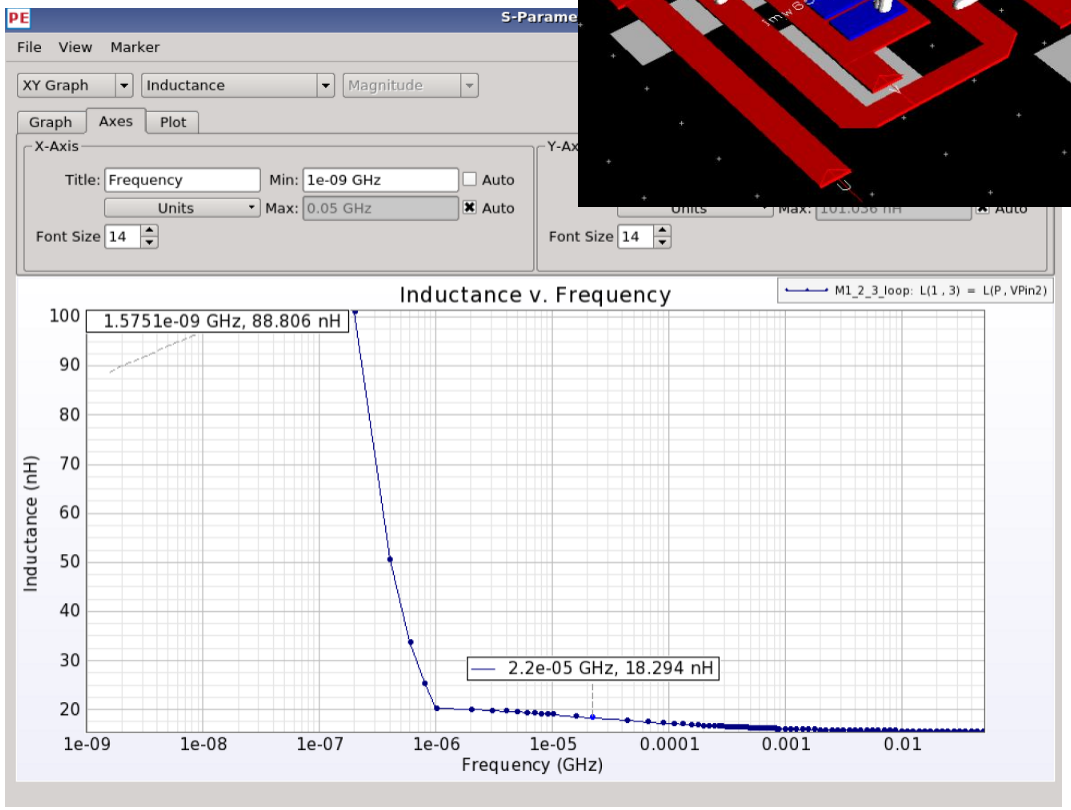
5. Use 3D power EM module in simulation

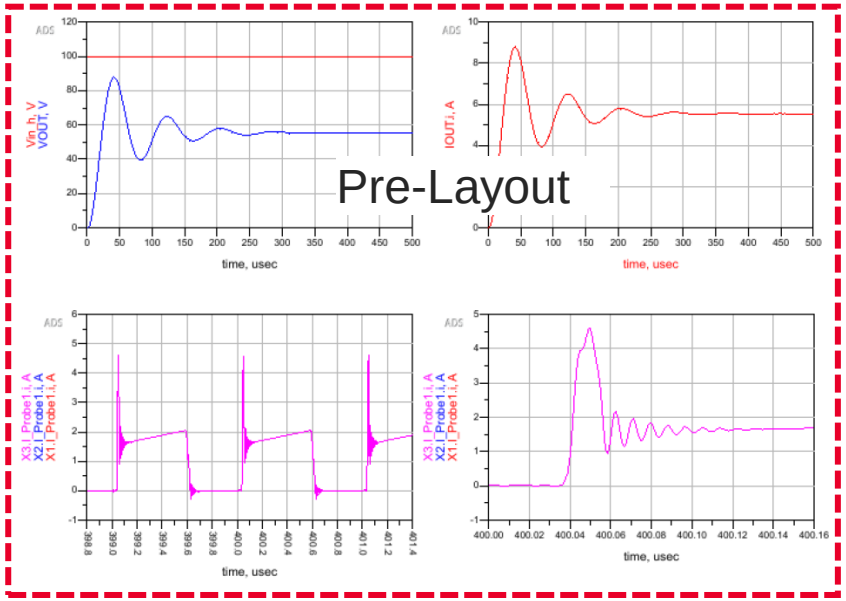


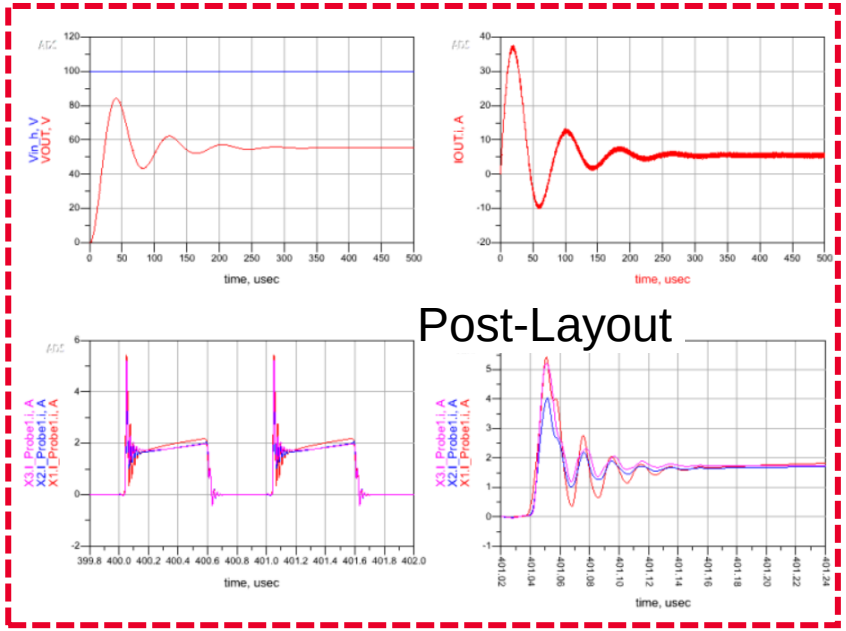
Basic PEPro Demo Guide

Comparison between Pre-layout and Post-layout









Agenda

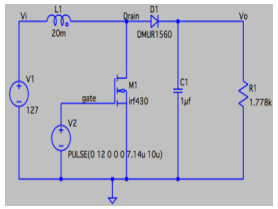
- Trends and Challenges in Power Converter Design
- Keysight ADS and PEPro Electromagnetic Simulation Solution
- **Demo**
- Summary

Agenda

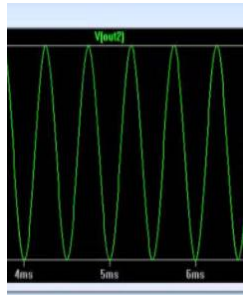
- Trends and Challenges in Power Converter Design
- Keysight ADS and PEPro Electromagnetic Simulation Solution
- Demo
- **Summary**

Add Post-Layout Simulation

Schematic
(Ideal)

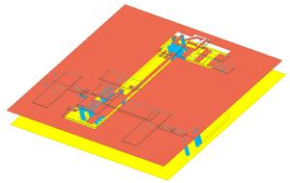


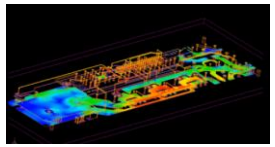
Draw circuit in schematic



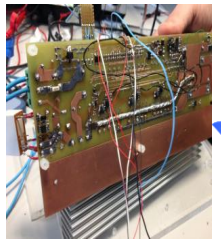
Simulate ideal conditions

Post-Layout Simulation
(Real World Effects in simulation)



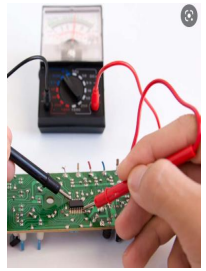


Prototype
(Real World)



1-2 spins
$6k-$60k/spin
3-8 weeks/spin

Test/Debug Validation
(Real World)



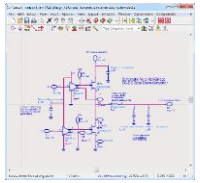
Key Takeaways

- Traditional workflows don’t work with new wide bandgap designs
- Post-layout simulation maximizes precision and accuracy
  - PEPro parasitic extraction offers insights you can’t get from basic circuit simulators
  - Unique Thermal + EMI insights in this workflow translate to less time prototyping and debugging
  - Only this ADS+PEPro workflow offer all these toolset in a single platform
- Do more simulation = Faster time to market

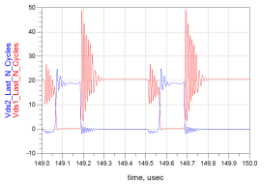
W3631B Power Electronics Bundle

All in one solution for switched-mode power supply design and more

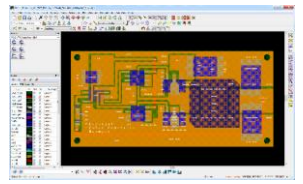
Power Electronics Models



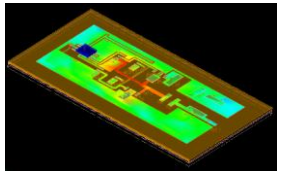
Schematic



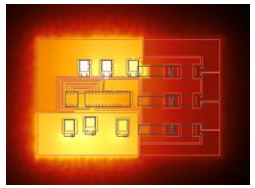
Transient Simulator



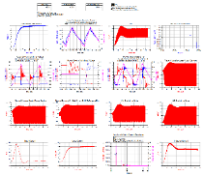
Layout Tool



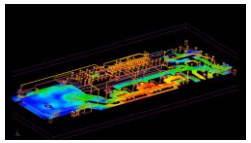
PEPro: EM Field Solver for PCB Parasitic Extraction



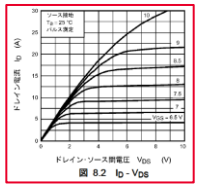
Thermal



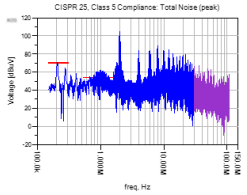
Data display



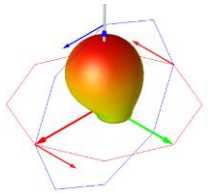
Circuit Excitation Display Current Density



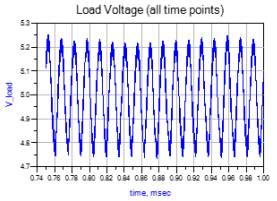
Datasheet Model Builder



Conducted EMI/EMC Test Bench



Radiated EMI/EMC Test Bench



Voltage Spike Test Bench

KEYSIGHT

Thank you


KEYSIGHT

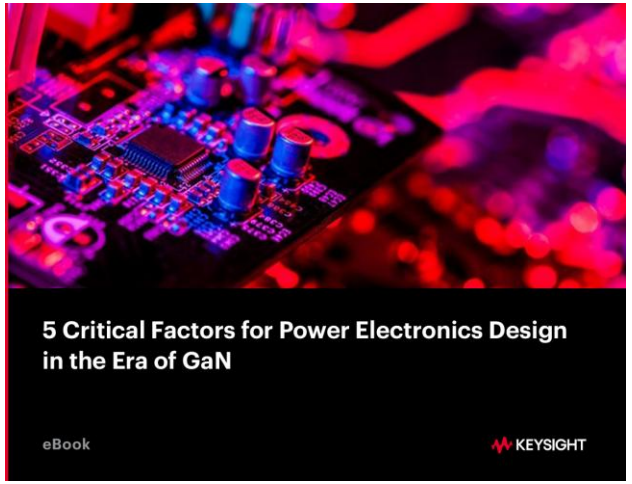
EMI Curriculum Available NOW

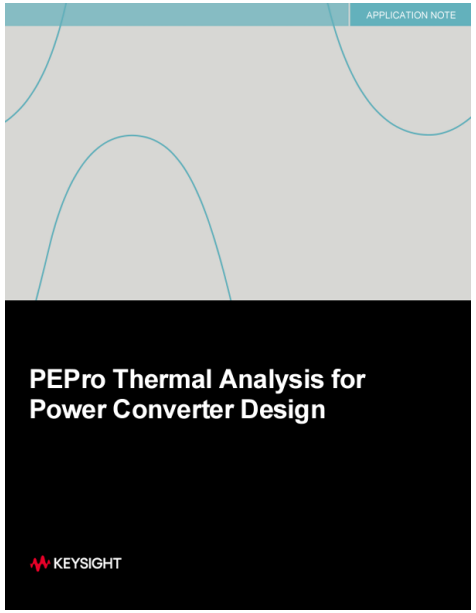
https://www.keysight.com/us/en/assets/7123-1100/ebooks/Power-Electronics-EMI-Laboratory.pdf

Learn more about Keysight Power Electronics Design

Guides, Overviews, App Notes, eBook

- PE Bundle Overview
- Quick Start Guide
- eBook: 5 Critical Factors for Power Electronics Design in the Era of Gan
- **Application Notes**
  - PE Thermal Analysis
  - Designing a SMPS using soft switching
  - 3D power module simulation
  - Parasitic extraction of inverter design
  - PE Curriculum Handbook for EMI

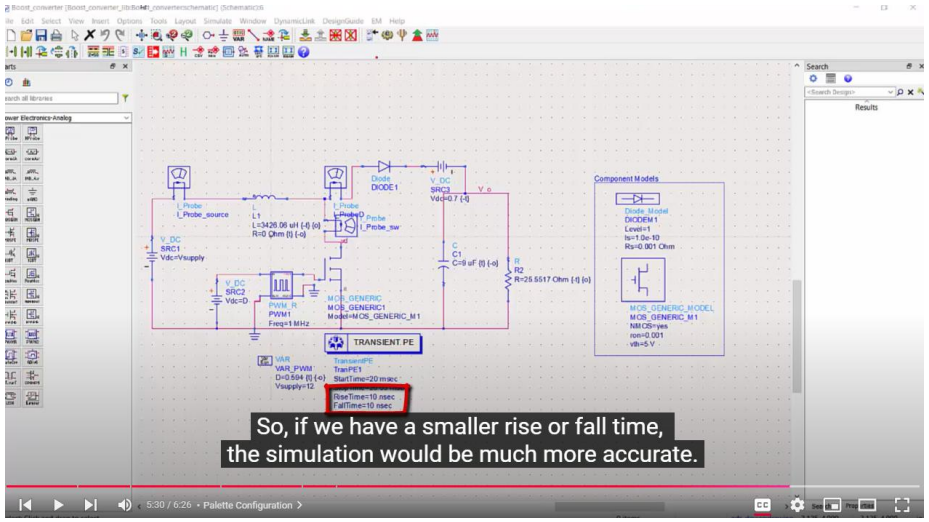


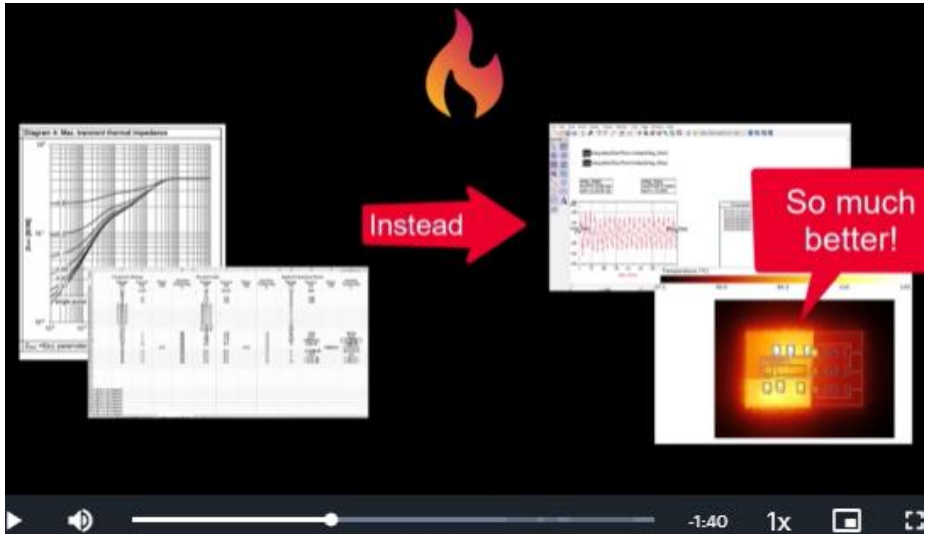


Learn more about Keysight Power Electronics Design

Videos

- **Videos**
  - Shooting Newton steady state solver
  - PE Thermal Analysis
  - Power Electronics Tutorial
    - Getting started
    - Designing your first switching device
    - Optimize your SMPS
    - Preparing your design for PEPro simulation





Learn more about Keysight Power Electronics Design

Technical Papers – PE Modeling

GaN Power Transistors Behavioral Modeling

Giulia Di Capua [1, 3] and Nicola Femia [2, 3]
[1] University of Cassino and Southern Lazio, Cassino (FR), ITALY
[2] University of Salerno, Fisciano (SA), ITALY
[3] IPERA S.R.L., Fisciano (SA), ITALY
e-mail: { giulia.dicapua@unicas.it , femia@unisa.it }

Abstract — **This paper discusses the behavi Gallium Nitride (GaN) power transistors for voltage/current waveforms and losses in hard-s Mode Power Supplies (SMPSs), with main emp and C-V characteristics. A new technique ex characteristics to high drain-source voltage is different capacitance models are also compare models are fully based on device datasheet curv implemented in PathWave Advanced Design S allowing easy construction of symbolically de 350 V/3 A boost converter is considered as a ca half-bridge of two 650 V-30 A GaN power tran**

Keywords — **Gallium Nitride, Modeling, Po Simulation.**

I. Introduction

Compared to Silicon (Si)-based MOSFETs, High Electron Mobility Transistors (GaN HEM specific on-resistances and capacitances, all achieve higher Switch-Mode Power Sup efficiency and power density at megahertz frequency [1]. The unprecedented perform HEMTs enable the design of SMPSs featuring density figures, as required in the next gene electronics applications [2], [3].

The Synchronous Half-Bridge (SHB) cell is high-efficiency SMPSs [4]. A GaN-based SH is shown in Fig. 1. Depending on the s topology, the V_{off} voltage can be the input vol output voltage (boost), or the input-output boost), whereas the I_m current is always the at the instant of the commutation. Due to the switching speed, the very high di/dt and dv each SHB commutation deeply impact the SM and determine voltage surges between the ga the device that is turning off. This can cause c if the gate-source threshold voltage value is problem is typically prevented in GaN-base negative bias gate-driver voltage at the tu negative bias must be limited as much as possi of the GaN devices operating in the reve increase as the magnitude of the negativ increases. A correct prediction of the possibl the gate-source voltage surges causing cross- help in assessing whether the negative gate bi what is its right voltage value [5]. In general voltages and resistances must be set base characteristics, to figure out the optimal Unfortunately, the current-versus-voltage char V_{DS} of GaNs are provided only at low vol prediction of GaN drain currents over the voltage of the application is needed to correc driver parameters and determine the con required at the device turn on and turn off.

979-8-3503-3265-0/23/$31.00 ©2023 IEEE

Power Losses Analysis of SiC MOSFETs in DC-DC Converters with High-Ripple-Current Inductors

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[1] University of Salerno, Fisciano (SA), ITALY
[2] AeroVironment Inc., Arlington, VA, U.S.A.
[3] University of Cassino and Southern Lazio, Cassino (FR), ITALY
[4] IPERA S.R.L., Salerno (SA), ITALY
e-mail: { femia@unisa.it ; Jafarian@avinc.com; giulia.dicapua@unicas.it }

Abstract— **This paper discusses behavioral models for power losses analysis of Silicon Carbide (SiC) MOSFETs in DC-DC converters, with emphasis on the impact of inductor saturation and peak-peak ripple current. All models are implemented in PathWave ADS software, by using symbolically defined devices. A PV-MPPT DC-DC boost converter is considered as a reference case study. The results confirm the advantages of working with large peak-peak ripple and partial saturation of power inductors.**

Keywords— SiC, power inductors, power losses, saturation, modeling, DC-DC converters, simulation.

I. Introduction

High efficiency, small volume, and low weight are among the most important targets in power electronics. The technical literature emphasizes the major impact of the cost and size of magnetic components on efficiency in PhotoVoltaic (PV) Maximum Power Point Tracking (MPPT) power converters [1]. Increasing efficiency and reducing volume and weight have priority in PV-powered Unmanned Aerial Vehicles (UAVs) [2]. The volume and weight of PV systems can be reduced by using nonlinear power inductors.

Nonlinear inductors in L-type filters of grid-connected PV inverters have been investigated for several years. In particular, the impact of inductor nonlinearity on the performance of PV controllers has always been the main concern. In [3], a nonlinear inductance model was developed allowing to prove how the harmonic compensation provided by resonant controllers can mitigate the effects of the grid filter inductor saturation. In [4], the effect of nonlinear grid filter inductors on the low-frequency and switching-frequency current harmonics produced by the inverter was investigated. In [5], LCL-type grid filters were studied, confirming good attenuation capabilities in grid-connected PV inverters, with smaller sizes if compared to standard L-type filters, at the price of additional components (two inductors and one capacitor). Beyond grid filters, the use of nonlinear power inductors in the voltage-boosting DC-DC converter stage of a PV system can offer further advantages. It has been proved that accepting a partial saturation of Ferrite Power Inductors (FPIs) can be a way to reduce the DC-DC converter size and achieve higher power density [6]. Although traditional bigger-core non-saturated FPIs can present lower peak-peak ripple current and temperature rise, smaller-core inductors working in partial saturation may operate with acceptable power losses, faster, ensuring lower switching losses, especially if High-Current Ripple (HCR) operation modes are verified [10]. Operating at higher switching frequencies, WBG devices enable passive components volume reduction and consequent power density increase. But, to fully exploit their capabilities, WBG devices must be accurately modeled to capture system design solutions that optimally combine nonlinear power inductors, gate driving setup, and switching characteristics.

This paper analyzes the combined impact of FPIs with large peak-peak ripple current and operating in partial saturation on the power loss performance of a SiC-based DC-DC converter, using analytical behavioral models of SiC and FPI devices, both generated starting from the experimental data included in their datasheets. Section II illustrates the $I_{DS} - V_{DS}$ and $C - V_{DS}$ characteristics of SiC devices and their analytical behavioral models. Section III studies the $L - I$ characteristic of FPIs and their analytical behavioral modeling. Section IV shows the implementation of SiC and FPI behavioral models in PathWave ADS software [11]. Section V presents the simulation results of an aerospace 200 kHz PV-MPPT boost DC-DC converter, powered by a PV source characterized by $V_{oc} = 143$ V, $I_{sc} = 9.5$ A, $V_{MPP} = 125$ V and $I_{MPP} = 8.3$ A under Standard Test Conditions (STC), charging a 400 V battery pack, and working at an ambient temperature T comprised between 233 K and 313 K (about −40°C and +40°C).

II. Modeling SiC MOSFET Characteristics

The first and third quadrant $I_{DS} - V_{DS}$ characteristics of the SiC MOSFET C3M0065090J are shown in Fig.1 for positive, negative, and zero gate-source voltage, at an operating junction temperature of −55°C [12]. Using Genetic Programming algorithms [13] allows to generate behavioral models of power devices starting from experimental data [14]. Applying that technique to the C3M0065090J data yields the inverse tangent series given in (1):

$$I_{DS}^{V_{GS}}(V_{DS}) = \sum_{k=1}^{N} i_{1k}^{V_{GS}} \, atan\left[i_{2k}^{V_{GS}}\left(V_{DS} - i_{3k}^{V_{GS}}\right)\right] \qquad (1)$$

where the series order N and the coefficients $i_{1k}^{V_{GS}}$, $i_{2k}^{V_{GS}}$, $i_{3k}^{V_{GS}}$ can be optimized for each V_{GS} value using a Non-Linear Least Square (NLLS) algorithm, starting from the sampled data of the curves shown in Fig.1. For the first quadrant characteristics, $N = 2$ is normally sufficient, whereas for the third quadrant characteristics $N \geq 4$ can be required. Model (1) can be developed at any available junction temperature.

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An ANN Assisted Reverse Recovery of Diode Model for Switching-on Characteristics of IGBT Devices

Huaiyuan Zhang[1], Abby Shih[2], Stefan Haensel[3], Zeeshan Umar[3], Steven Lee[1], Felix Zeyss[3]

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Corresponding author:
Speaker:

The Power Point Prese

Abstract

This paper presents a ne for insulated-gate bipola carrier lifetime (τ) and di modeled by ANN after a model can accurately fit three voltages (100, 500 extraction workflow for t achieved for an IGBT po

1 Introduction

IGBT power modules are verters due to its simple frequency and optimal and voltage [1–3]. The d tronic modules with para consuming, if the switchi dicted. In contrast, unlik conditions that are provi sient waveform in most an accurate fitting of the IGBT power module is re of currents and voltages. stability and accuracy of The switching characteri double pulse testing (DP with the freewheeling di power module. Fig. 1 s circuit for IGBT transient the DC supply voltage. source. R_g is the gate re inductance. L_{load} and R_l and resistance, respecti i_C, v_{GE} and v_{CE} are the

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Semiconductor Chip Models are the Key for Enabling Virtual Design and Optimization Workflows of Power Electronic Systems

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[2] Keysight Technologies, Germ

Corresponding author: Stefan
Speaker: Stefan

Abstract

Virtual optimization of power exactly describe the switching combined static and dynamic which enables semiconductor workflow three different IGBTs results are promising and enab required for a complete optimiz

1 Introduction

Power electronic systems integral part of our everyday li /power supplies in the electromobility up to the integr sources and energy distributio in all applications is the pow which influences the overall terms of electrical behavior, co gate driver circuits, filter compo effort. Virtual design of po optimization of complete conve with a sufficiently accurate semiconductor switching beha cover various influences, e. current sharing of parallel di module or over-voltage in points. A lot of experience a iterations are required to dev power module for a certain development process takes prototypes which are charact range of operation conditions t suited solution. Simulations i accompany the developmen although there is currently workflow from the die chara power module model which is cover all design criteria of converter system.

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Parameter Extraction for an ANN-assisted IGBT Model in Transient Simulations

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Abstract

The development of power IGBT devices require an accurate transient model over multiple currents and voltages. With the Artificial Neural Network (ANN) assisted diode model and the modified Angelov-based capacitance model, a new IGBT model describes both the overshoot of collector current and collector-emitter tail voltage at different bias conditions. Given a completed parameter extraction workflow, a comprehensive good fitting of the transient current and voltage waveforms is verified at both the turn-on and turn-off process for currents from 30 to 600 A and voltages from 100 to 820 V.

1 Introduction

The IGBT devices attracts lots of industrial interests in power modules and electrical vehicles. The accurate modeling of switching behavior of power devices can help to accelerate the development cycles, analyze the power loss and determine the electromagnetic compatibility [1–3]. In contrast, unlike only one or several bias conditions are dealt with in most literature, such as [4–11], the actual applications of power modules over a wide range of currents and biases challenge the stability and accuracy of an IGBT model. We recently proposed a new ANN-assisted reverse recovery characteristics of diode model for IGBT devices[12]. The collector current (i_C) of IGBT is well fitted up to 600 V at currents from 30 to 500 A. In this paper, The packaging parasitic networks surrounding the IGBT devices are considered but not shown in the schematic. V_{DC} is the DC supply voltage. V_{pulse} is the pulse voltage source. $R_{G,ext}$ is the extrinsic gate resistance. L_{stray} is the lumped stray inductance. L_{load} and R_{load} are the load inductance and resistance, respectively. L_s is the lumped inductance at the source side. I_L is the load current. i_C, v_{GE} and v_{CE} are the measured collector current, gate-emitter voltage and collector-emitter voltage of the IGBT at lower side, respectively. Fig. 1(b) shows the internal capacitances in the IGBT model. C, G, E, G' and B' are the collector, gate, emitter, internal gate and base nodes, respectively. D' and S' are also shown for internal nodes of the MOS model. $R_{G,int}$ is the intrinsic gate resistance. C_{GD}, C_{GS}, C_{BE}, C_{Diode} are the gate-drain, gate-source, base-emitter and diode capacitances, respectively.

Learn more about Keysight Power Electronics Design

Technical Papers – Converter Design, EMI, Parasitics

Digital Twin Model understanding Printed Wiring Board Effects in High Efficiency Switching Power Supplies

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***Abstract*— The conventional simulation-based procedures used for Switch Mode Power Supplies (SMPS) design treats the printed circuit board (PCB) as an interconnect. The complex electromagnetic (parasitic) properties of the PCB in general have been ignored. Wide bandgap devices such as SiC and GaN MOSFETs have faster switching edges and enable higher switching frequencies than Silicon devices. These characteristics cause, the effects of capacitive coupling and inductance in the PCB to become significant and limiting performance. This paper illustrates the use of modern EDA methodologies to quantify these effects and optimize the overall performance of a high power boost converter.**

Keywords—Digital Twin, PCB simulation, EM extraction, switching behavior, coupling, Wide bang gap half bridge design

I. INTRODUCTION

The issue of the effect of the PWB layout on circuit performance was faced by the microwave design community a generation ago. The design tool companies responded by developing fast 2 ½ D simulators that characterized the layered metallization, dielectric and via properties of a PCB up to microwave frequencies. These tools have now been repurposed for SMPS designs.

Keysight Technologies and Wolfspeed have recently worked together on the simulation of a half-bridge design that takes into account the electromagnetic properties of the PCB. Simulation and measurements are compared for both Clamped Inductive Switching and a 10KW Synchronous Boost Converter. The Keysight PATHWAVE Advanced Design System (ADS) is a mature design environment with major users in the microwave and high-speed digital community. It is generally not that familiar to the SMPS community. The tool has multiple types of solvers available and the "Transient Solver" can trace its origin back to the original Berkley SPICE. The tool has a graphical user interface and the netlist is not visible to the user. A new user has to import the semiconductor SPICE models and generate the circuit with the layout. For the first task, ADS has import capability for the various SPICE dialects including LTSPICE, PSPICE, HSPICE and Spectre. The layout and circuit can either be built from scratch or imported from any layout file.

Simon Muff

Importance of Switched-Mode Power Supply IC Model for Conductive EMI Noise Simulation

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***Abstract*—This paper proposes a modeling method for switched-mode power supplies (SMPSs) mainly focusing on IC model for conductive noise simulation. In modern automobiles, the number of electronic control unit (ECU) are increasing in order to implement advanced features and introducing an all-electric or hybrid drive system draws a high current. Since this requires higher efficiency power systems, SMPSs are widely used. Although systems using SMPSs produce switching noise as a side effect, they have to be designed to work as expected and to satisfy EMC regulation, too. To achieve this goal, it is imperative to predict and control the amount of noise at an early stage in the design by using accurate simulation models to reproduce the system behavior. Doing so greatly contributes to reducing design cost. However, it is very difficult to build SMPS IC models for noise simulation. In this paper, induced conductive EMI noise was evaluated through Electro-Magnetic (EM) and SPICE co-simulation following CISPR25 regulations. The SMPS, PCB, load device, line impedance stabilization network (LISN), and cables were all modeled to reproduce the regulation test environment. This model was validated by measurement on the same conditions as simulation.**

Keywords— EMI; EMC; Inverter/Converters for Electric Vehicles; Evaluation

I.INTRODUCTION

The adoption of electronics in automobiles keeps progressing as a result of the popularization of EV/PHEV and the expectation of an autopilot system in vehicles. Along with this progress, there is a trend for an increasing number of ECUs installed in automobiles, and as a result the current consumption is also increasing. For example, more than 100 ECUs are installed in a luxury car and large scale FPGA, used for ADAS (Advanced Driving Assist System) image processing, requires large-current at modest voltage. Hence, SMPSs which are excellent in terms of efficiency are widely used for the power supplies of ECUs. SMPS can perform buck, boost, and buck-boost conversion. However, it has demerit of generating high frequency noise caused by its switching operation.

Since devices are mounted closely to each other due to the increase in ECUs, the problem caused by interference of high frequency noise generated from the devices has become more serious than before. This noise can lead to ECU and automobile malfunction, and in worst case, it may cause an accident that would lead to the loss of human live. To avoid these from happening, committees (CISPR, IEC, EN, etc.) were founded to set strict regulations on the noise interference

An ECU design cannot proceed to mass-production unless it has passed the standards set by the committees. Ideally, EMC counter-measures to pass each regulation would be validated during the development stage, but actually they are often carried out
standards the de
beginning. Mor
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space to mount
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counter-measure

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Fig. 1. Wavefo
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time validating
difficult to get
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Analysis of PCB parasitic effects in a Vienna Rectifier for an EV battery charger by means of Electromagnetic Simulations

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Keywords

Power Converters for EV, Power factor correction, Simulation, Silicon Carbide (SiC), Battery charger.

Abstract

The aim of this work is to investigate the impact of the PCB (Printed Circuit Board) electrical parasitic parameters on the performances of a SiC Three-Level T-type rectifier used for electric vehicle battery chargers. The short switching times of the SiC devices enables high switching frequency at very high efficiency. On the other hand, as the time derivative of the current increases (as a rule of thumb we can set 1A/ns as a breaking point), PCB parasitics start to play a significant role and may cause the degradation of the performances or even a design failure, if not taken into account right from the first design stage. Industry standard EDA (Electronic Design Automation) tools can be used to extract a model for the PCB to evaluate all the unwanted effects introduced by the physical realization of the board layout. For the scope of the current study, the software *Advanced Design System ADS* by

Exploiting the Benefits of Partially Saturating Inductors on Switch-Mode Power Supplies Electro-Magnetic Compatibility and Efficiency

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Understanding the Impact on parasitic Probing Effects onto the PCB Power-to-Control Crosstalk in Switch-Mode Power Supplies

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pm

pplies (SMPS) can be dominated by
apparently harmless elements of the
ground planes, and the setup of the
e the PCB PCC in power converters
g in measurements, which can mask
ena.

ic MOSFET gate drive pulse se-
teady-state operation, depending on
nt level. As long as the PSM activa-
aperiodic MOSFET gate drive pulse
here are no undesired EMI implica-
resulting input current spectrum is
d the switching frequency harmonics.
under certain operating conditions,
y the combination of input voltage,
, output current, switching frequency
characteristics, the PSM activation
eriodic MOSFET gate drive pulse se-
his case, a certain number of regular
les is followed by one-half switching
cle, which results in a subharmonic
ation that can be easily confused with
enomenon occurring in peak-current-
led regulators with an unstable cur-
6], the EMI impact of a PSM-induced
harmonic operation of TI-PMLK
4160 peak-current buck regulator is
he paper also emphasizes the influ-
e transconductance error amplifier,
in peak-current control, can play on
subharmonics and EMI. In particular,
EMI becomes more significant if the
esigned to achieve a high cross-over

ents and
inductors
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out.

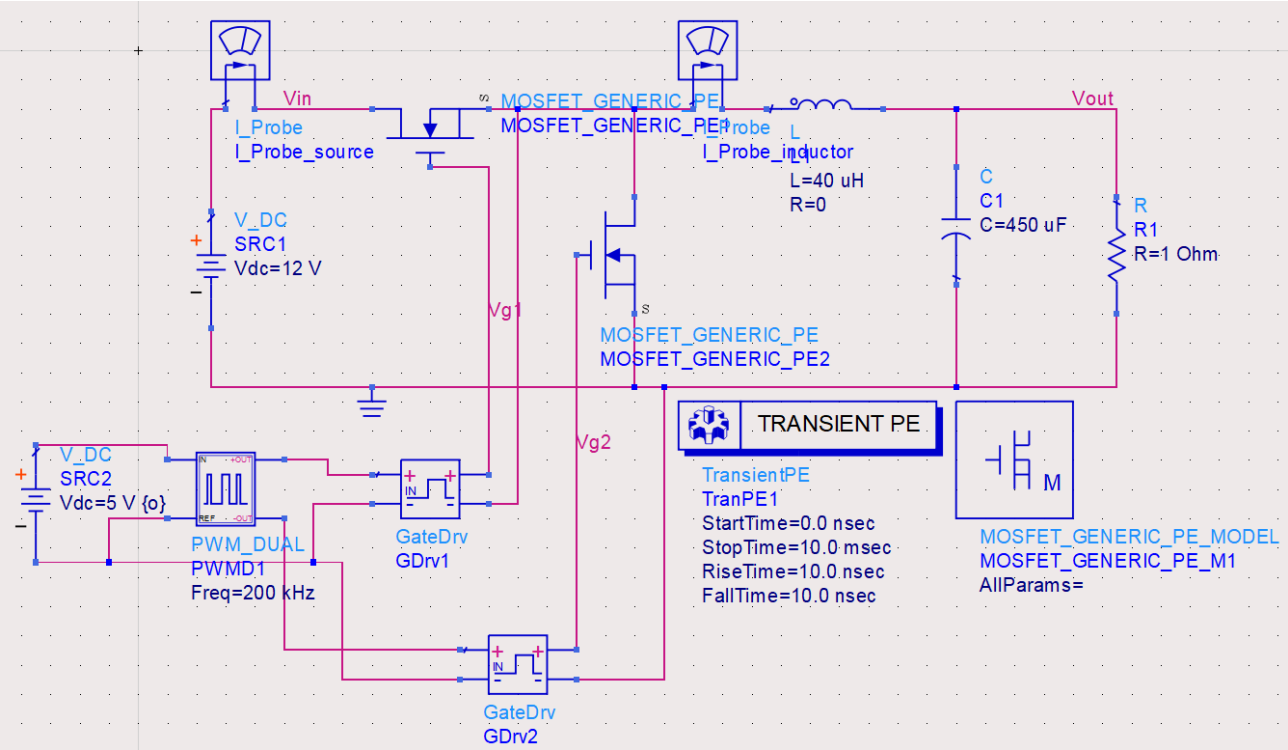
Normally, the worst case operations for EMC compliance are the ones generating the highest noise level. The maximum load is typically considered as the worst-case, and the EMC filters for conducted emissions are designed based on the differential mode and common mode noise spectrum under these conditions. The peak noise at the switching frequency is used as reference for the selection of the filter resonance frequency, based on the EMC standard of interest, and the *L* and *C* parameters are consequently determined. Although the resulting SMPS with embedded EMI filter can comply with the given EMC standard at maximum load, there can be low load operating conditions causing additional low frequency noise in the SMPS, which can cause interference to the surrounding devices. This may happen because of the Light Load Operation-Loss Reduction (LLO-LR) techniques implemented by most of ICs featuring SMPS control, which are required in all the applications involving stand-by and sleep modes. The simplest LLO-LR technique is to reduce the switching frequency under LLO. Frequency Modulation (FM) techniques [6][7] and Pulse-Skip Mode (PSM) techniques [8]-[10] reduce the frequency as the load decreases. FM and PSM may have different embodiments, which may influence EMI, because of increased current and voltage ripples, or determine a pseudo spread spectrum effect, which may facilitate EMC compliance. Moreover, the possible occurrence of Discontinuous Conduction Mode (DCM) under low frequency operation causes larger current ripple and worsen the EMI. Burst Mode (BM), also widely used as a LLO-LR feature, causes EMI worsening. Overall, as the frequency reduction techniques as the many other LLO-LR techniques proposed in literature [11]-[21] mostly have a negative and not easily predictable impact on low frequency EMI. In fact, they may cause subharmonics and/or non-periodic modes whose occurrence is largely influenced by the SMPS design and operating conditions.

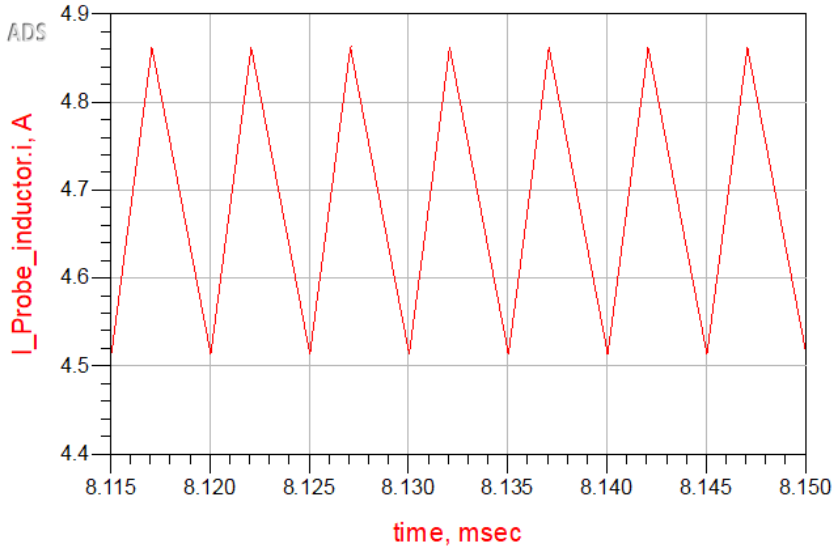
In the recent years, many studies have investigated the possibility of using Partially Saturating Inductors (PSIs) to increase the SMPS power density, compared to Non-Saturating Inductors (NSIs) [22], and several methods are available today for a good prediction of PSI performances and relevant impact on SMPSs [23]-[25]. A good collateral effect of PSIs is the current ripple reduction and the improvement of the efficiency under LLO, thanks to the inductor de-saturation, resulting also in possible EMI reduction due to the prevention of the negative effects caused by the control chip features for LLO-LR.

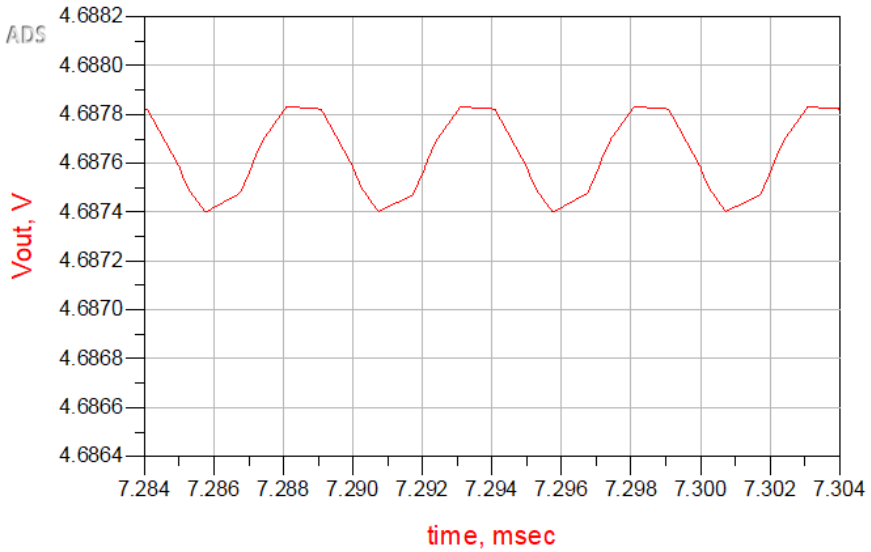
This paper illustrates the benefits of PSIs under LLO, which may help mitigating the effects of PCB parasitics. By

Example design: Synchronous buck open loop power stage

Open loop power stage with switching simulation engine.



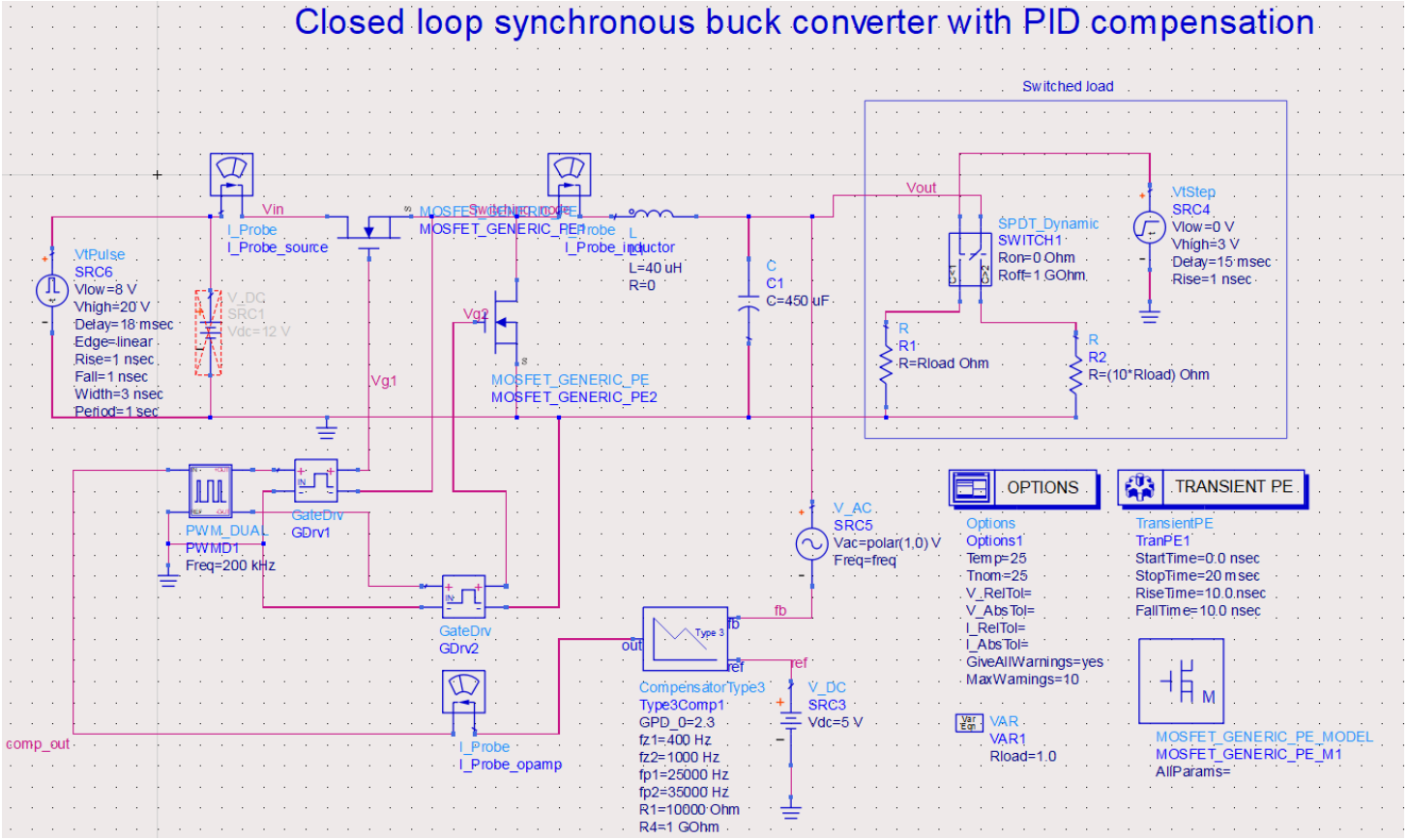




Example design: Closing the loop

Closed loop design: Put the designed block together with the converter.

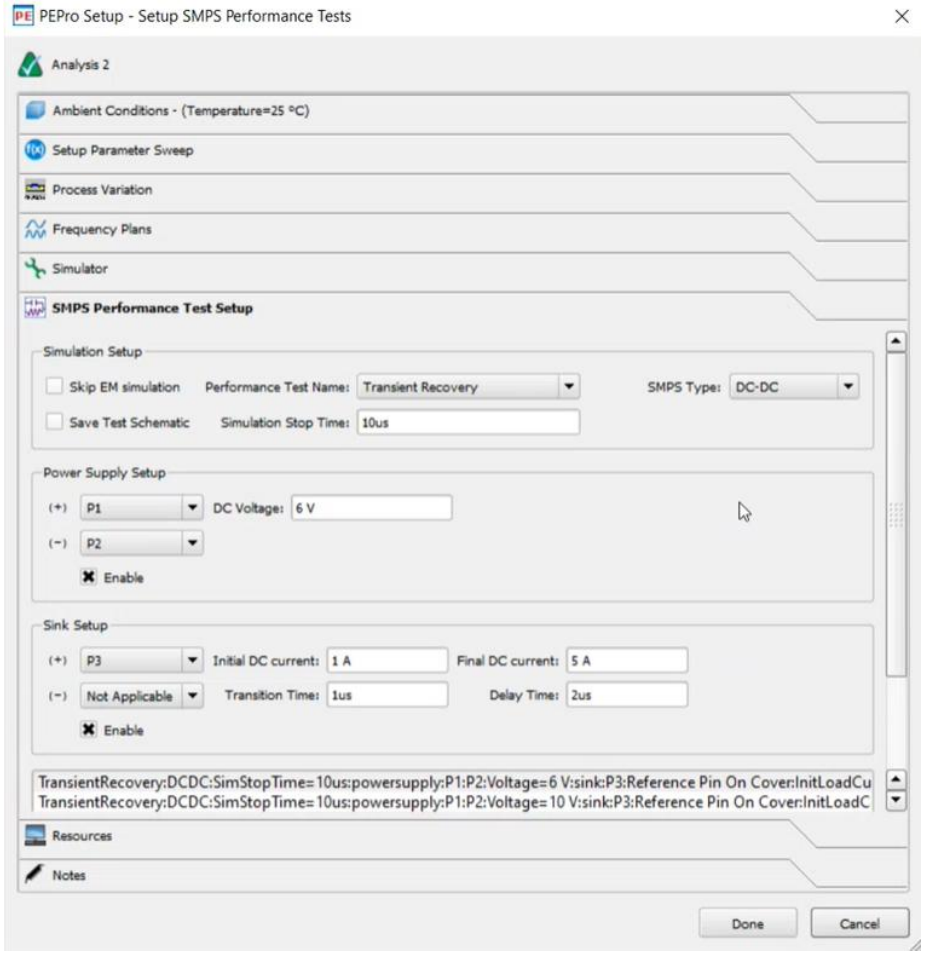
- Designed and implemented the compensation in minutes rather than hours!!
- All of this done on one eco system instead of jumping between MATLAB and circuit simulators.



SMPS Performance Testbench

Easily test your SMPS design without the hassle of complex setups

- SMPS Performance Testbench
- Available both in ADS and PEPro
- A tool to streamline all the common test you do for a SMPS design
  - Transient Recovery
  - Efficiency
  - Switching Losses
  - Electrical Fast Transietn



Thermal analysis in schematics

- Running the schematic level thermal analysis gives us a data display window pop up.
- We get the Power flowing through every device and the junction temperatures.
- This data can be exported to a CSV file for further analysis in PEPro.