

Photonic Designer Enhancing Accuracy with Digital Twin Technology

[Your Name | Title]
[Date]

Agenda

Photonic Designer

- **Challenges in Photonic Design**
- **Introduction to Photonic Designer**
 - How do we address the challenges
 - Demonstrations
 - Achieving model accuracy using digital twin



Photonic Design Flow Challenges

Issues cited by industry leading photonics design teams

- **Predictive Simulation**

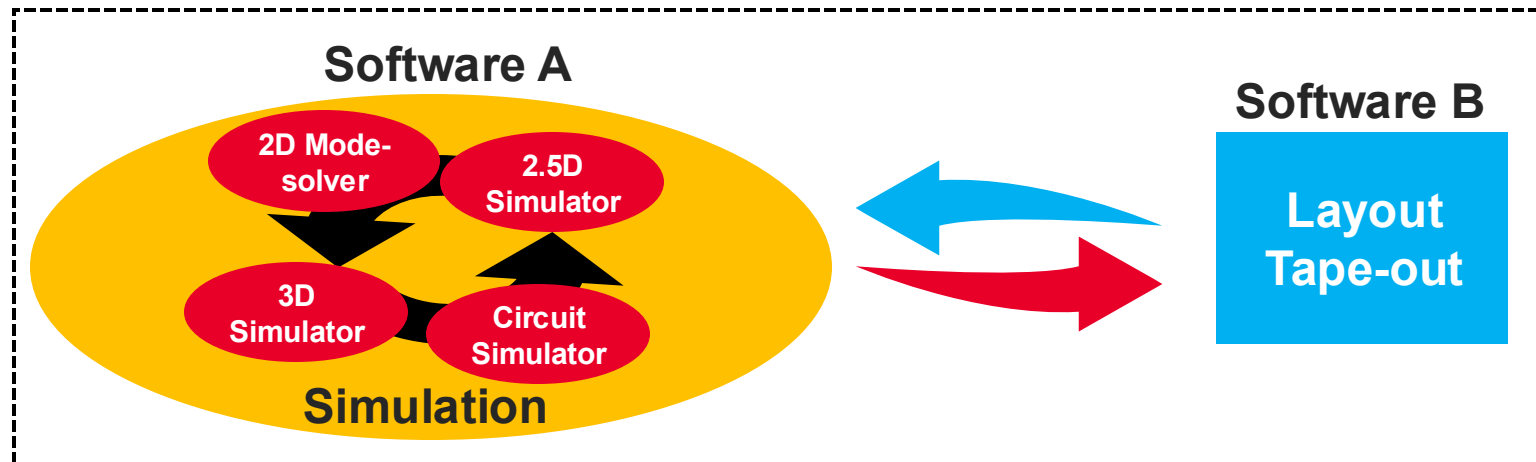
- Lack of accuracy
- Capturing the underlying physics
- Fast simulation
- Achieving yield

- **Photonic Design Workflow**

- Fragmented solutions
- Manual efforts – lack of automation

- **Design & Test Eco-system**

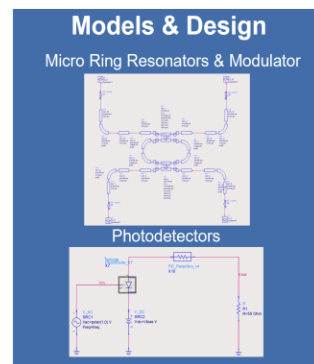
- Not an easy way to correlate design and test results
- Using measurements to update models



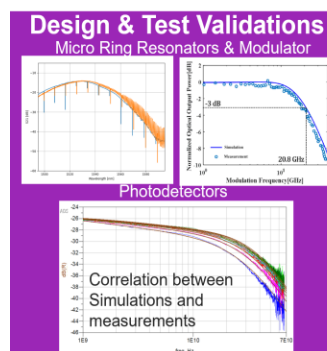
Key Features

Electronic Photonics Design Automation (EPDA)

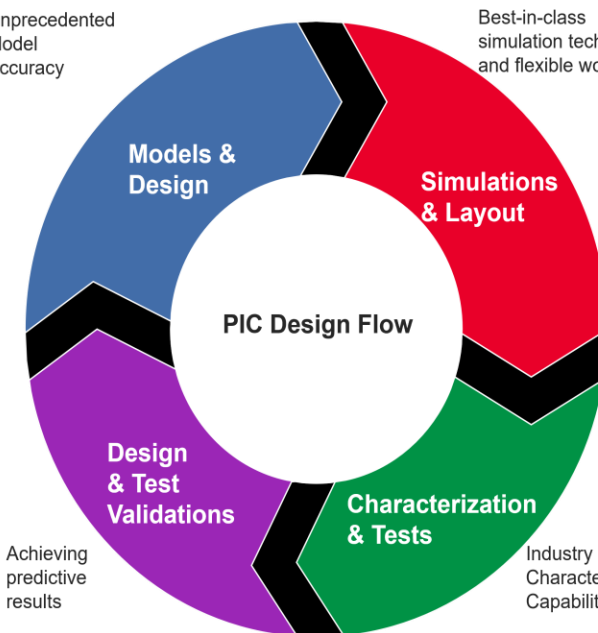
- Best-in-Class Models
 - Unprecedented accuracy
- Leverage platform
 - Integrated PIC workflow in ADS (schematic, layout, simulation)
 - Integrated circuit and system (Dataflow + ADS circuit simulation)
 - Integrated EPDA (E-O-E) workflow
 - Foundry program experience
- Design and test engineering lifecycle
 - Modeling, characterization, model extraction from measurements expertise
 - Standards compliance (400GBASE-LR8, CEI-VSR-PAM4, etc.)
 - Keysight Requirements Verification Suite
- High frequency application expertise



Unprecedented
Model
Accuracy

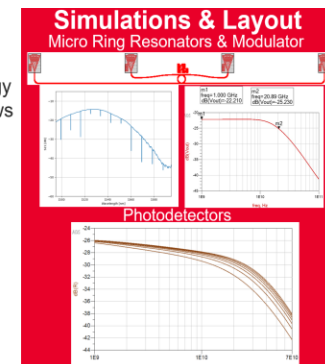


Achieving
predictive
results



E-O-E design, simulation and measurement flow

Best-in-class
simulation technology
and flexible workflows



Industry Leading
Characterization
Capabilities



Photonics Design Cycle

Idea

Schematic

Simulation

Layout Generation

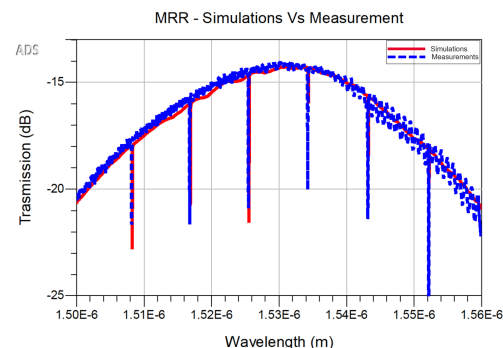
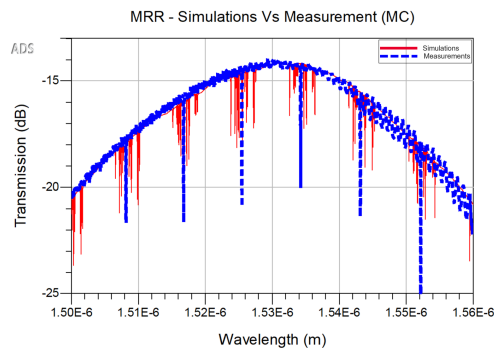
Foundry

Model refinement based on analysis

Yield Analysis

Sim. Vs Measurement

Chip/wafer level characterizations



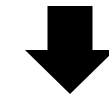
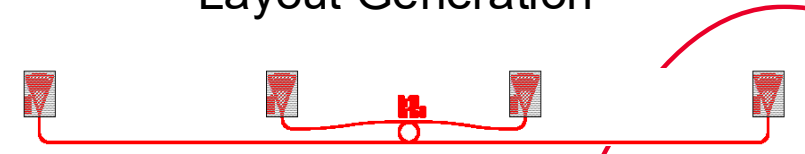
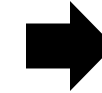
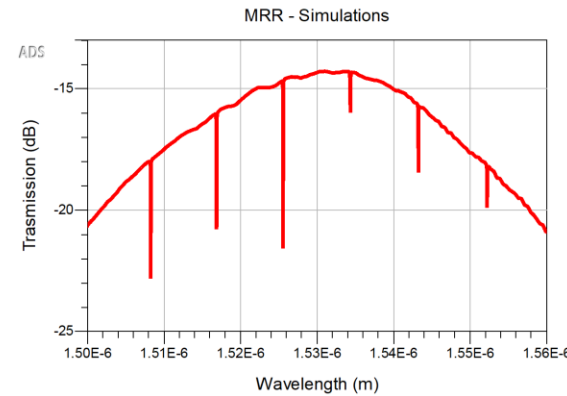
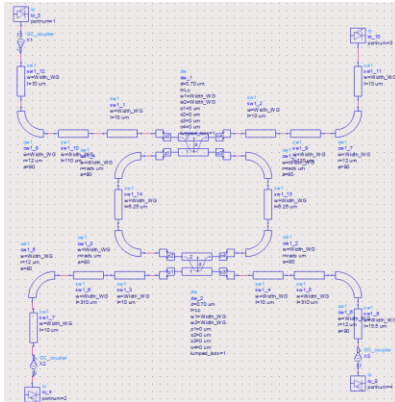
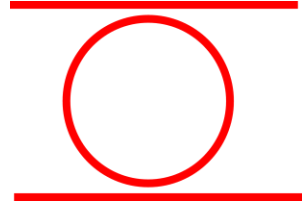
Photonics Design Cycle

Schematic

Simulation

Layout Generation

Idea



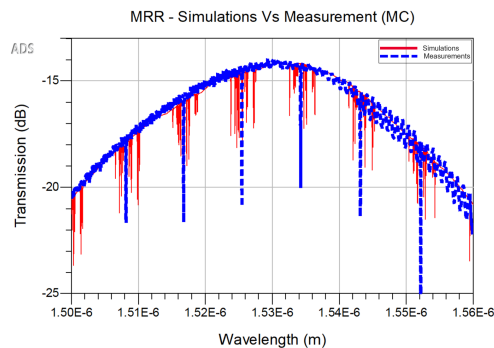
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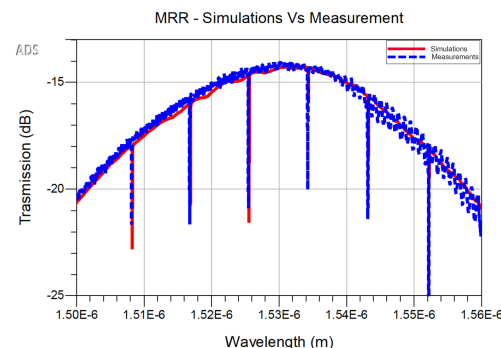
All design steps in a single platform - Advanced Design System (ADS)

Model refinement based on analysis

Yield Analysis



Sim. Vs Measurement



Chip/wafer level characterizations



Use Cases

- Component Design
 - Photonics components design
 - Accurate models
- Circuit Design
 - Circuits using components
 - Photonics subsystems
- System Design
 - System using the circuits

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Components Design

Photo Detector (PD)

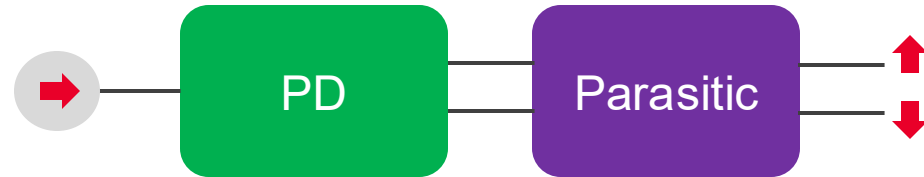
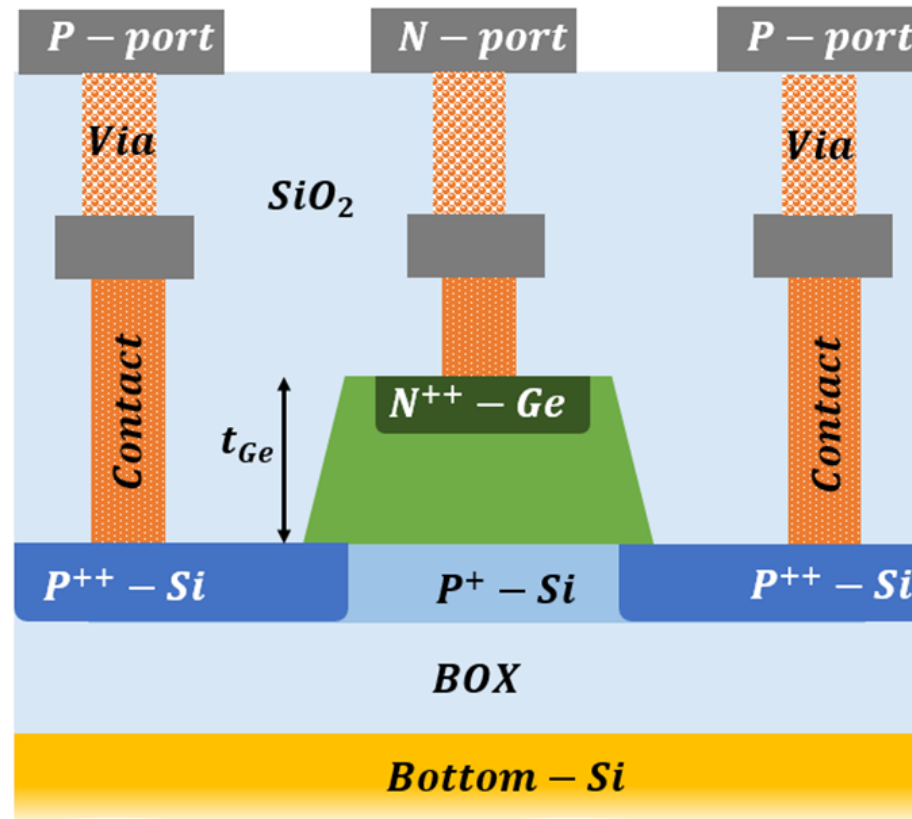
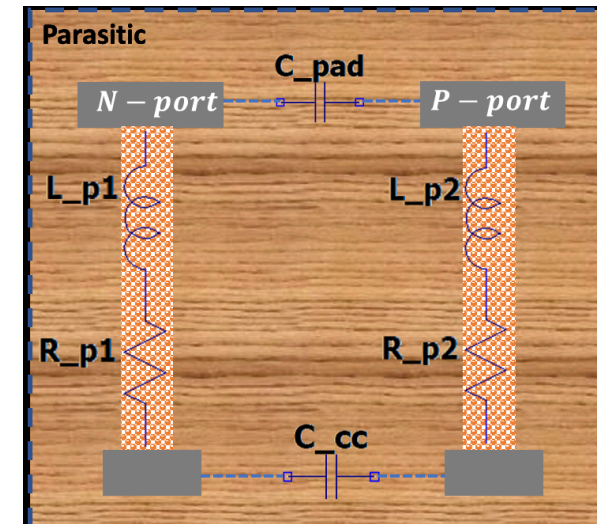


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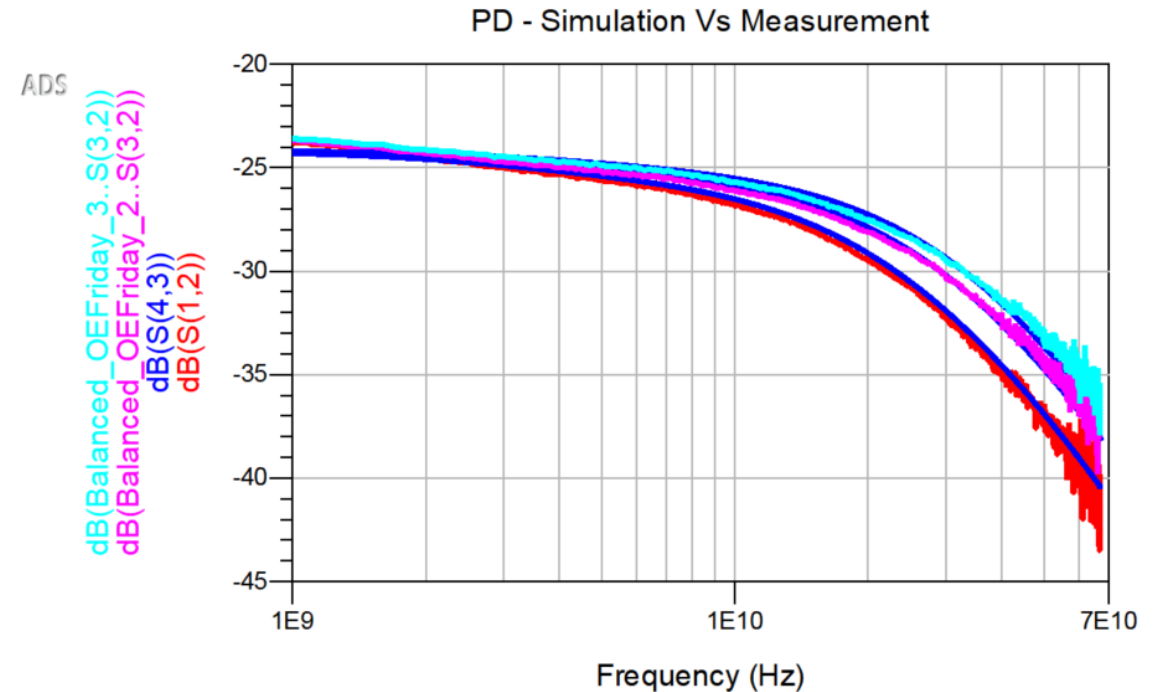
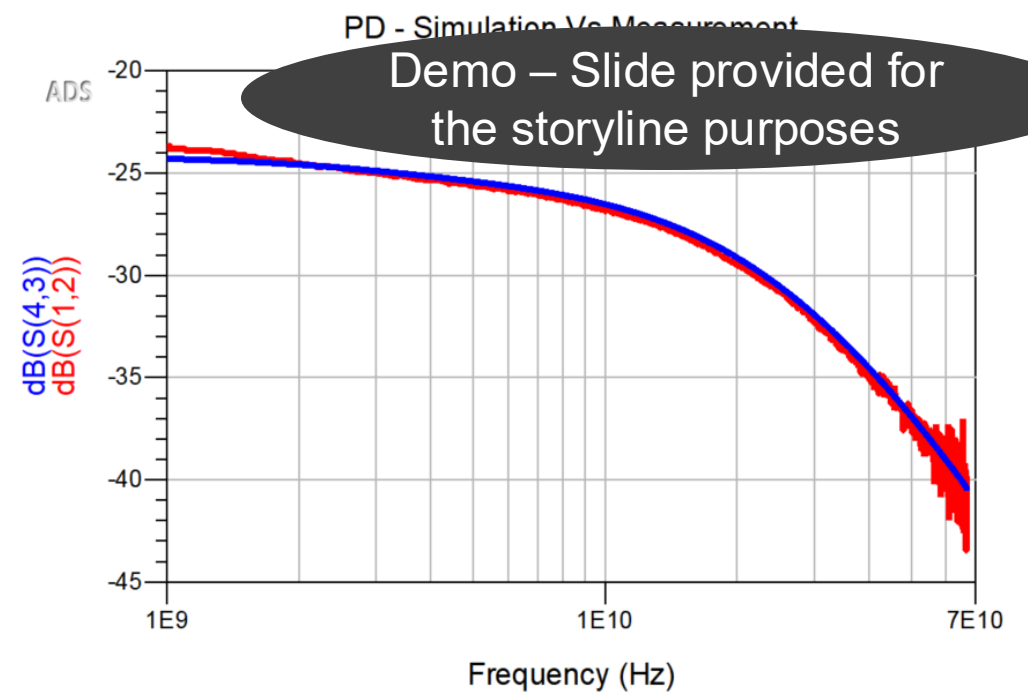
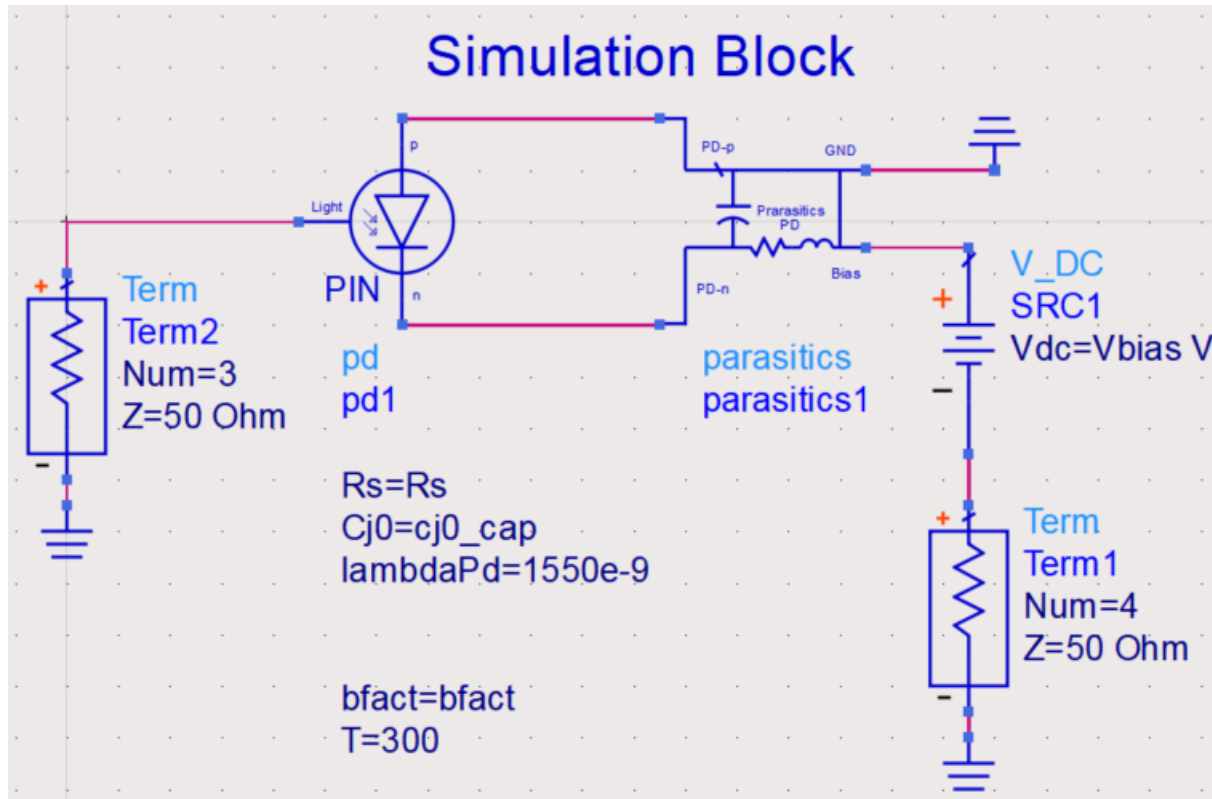


Parasitic



Components Design

Photo Detector (PD)

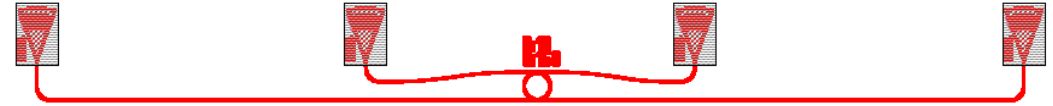
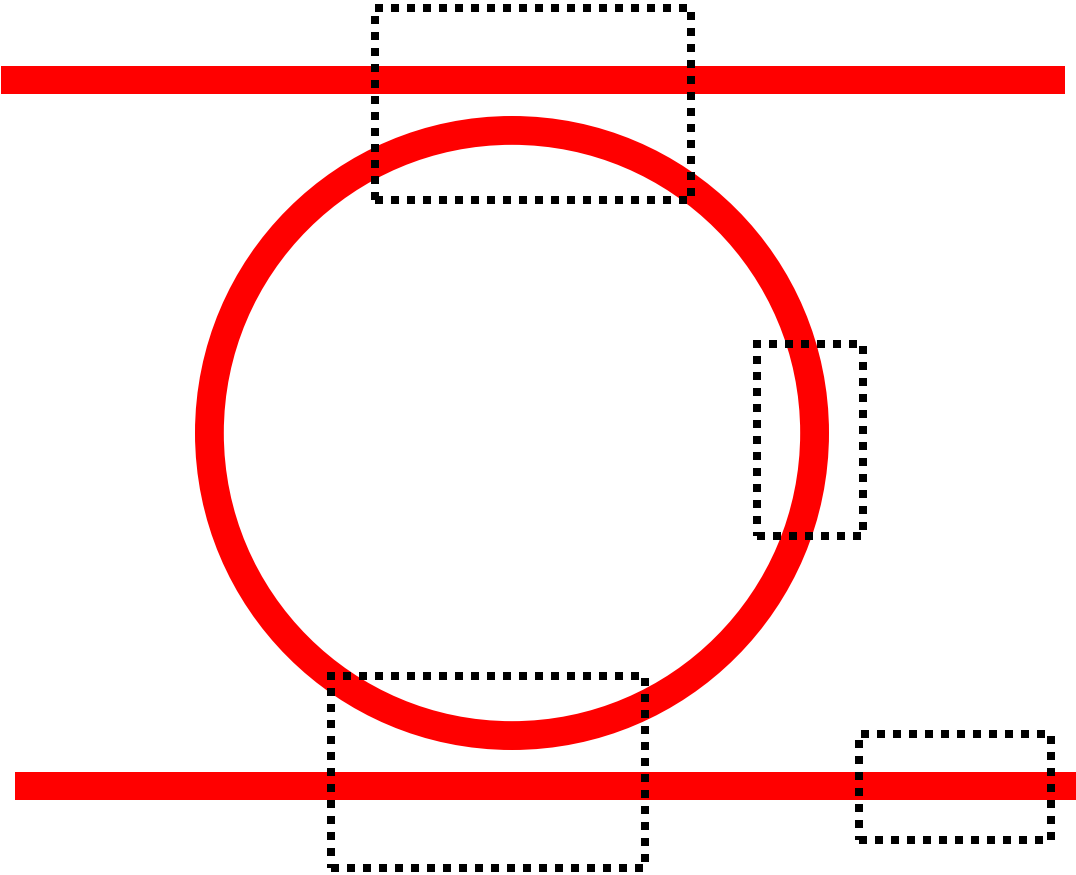


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Circuit Design

Micro Ring Resonator (MRR)



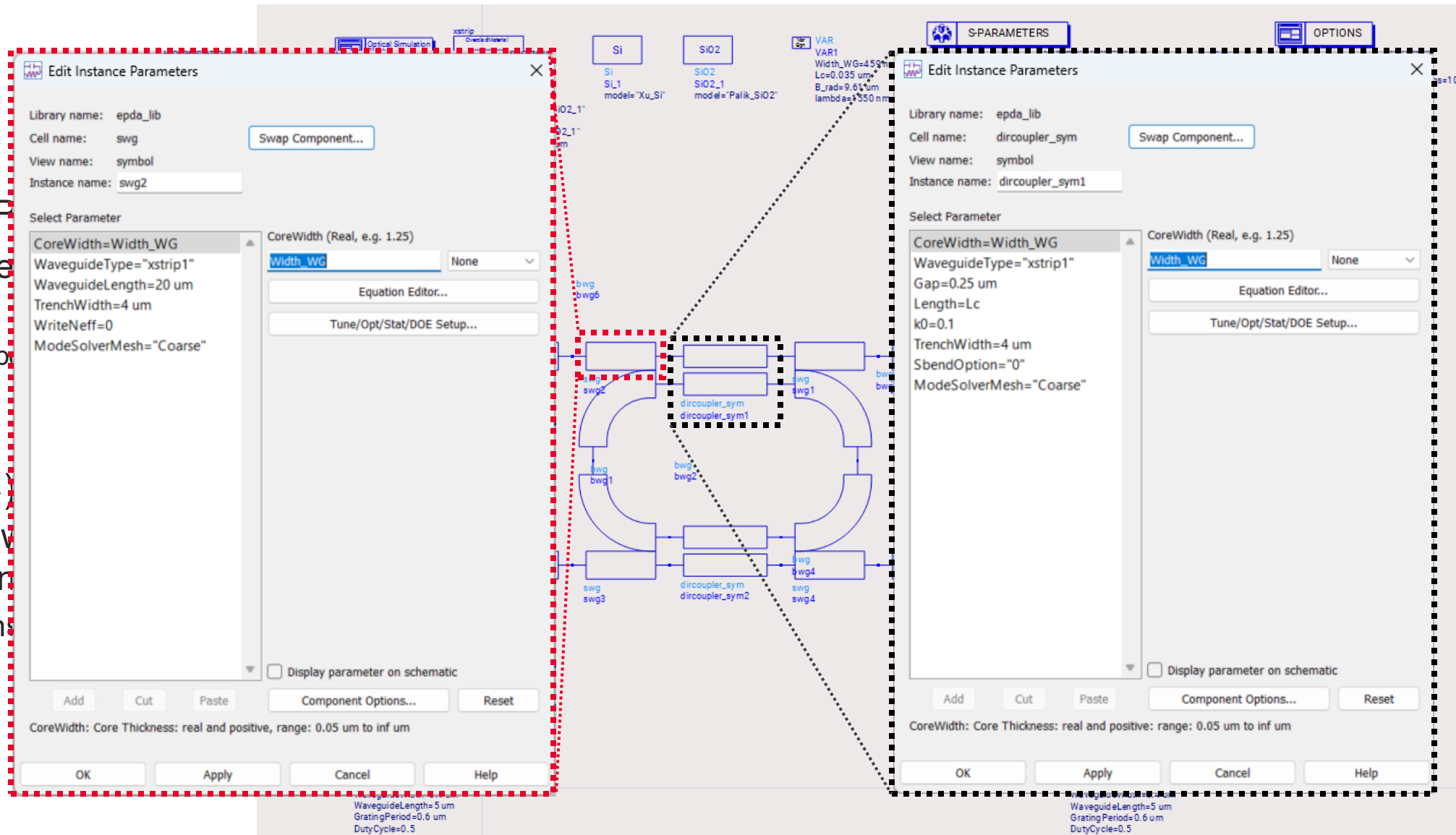
- Directional Coupler
 - Bend waveguide
 - Straight waveguide
-
- Simulate the circuit
 - Modesolver

Circuit Design/Simulation

MRR Schematic

- Simulations
 - MRR on Golden P
 - Wavelength range
 - 1500-1560 nm
 - 1500 wavelength p
- Monte-Carlo (MC)
 - 1% variations on v
 - (WG) width (443 n
 - To mimic variations
 - WG thickness
 - WG width

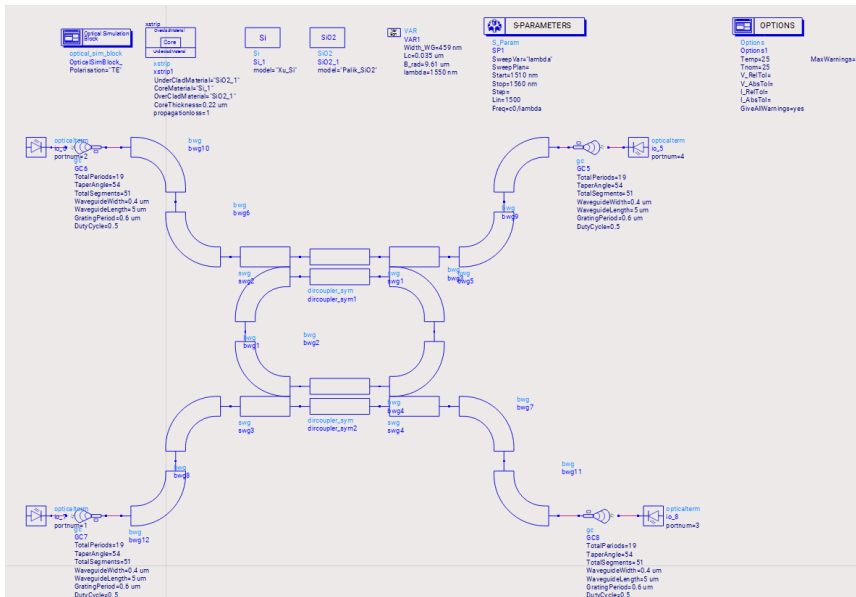
Demo – Slide provided for the storyline purposes



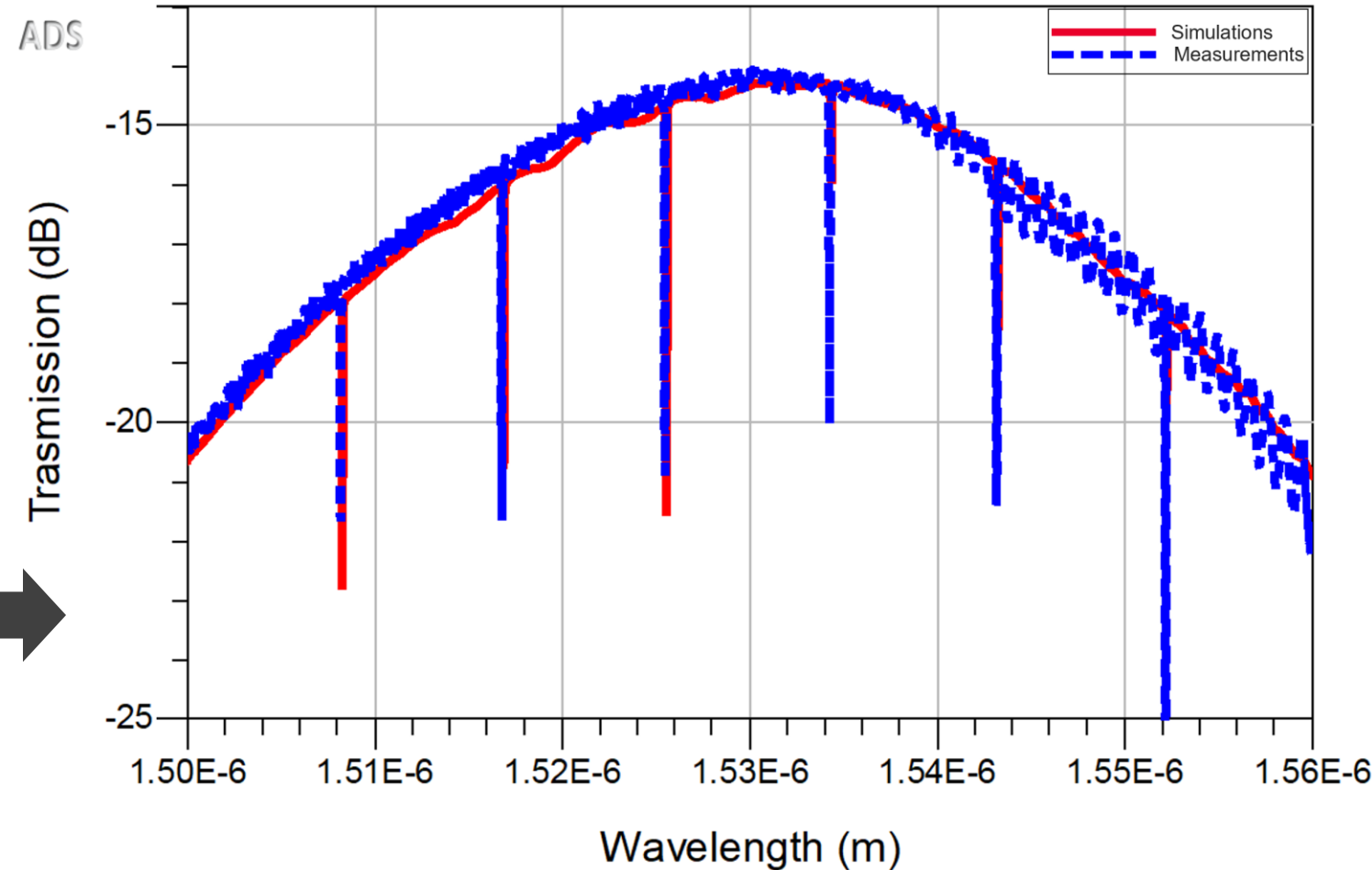
Circuit Design/Simulation

Results

- Measurements
- Golden PIC MRR structure
- λ : 1500 – 1560 nm
- Good match b/w Sim. & Measurement



MRR - Simulations Vs Measurement

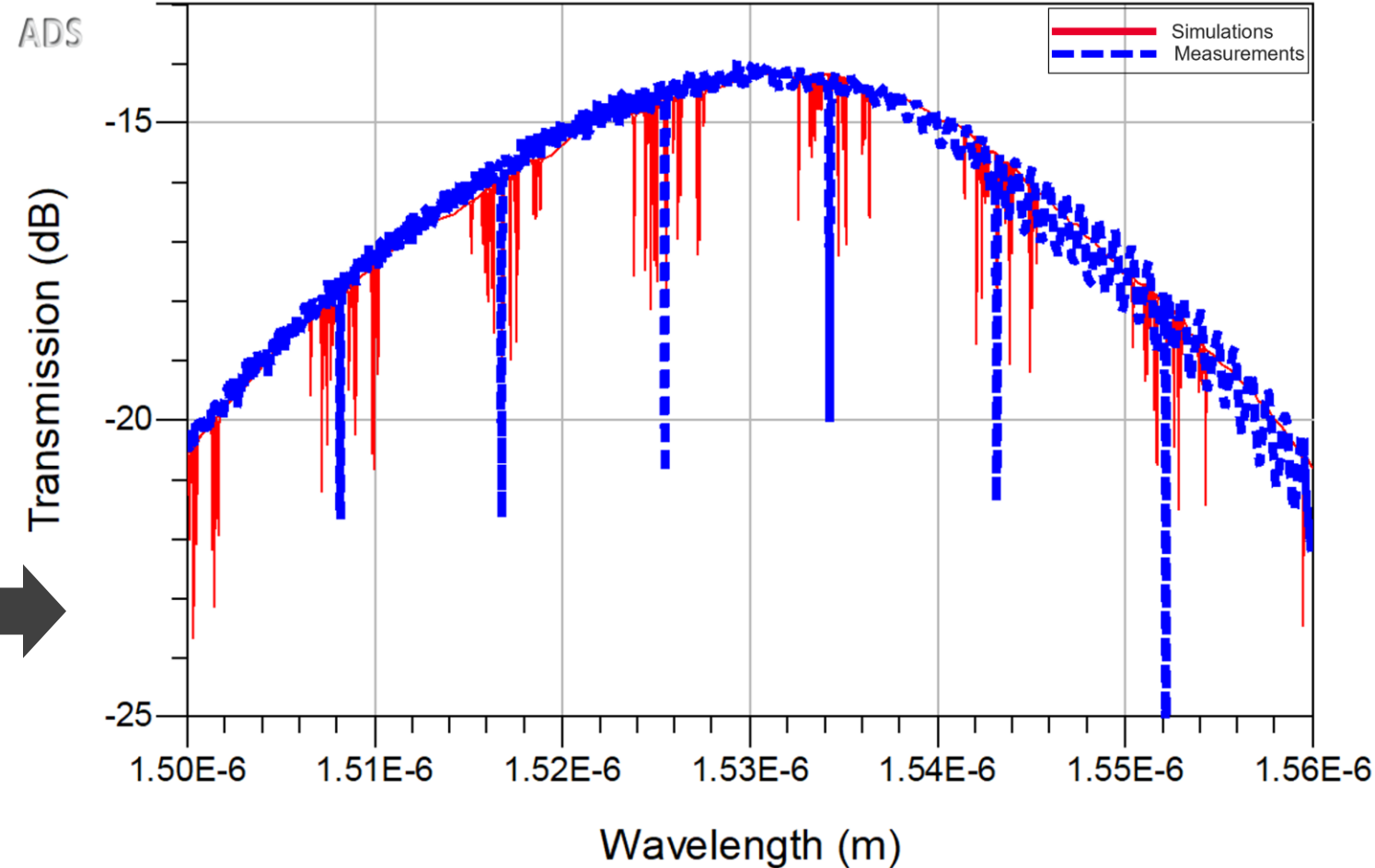
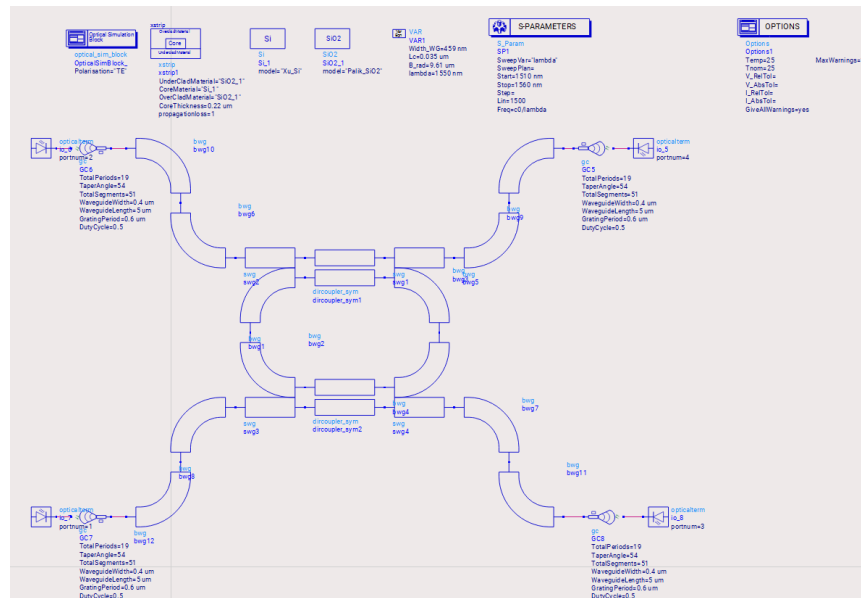


Circuit Design/Simulation

Results including Monte Carlo

- Measurements
 - Golden PIC MRR structures
 - λ : 1500 – 1560 nm
- Monte Carlo -> WG width variations

MRR - Simulations Vs Measurement (MC)



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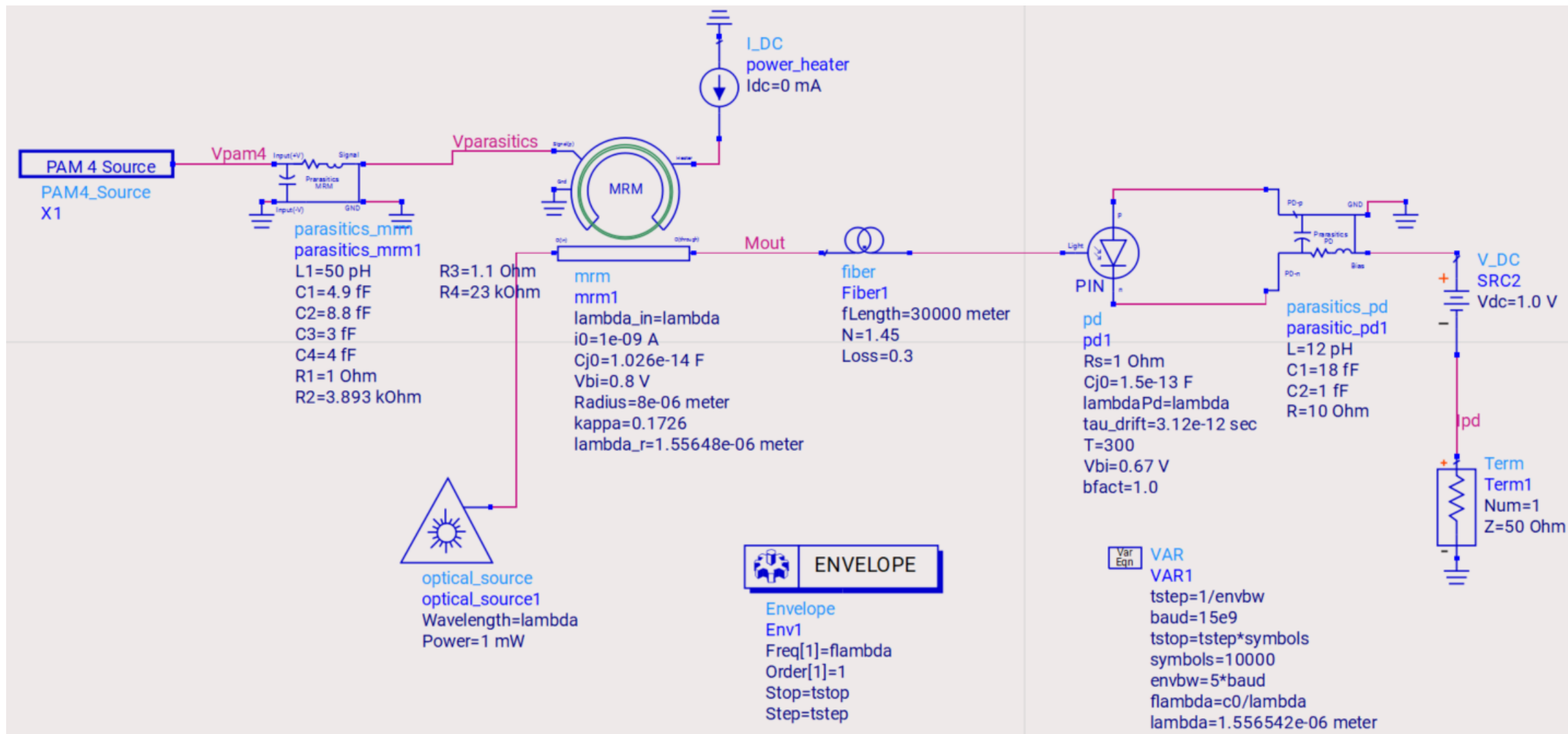
EOE simulation

PAM4



EOE simulation

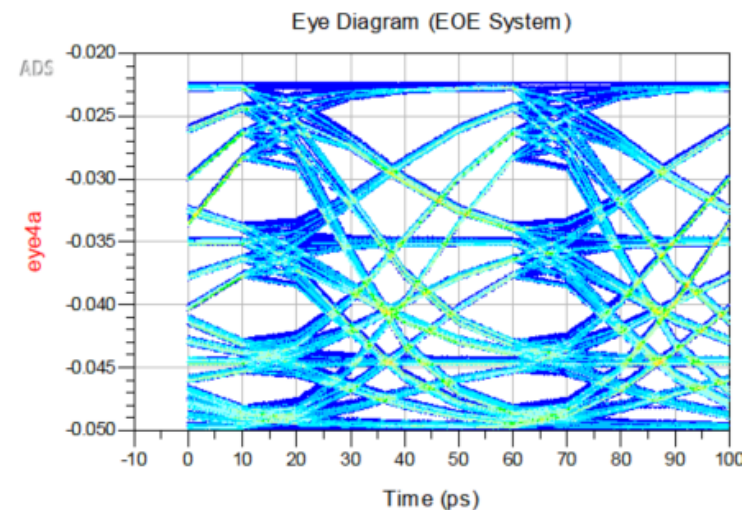
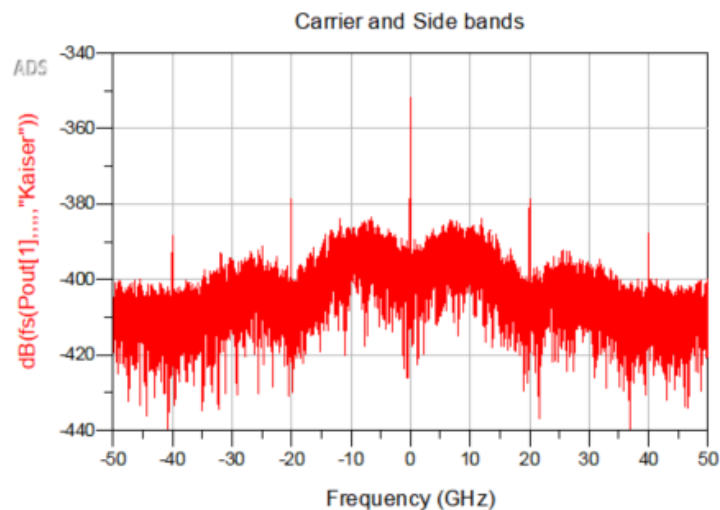
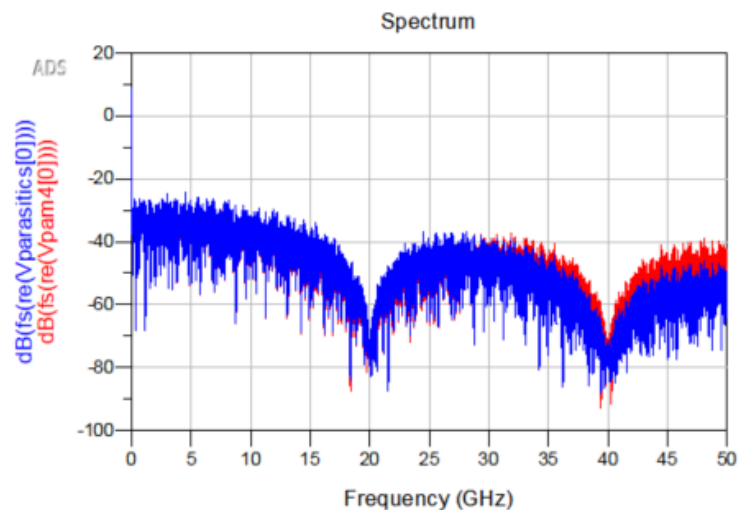
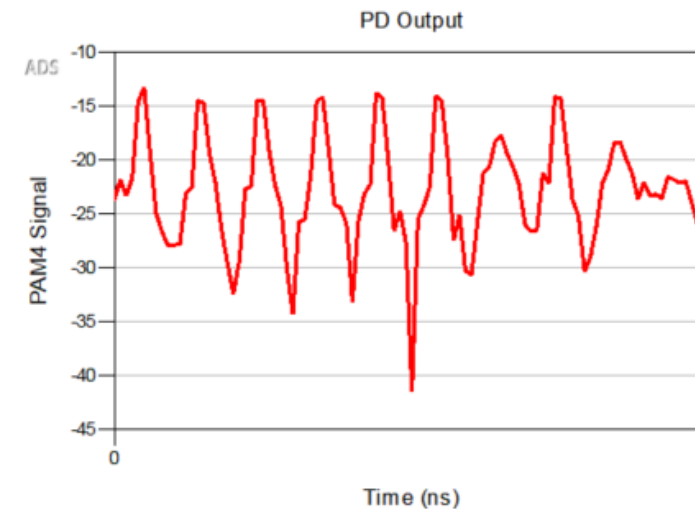
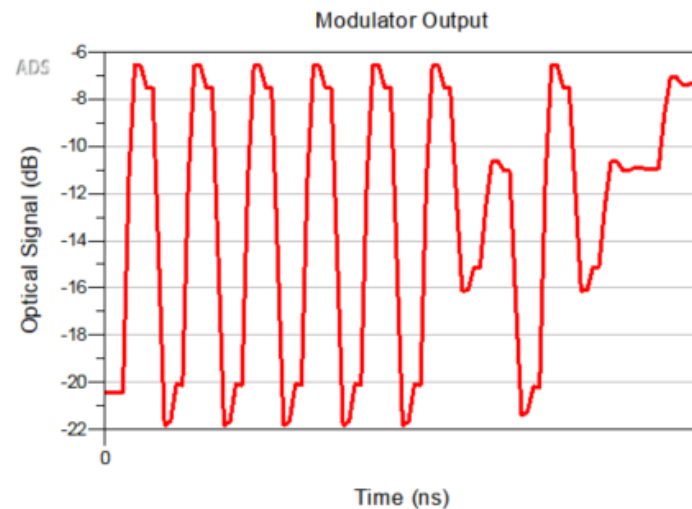
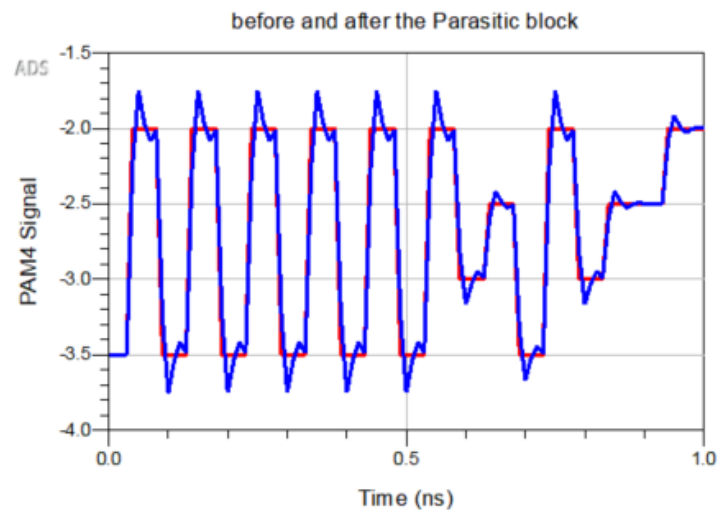
PAM4



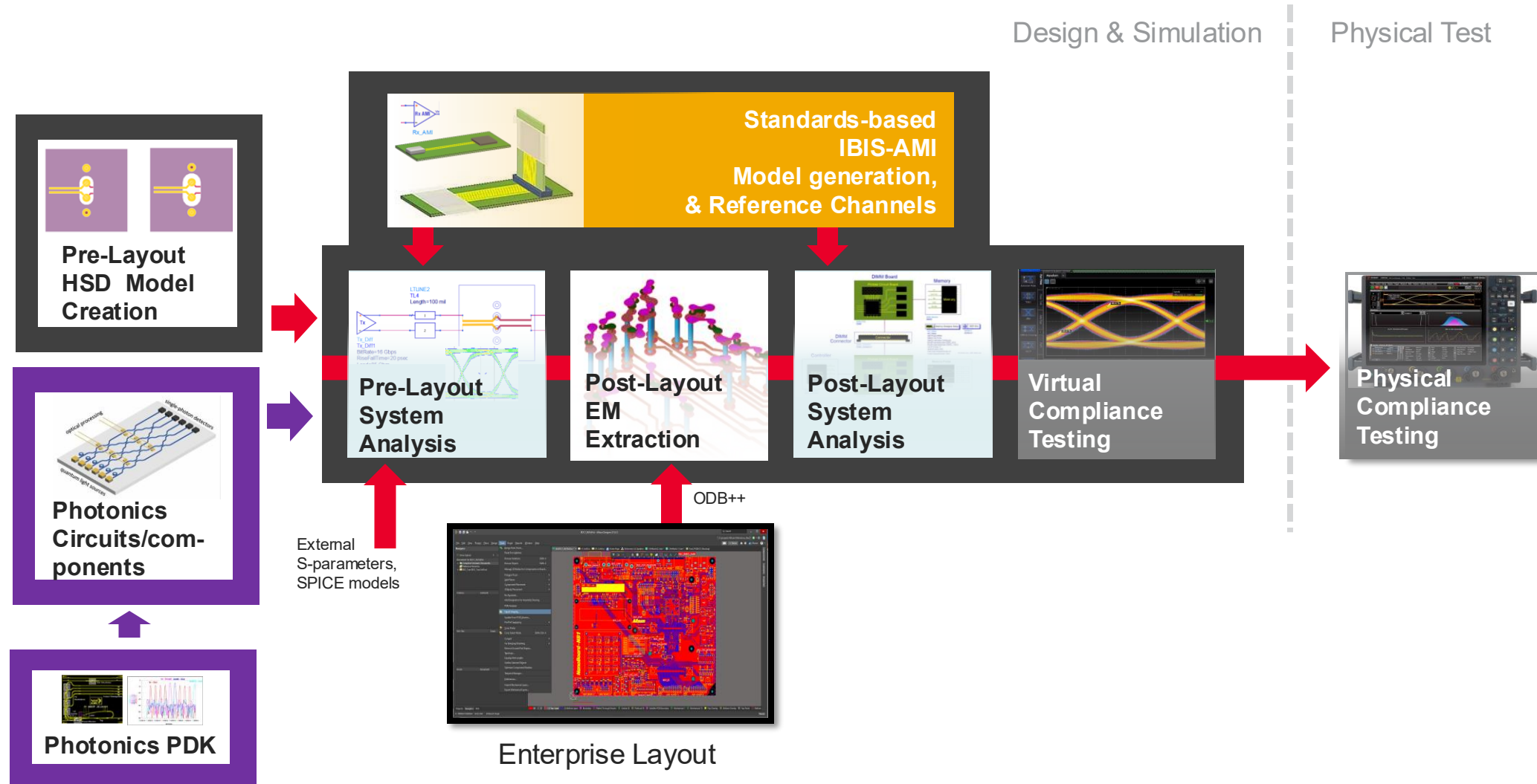
EOE simulation

PAM4

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High Speed Digital + Photonics Workflow





Summary

Photonic Designer